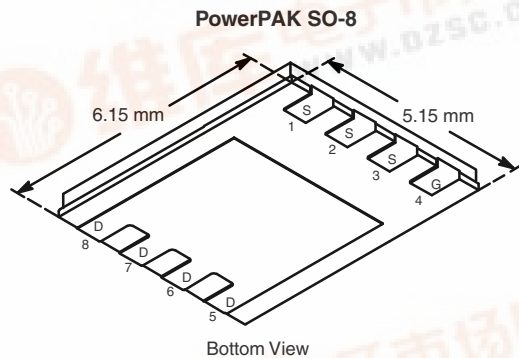


## P-Channel 200 V (D-S) MOSFET

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)
- 200	0.174 at V <sub>GS</sub> = - 10 V	- 3.8	88
	0.180 at V <sub>GS</sub> = - 6 V	- 3.6	



Ordering Information: Si7431DP-T1-E3 (Lead (Pb)-free)  
 Si7431DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

### FEATURES

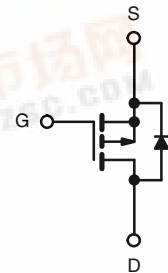
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Power MOSFETs
- Ultra-Low On-Resistance Critical for Application
- Low Thermal Resistance PowerPAK<sup>®</sup> Package with Low 1.07 mm Profile
- 100 % R<sub>g</sub> and Avalanche Tested
- Compliant to RoHS Directive 2002/95/EC



**RoHS**  
 COMPLIANT  
 HALOGEN  
**FREE**  
 Available

### APPLICATIONS

- Active Clamp in Intermediate DC/DC Power Supplies



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)				
Parameter	Symbol	10 s	Steady State	Unit
Drain-Source Voltage	V <sub>DS</sub>	- 200		V
Gate-Source Voltage	V <sub>GS</sub>	± 20		
Continuous Drain Current (T <sub>J</sub> = 150°C) <sup>a</sup>	I <sub>D</sub>	T <sub>A</sub> = 25 °C	- 3.8	- 2.2
		T <sub>A</sub> = 70 °C	- 3.0	- 1.8
Pulsed Drain Current	I <sub>DM</sub>	- 30		A
Continuous Source Current (Diode Conduction) <sup>a</sup>	I <sub>S</sub>	- 4.2	- 1.6	
Single Pulse Avalanche Current	I <sub>AS</sub>	- 30		mJ
Single Pulse Avalanche Energy	E <sub>AS</sub>	45		
Maximum Power Dissipation <sup>a</sup>	P <sub>D</sub>	T <sub>A</sub> = 25 °C	5.4	1.9
		T <sub>A</sub> = 70 °C	3.4	1.2
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) <sup>b, c</sup>		260		

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>a</sup>	R <sub>thJA</sub>	t ≤ 10 s	18	23	°C/W
		Steady State	50	65	
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	1.0	1.5		

Notes:

- Surface mounted on 1" x 1" FR4 board.
- See solder profile ([www.vishay.com/ppg?73257](http://www.vishay.com/ppg?73257)). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.



SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
<b>Static</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = - 250 μA	- 2.0		- 4.0	V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = - 200 V, V <sub>GS</sub> = 0 V			- 1	μA
		V <sub>DS</sub> = - 200 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C			- 10	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = - 10 V, V <sub>GS</sub> = - 10 V	- 20			A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 3.8 A		0.145	0.174	Ω
		V <sub>GS</sub> = - 6 V, I <sub>D</sub> = - 3.6 A		0.147	0.180	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = - 15 V, I <sub>D</sub> = - 3.8 A		17		S
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = - 4.2 A, V <sub>GS</sub> = 0 V		- 0.78	- 1.2	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = - 75 V, V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 5.2 A		88	135	nC
Gate-Source Charge	Q <sub>gs</sub>			16.5		
Gate-Drain Charge	Q <sub>gd</sub>			25		
Gate Resistance	R <sub>g</sub>		1.5	3	4.5	Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = - 75 V, R <sub>L</sub> = 15.5 Ω I <sub>D</sub> ≅ - 4.8 A, V <sub>GEN</sub> = - 10 V, R <sub>g</sub> = 6 Ω		23	40	ns
Rise Time	t <sub>r</sub>			49	75	
Turn-Off Delay Time	t <sub>d(off)</sub>			110	180	
Fall Time	t <sub>f</sub>			66	100	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = - 2.9 A, di/dt = 100 A/μs		75	120	

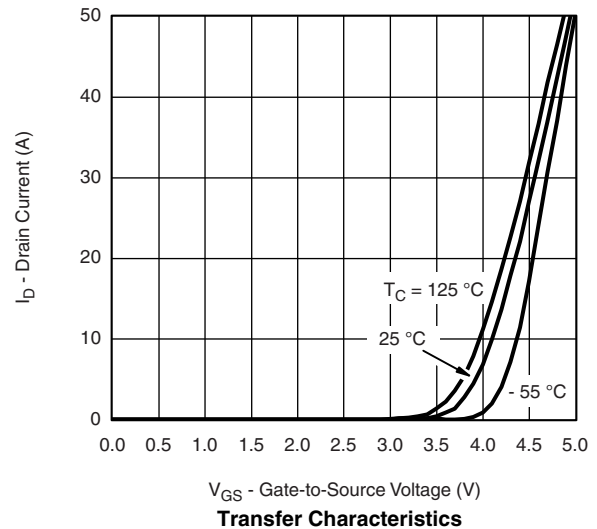
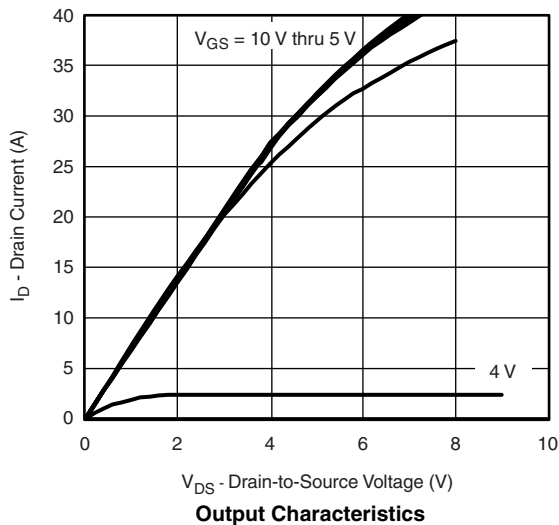
Notes:

a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.

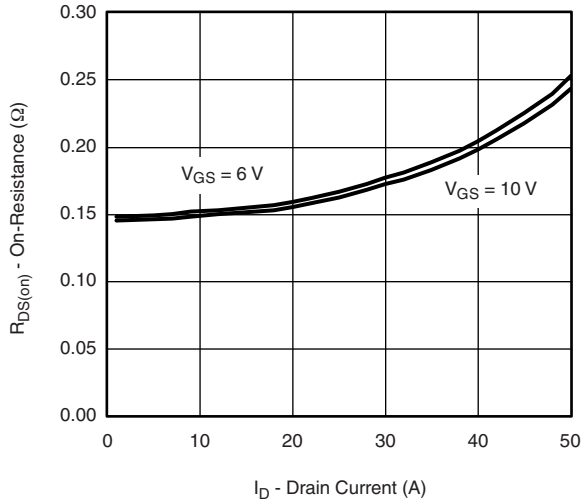
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

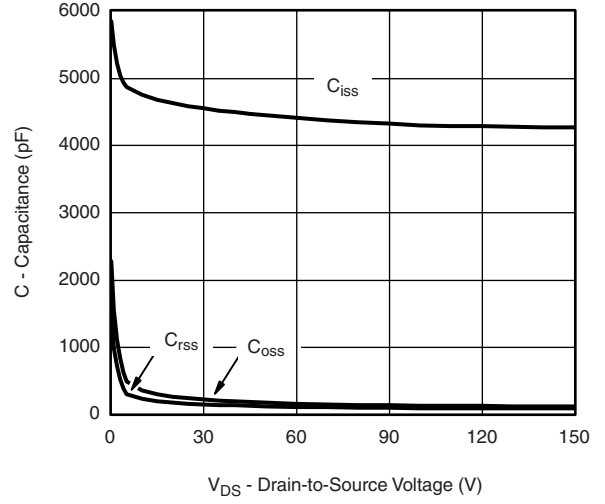
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



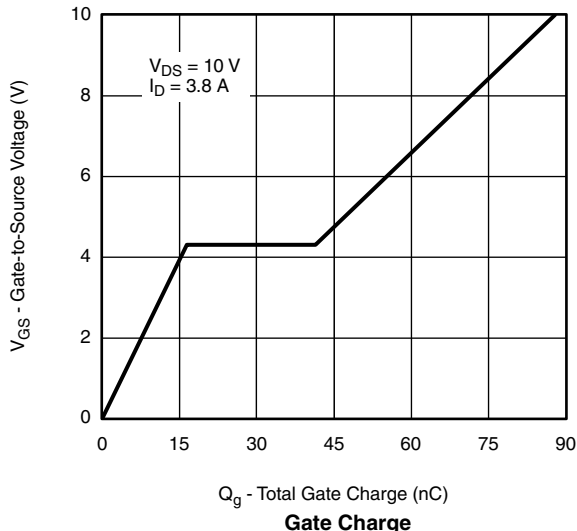
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



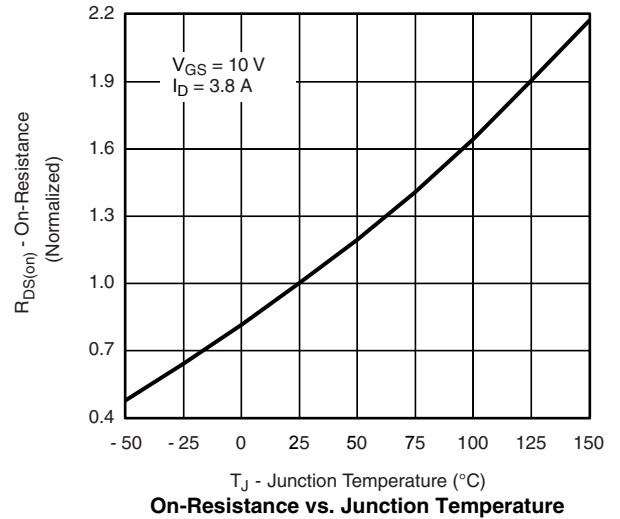
**On-Resistance vs. Drain Current**



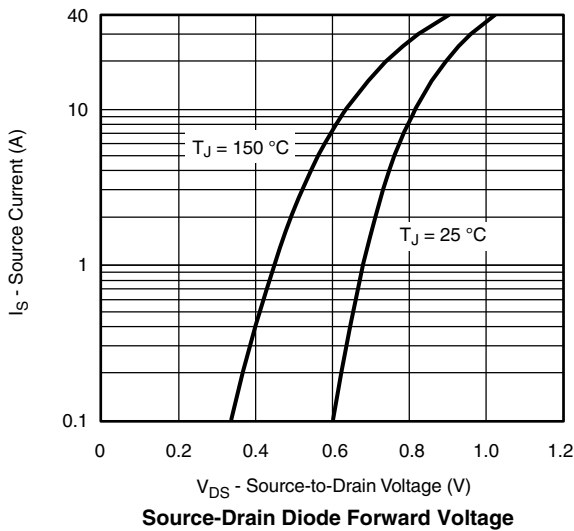
**Capacitance**



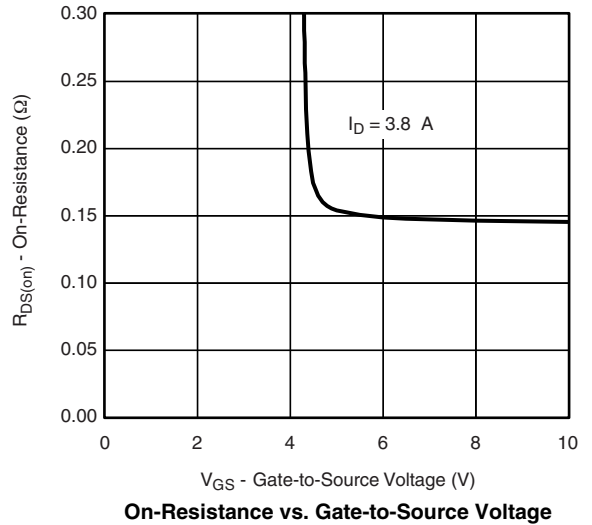
**Gate Charge**



**On-Resistance vs. Junction Temperature**

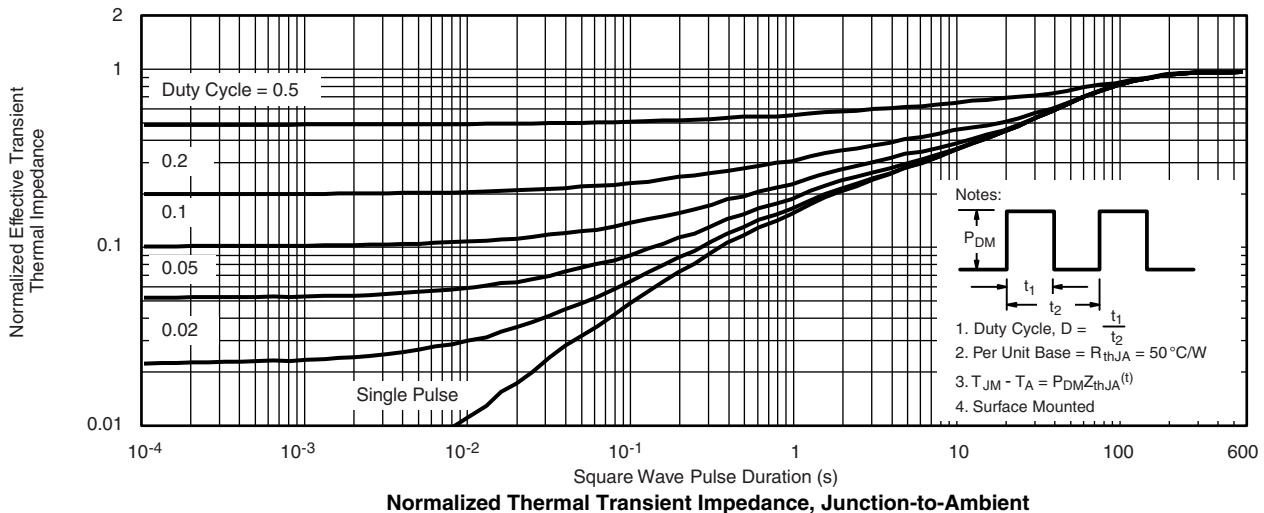
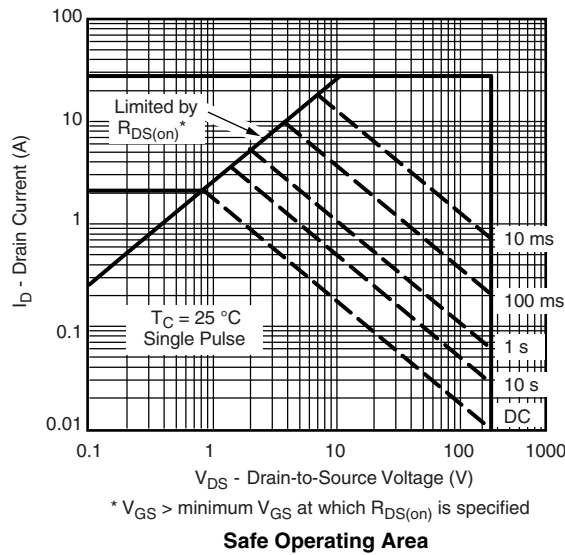
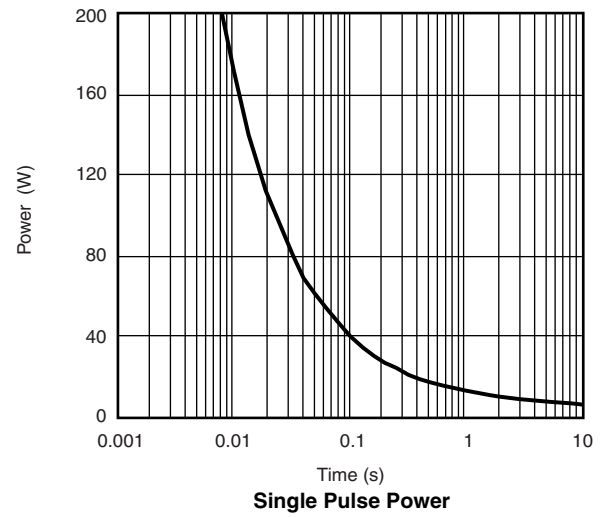
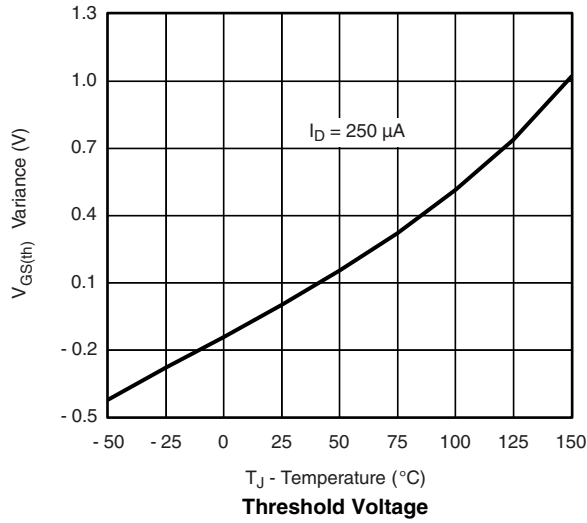


**Source-Drain Diode Forward Voltage**

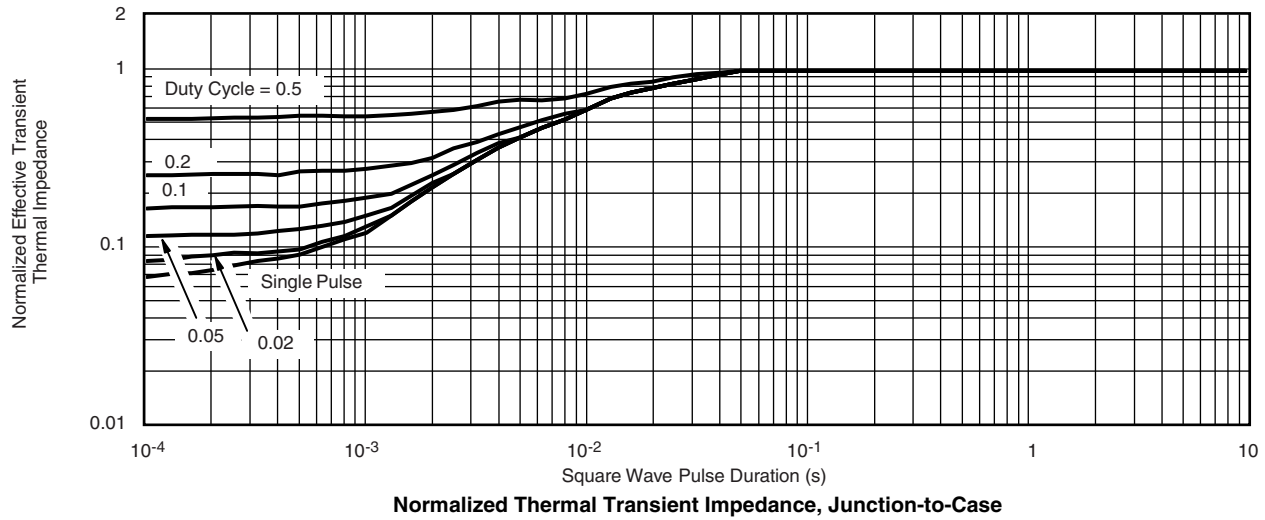


**On-Resistance vs. Gate-to-Source Voltage**

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



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