Ordering number : EN5588

CMOS LSI

LC75373E

Electronic Volume Control for Car Stereo Systems

Overview

The LC75373E is an electronic volume control that can implement volume, balance, fader, bass/treble + super bass, loudness, input switching, and input/output level control functions with a minimal number of external components.

Functions

- Volume: Provides 81 positions, from 0 dB to –79 dB (in 1-dB steps) and –∞. A balance function can be implemented by controlling the left and right channels independently.
- Fader: This function can attenuate either the rear or the front outputs over 16 positions. (From 0 to –20 dB in 2-dB steps, from –20 to –25 dB in one 5-dB step, from –25 to –45 dB in 10-dB steps, –60 dB, and –∞.)
- Bass/treble: Forms an NF-type tone control circuit with the addition of external capacitors. The base and treble controls each have 15 positions.
- Input gain: The input signal can be amplified from 0 dB to +18.75 dB in 1.25 dB steps.
- Output gain: One of two output of 0 dB and + 6.5 dB can be selected for fader output.
- Input switch: The signal can be selected from one of four inputs for each of the left and right channels.
- Super bass: The position of super bass can be controlled in 11 steps.

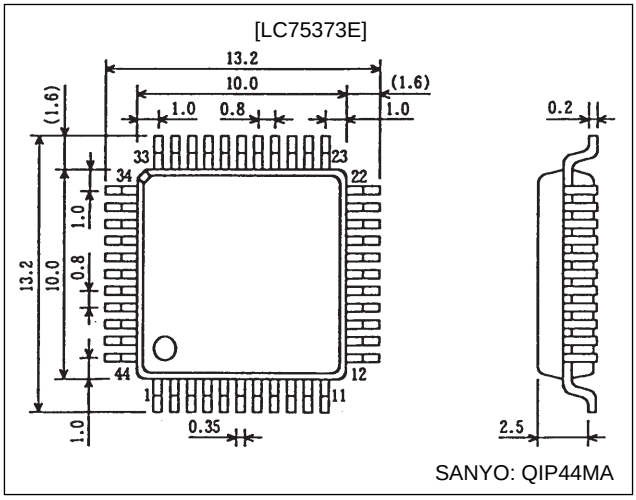
Features

- On-chip buffer amplifiers for a minimum of external components.
- Built-in reference voltage generation circuit
- Serial data input: Supports CCB format communication with the system controller.

Package Dimensions

unit: mm

3148-QFP44MA



- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	11	V
Maximum input voltage	V_{IN} max	CL, DI, CE	V_{SS} – 0.3 to V_{DD} + 0.3	V
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–50 to +125	°C

SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Allowable Operating Ranges at Ta = 25°C, V_{SS} = 0 V

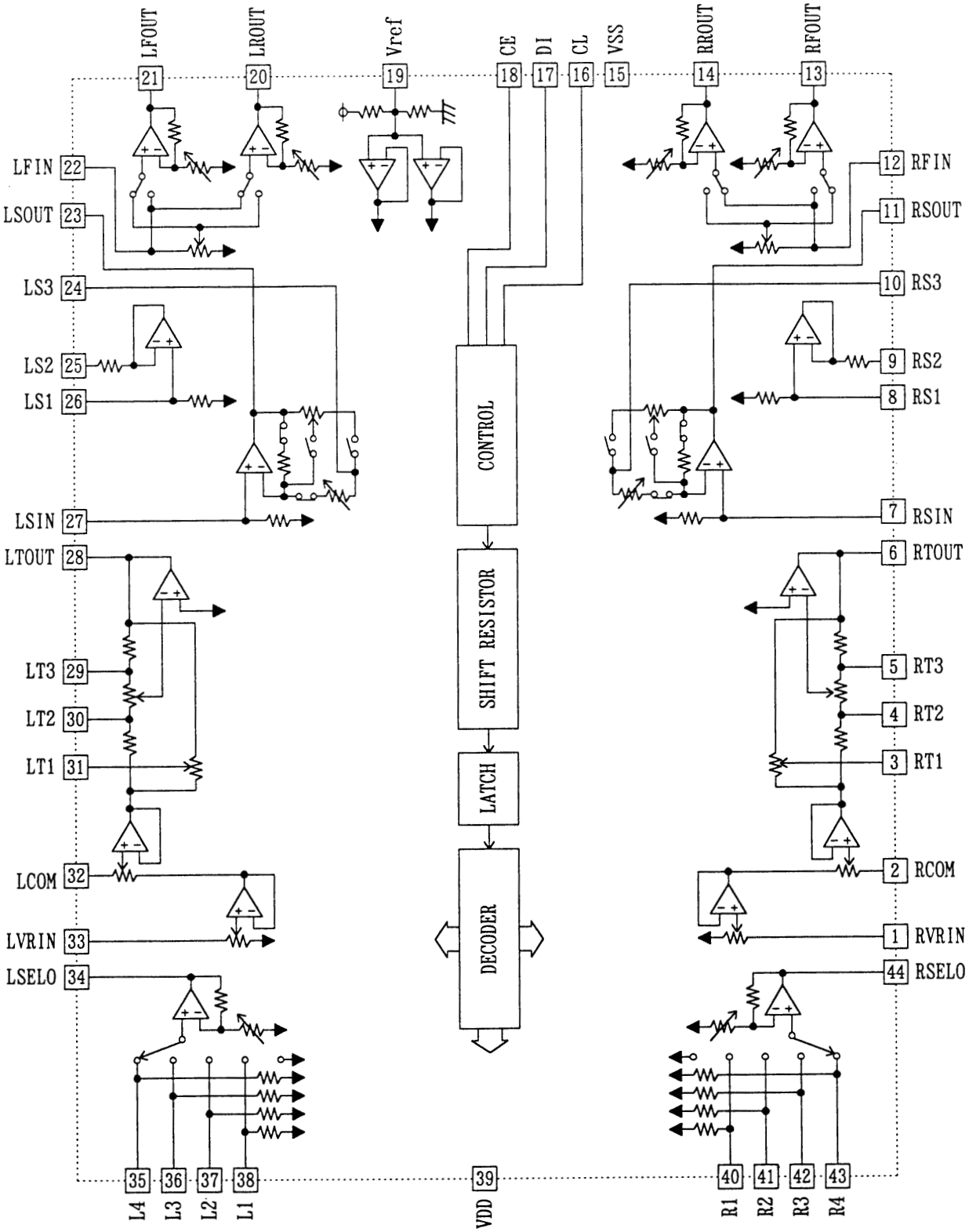
Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}	V_{DD}	6.0		10.5	V
Input high-level voltage	V_{IH}	CL, DI, CE	4.0		V_{DD}	V
Input low-level voltage	V_{IL}	CL, DI, CE	V_{SS}		1.0	V
Input voltage amplitude	V_{IN}	CL, DI, CE, LVRIN, RVRIN, L1 to L4, R1 to R4 LFIN, RFIN, LSIN, RSIN	V_{SS}		V_{DD}	Vp-p
Input pulse width	$t_{øW}$	CL	1			µs
Setup time	tsetup	CL, DI, CE	1			µs
Hold time	thold	CL, DI, CE	1			µs
Operating frequency	fopg	CL			500	kHz

Electrical Characteristics at Ta = 25°C, V_{DD} = 8 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
[Input Block]						
Maximum input gain	Gin max			+18.75		dB
Step resolution	Gstep			+1.25		dB
[Output Block]						
Maximum output gain	Gout max			+6.5		dB
[Volume Control Block]						
Step resolution	ATstep			1		dB
Step error	ATerr	step = 0 to –20 dB step = –20 to –50 dB	–1 –3	0 0	+1 +3	dB dB
[Fader Volume Block]						
Step resolution	ATstep	step =0 to –20 dB step = –20 to –25 dB step = –25 to –45 dB		2 5 10		dB
Step error	ATerr	step = 0 to –45 dB step = –45 to –60 dB	–2 –3	0 0	+2 +3	dB dB
Output load resistance	R_L		10			kΩ
[Bass/Treble Control Block]						
Bass control range	Gbass	Max. boost/cut	±9	±10.5	±12	dB
Treble control range	Gtre	Max. boost/cut	±8	±10.5	±13	dB
[Super Bass Block 1 (Type GEQ)]						
Control range	Crange	Max. boost		+17		dB
Step resolution	ATstep			+1.7		dB
[Super Bass Block 2 (Type T)]						
Control range	Crange	Max. boost		+20		dB
Step resolution	ATstep			+2.0		dB
[Overall Characteristics]						
Total harmonic distortion	THD	V_{IN} = 1 Vrms, f = 1 kHz, all settings flat overall		0.003	0.01	%
Crosstalk	CT	V_{IN} = 1 Vrms, f = 1 kHz, all settings flat overall, Rg = 1 kΩ		80.5		dB
Output at maximum attenuation	V_O min	V_{IN} = 1 Vrms, f = 1 kHz, main volume at –∞		–80		dB
Output noise voltage	V_N1	All settings flat overall (IHF-A), Rg = 1 kΩ		8		µV
	V_N2	All settings flat overall (DIN-AUDIO), Rg = 1 kΩ		10		µV
Input high-level current	I_{IH}	CL, DI, CE: V_{IN} = 8 V			10	µA
Input low-level current	I_{IL}	CL, DI, CE: V_{IN} = 0 V	–10			µA

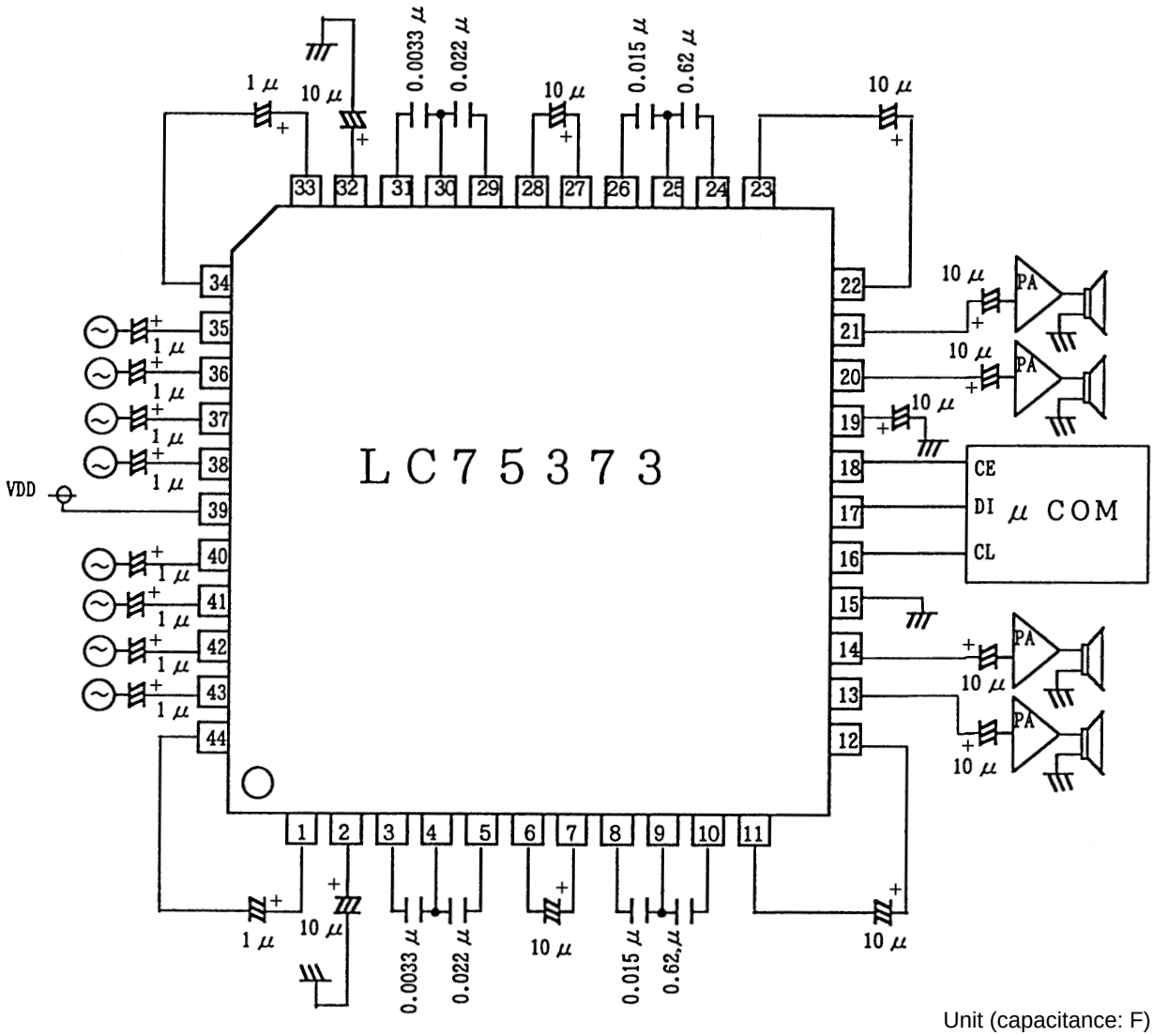
Note: Values in parenthesis are targets and will be fixed after evaluation.

Equivalent Circuit Block Diagram



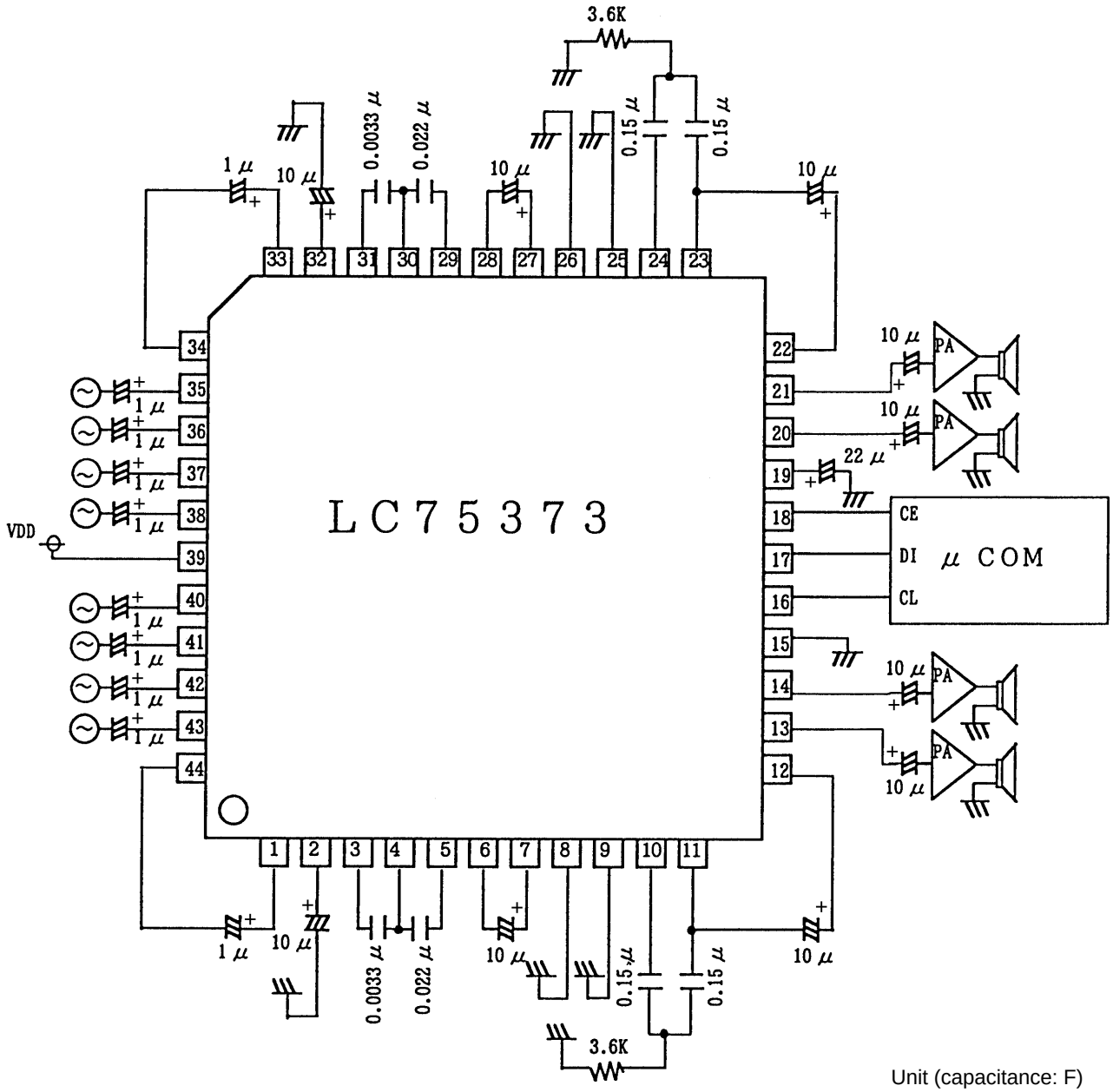
Sample Application Circuit

1. When super bass circuit 1 (Type GEQ) is used



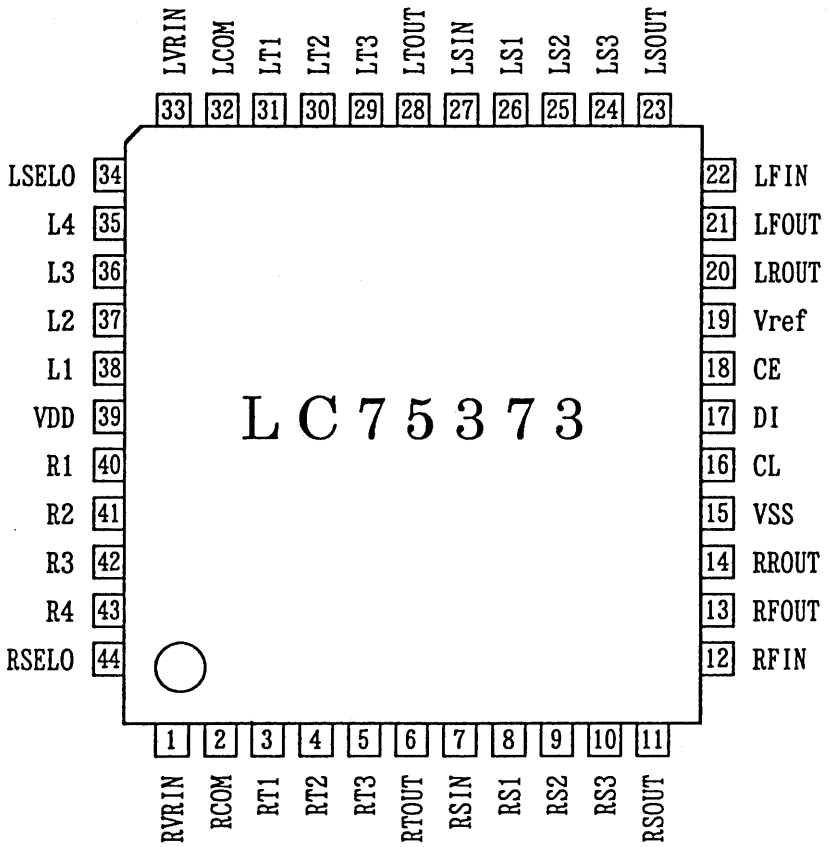
Unit (capacitance: F)

2. When super bass circuit 2 (Type T) is used



Unit (capacitance: F)
Unit (resistance: Ω)

Pin Assignment



Top view

Pin Functions

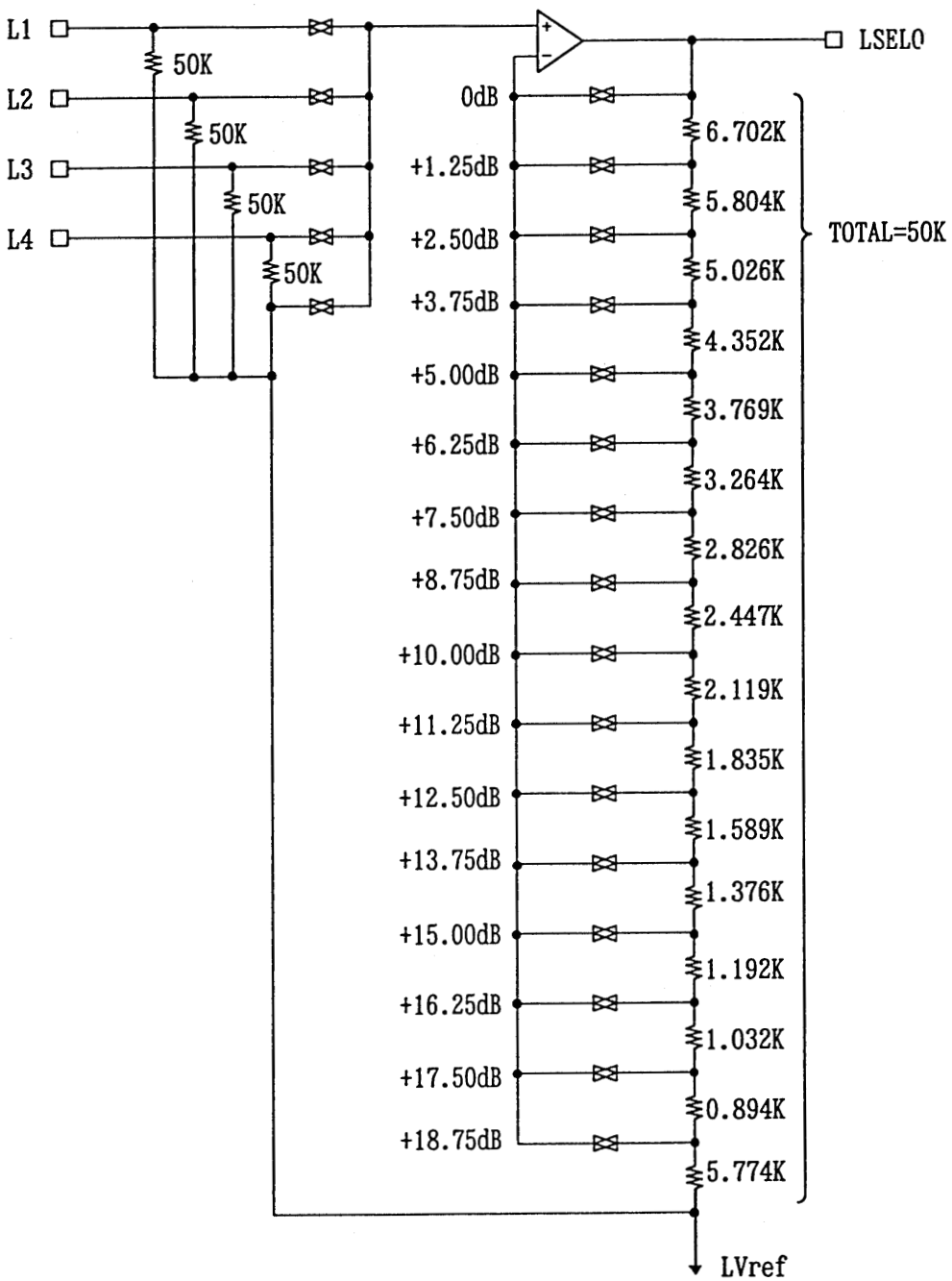
Pin No.	Symbol	Function	Note
19	Vref	• 1/2 V_{DD} voltage generation block. A capacitor must be connected between Vref and V_{SS} to suppress power supply ripple.	
20 21 14 13	LROUT LFOUT RROUT RFOUT	• Fader outputs. The front and rear systems can be attenuated independently.	
22 12	LFIN RFIN	• Fader inputs • Must be driven from low-impedance circuits.	
28 6	LTOUT RTOUT	• Tone control outputs	
31 30 29 3 4 5	LT1 LT2 LT3 RT1 RT2 RT3	• Connections for the bass and treble compensation capacitors for the tone control circuit Connect high-band compensation capacitors between T1 and T2. Connect low-band compensation capacitors between T2 and T3.	
26 25 24 8 9 10	LS1 LS2 LS3 RS1 RS2 RS3	• Super bass compensation capacitors	
33 1	LVRIN RVRIN	• 4-dB volume control inputs • These inputs must be driven from low-impedance circuits.	

Continued on next page.

Continued from preceding page.

Pin No.	Symbol	Function	Note
34 44	LSELO RSELO	• Outputs from the input selector	
38 37 36 35 40 41 42 43	L1 L2 L3 L4 R1 R2 R3 R4	• Signal inputs	
39	V_{DD}	Power supply connection	
15	V_{SS}	Ground	
18	CE	Chip enable. Data is latched internally at the point this pin goes from high to low. The analog switches operate at that point. Data transfer is enabled when this pin is high.	
16 17	CL DI	Inputs for the serial data and clock used for LSI control.	
32 2	LCOM RCOM	1-dB block common outputs	
27 7	LSIN RSIN	• Super bass inputs • These inputs must be driven by low-impedance circuits.	
11 23	RSOUT LSOUT	• Super bass outputs	

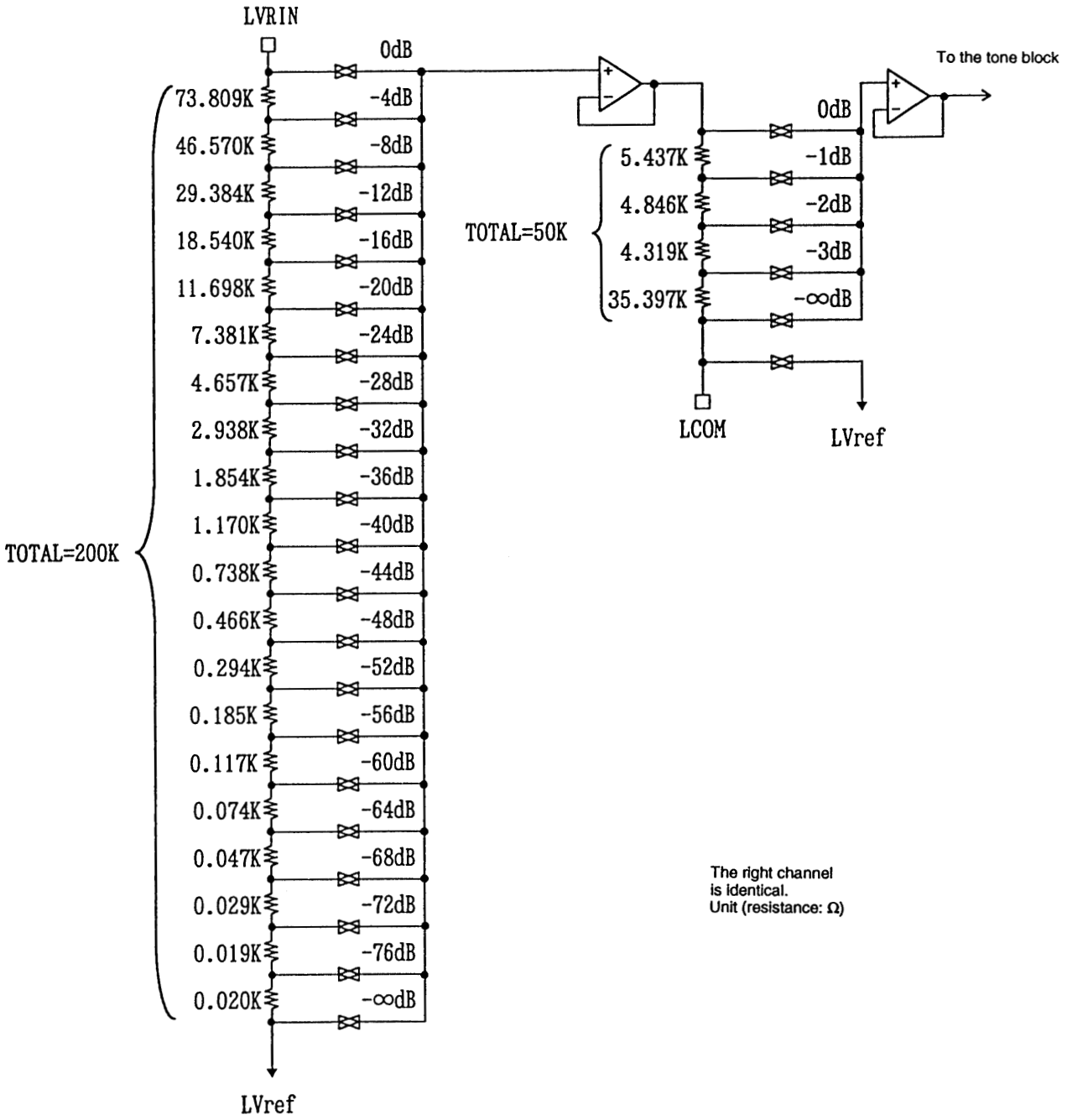
Input Block Equivalent Circuit



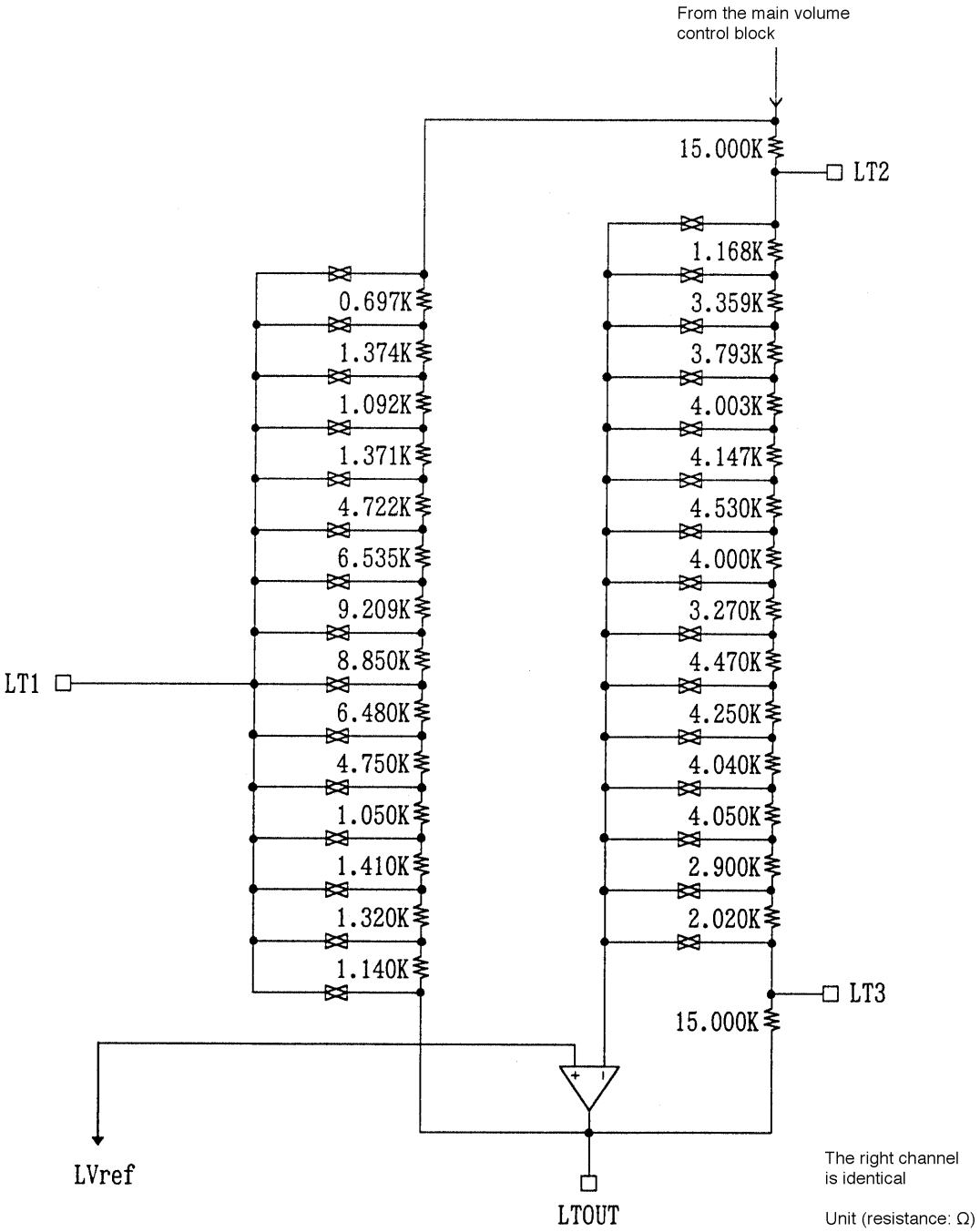
The right channel is identical.

Unit (resistance: Ω)

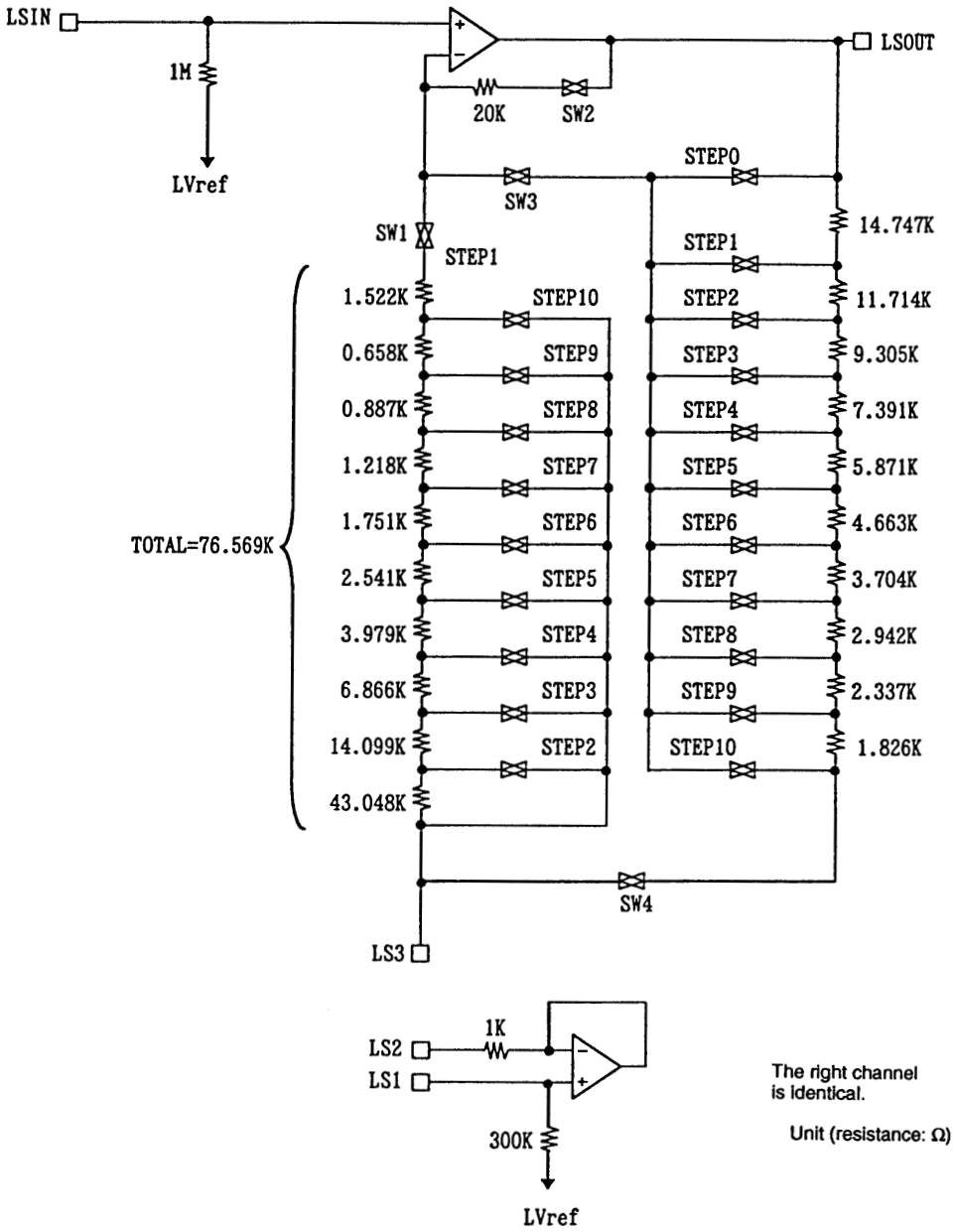
Main Volume Control Equivalent Circuit



Tone Control Block Equivalent Circuit



Super Bass Block Equivalent Circuit



Note: Concerning super bass switching control

• If the Q for super bass 1 (Type GEQ) is to be set to a relatively large value

SW1.....on (Note that this switch should be set to the off position only if STEP 0 data was sent.)

SW2.....on

SW3.....off

SW4.....off

• If the Q for super bass 2 (Type T) can be set to a relatively small value without problem

SW1.....off

SW2.....off

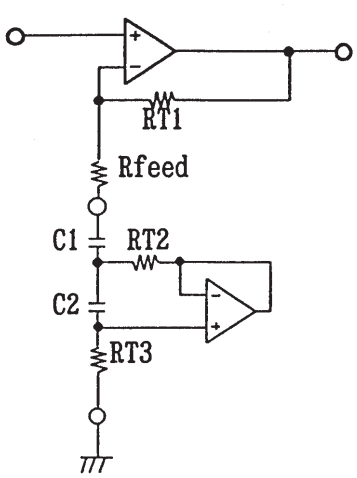
SW3.....on

SW4.....on

Super Bass Block Circuit 1 External Capacitor Calculation Example

The LC75373E external capacitors function as the structural elements for simulated inductances. This section presents the equivalent circuits and the formulas used to calculate the desired center frequencies.

Simulated Inductance Equivalent Circuit



Sample Calculations

Specifications: Center frequency: F0 = 100 Hz
Q at maximum boost: Qmax = 1.05

① Determine the sharpness Q0 of the simulated inductance itself.

$$Q0 = \frac{(RT2 + Rfeed)}{RT2} * Qmax \approx 2.6481$$

②Determine C1.

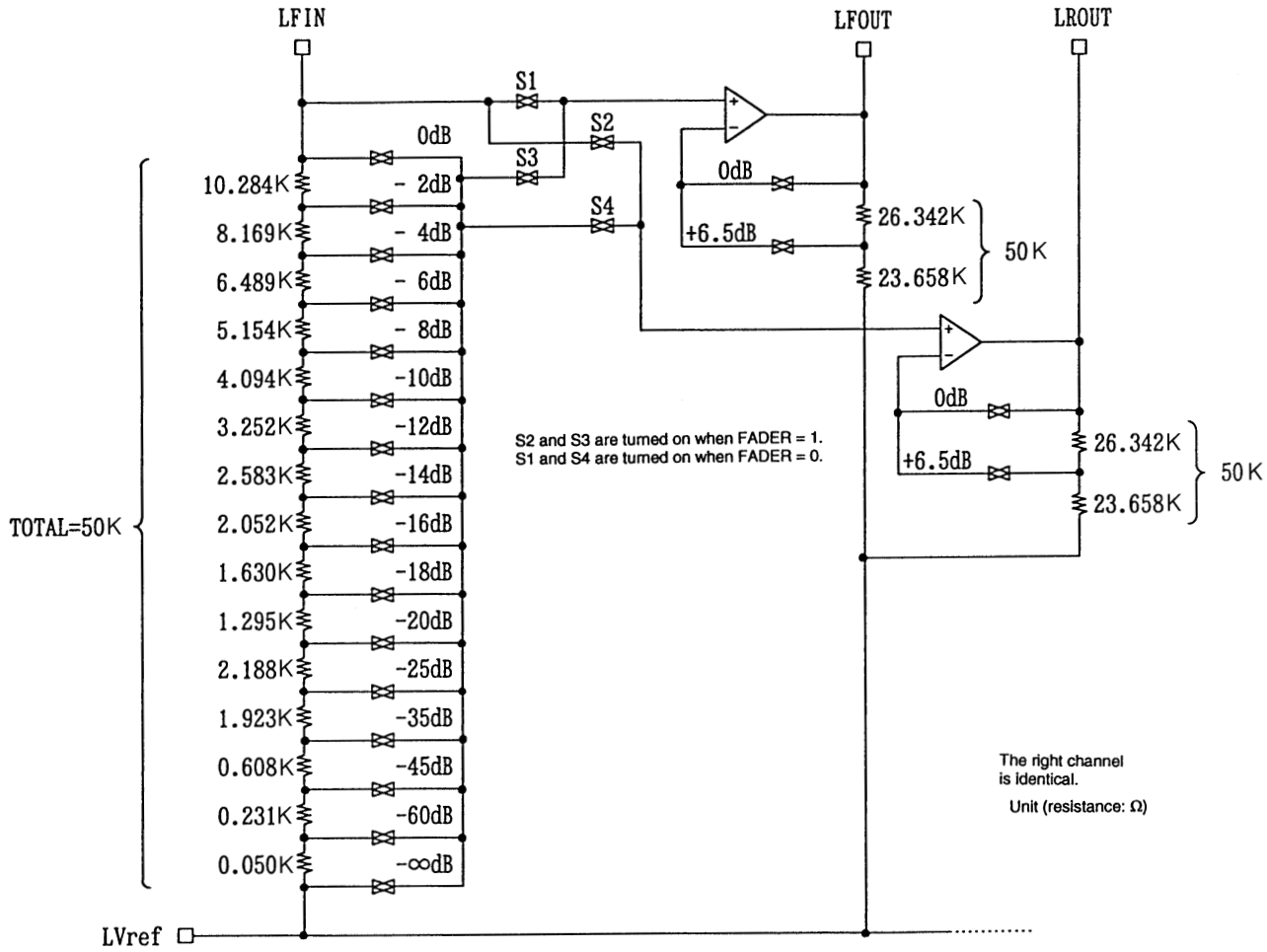
$$C1 = \frac{1}{2 * \pi * F0 * RT2 * Q0} \approx 0.60\ (\mu F)$$

③ Determine C2

$$C2 = \frac{Q0}{2 * \pi * F0 * RT3} \approx 0.014\ (\mu F)$$

*: See the super bass block equivalent circuit diagram for the values of the internal resistors.

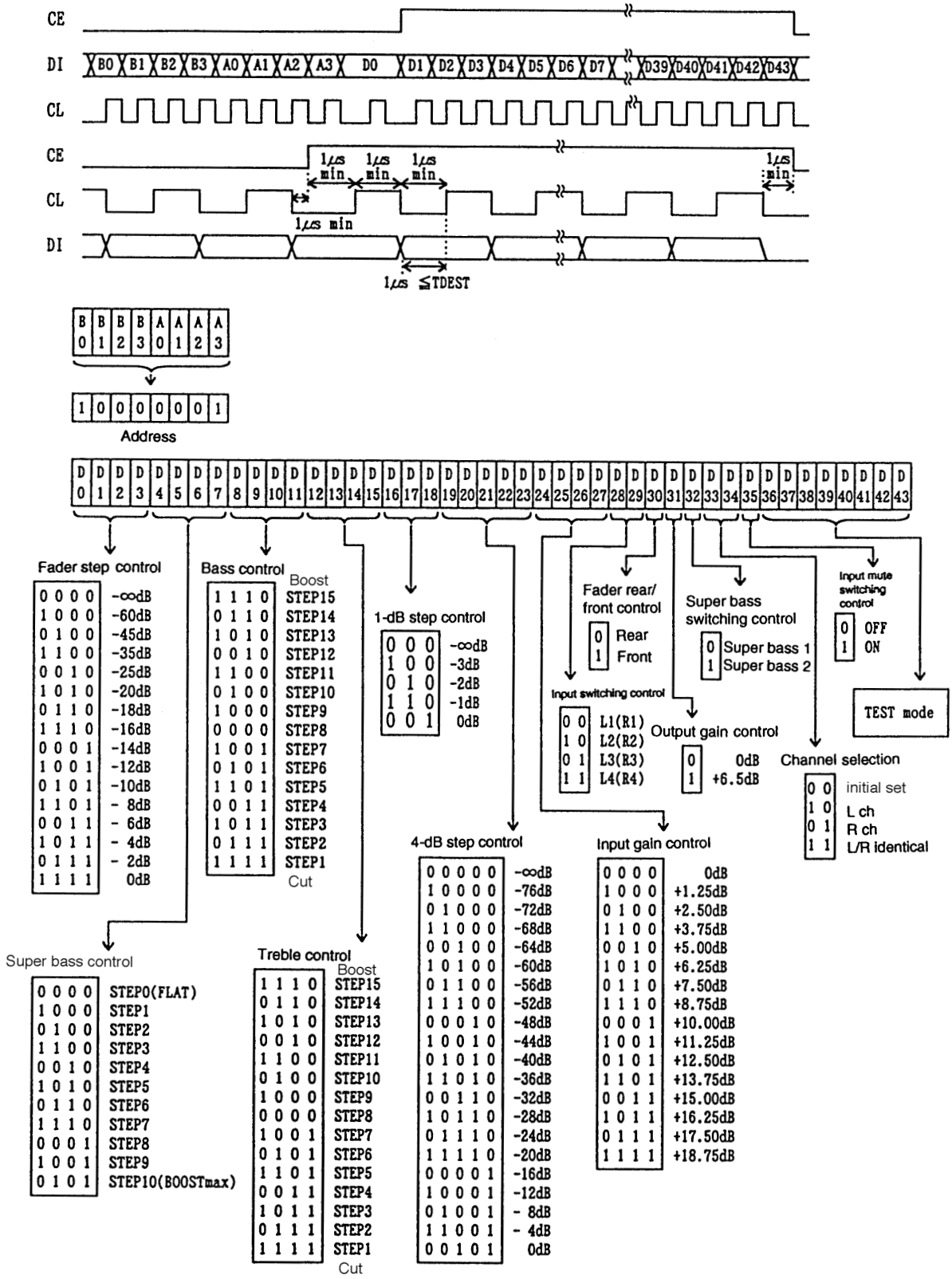
Fader Volume Control Block Equivalent Circuit



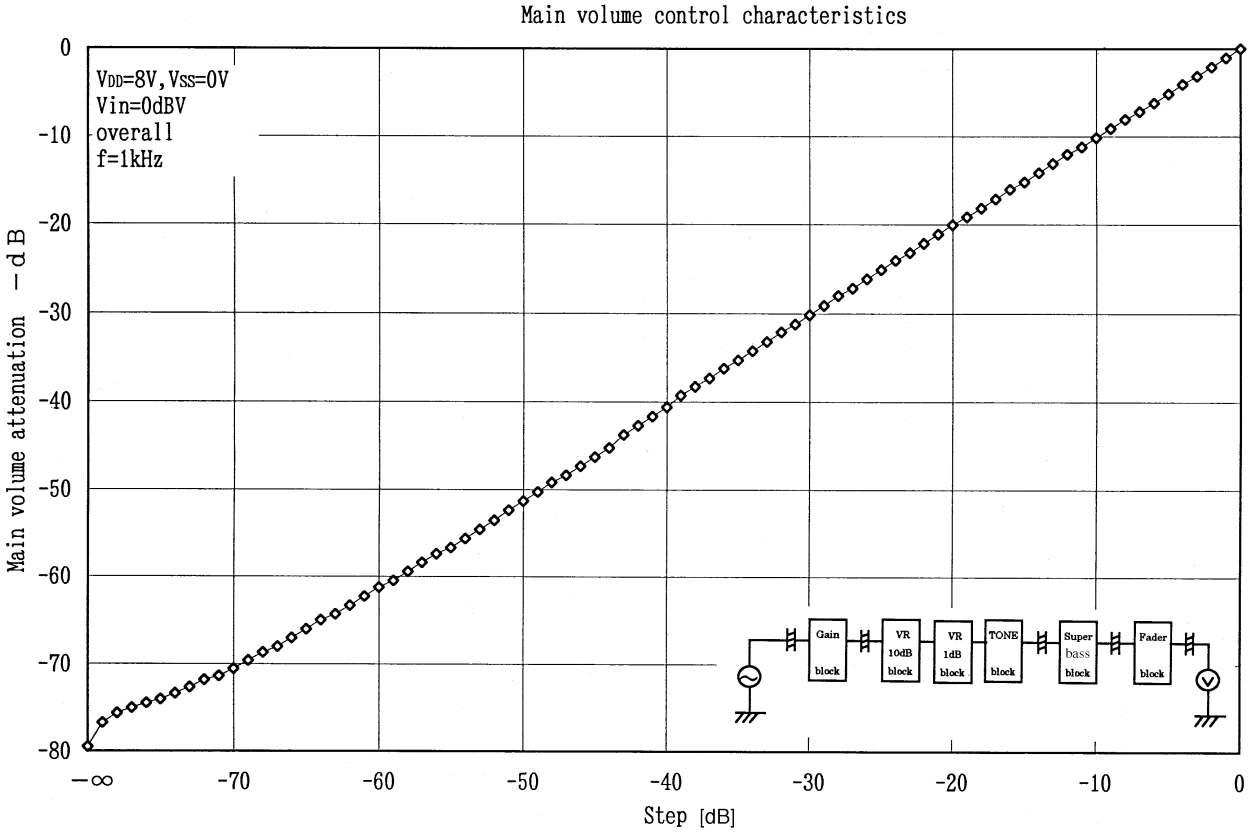
When data indicating an gain of —∞ is sent to the main volume control 1-dB step function, S1 and S2 open, and S3 and S4 go on at the same time.

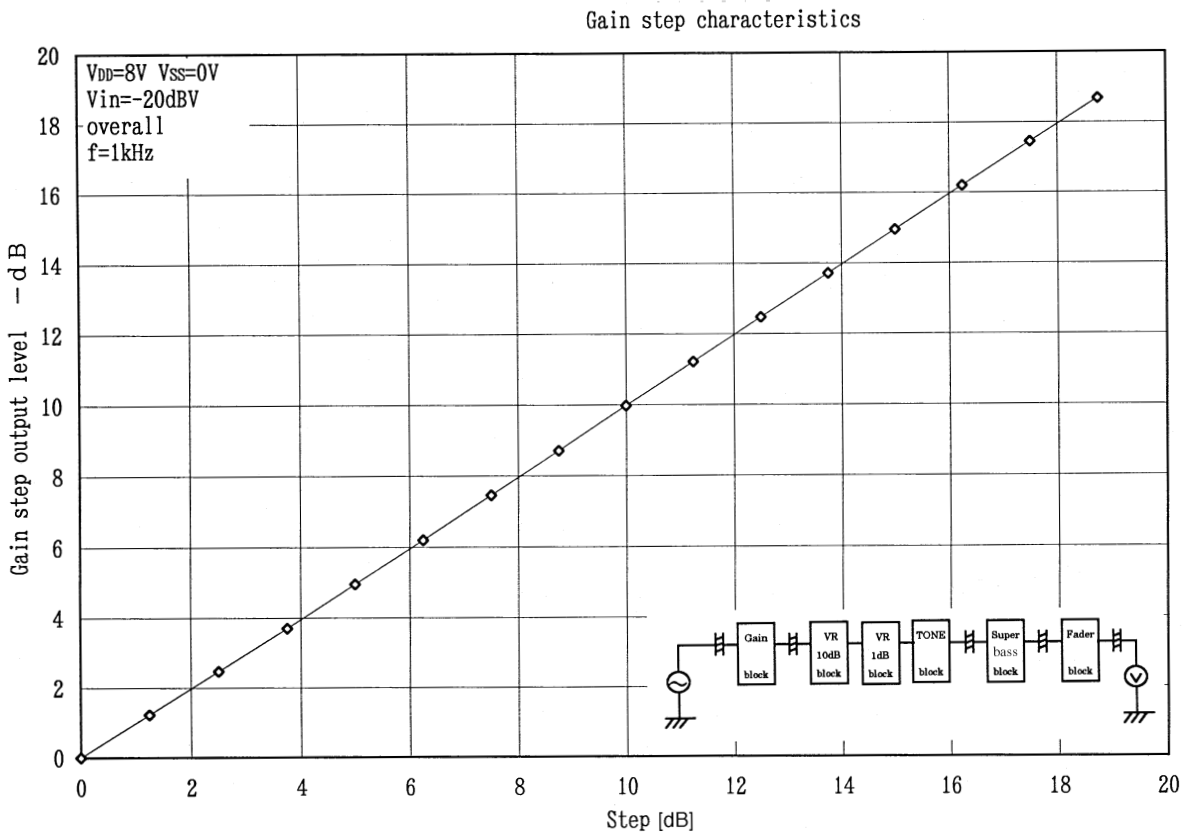
Control System Timing and Data Format

The LC75373E is controlled by applying serial data in the stipulated format to the CE, CL, and DI pins. The data consists of 52 bits, of which 8 bits are the chip address and 44 bits are the data.

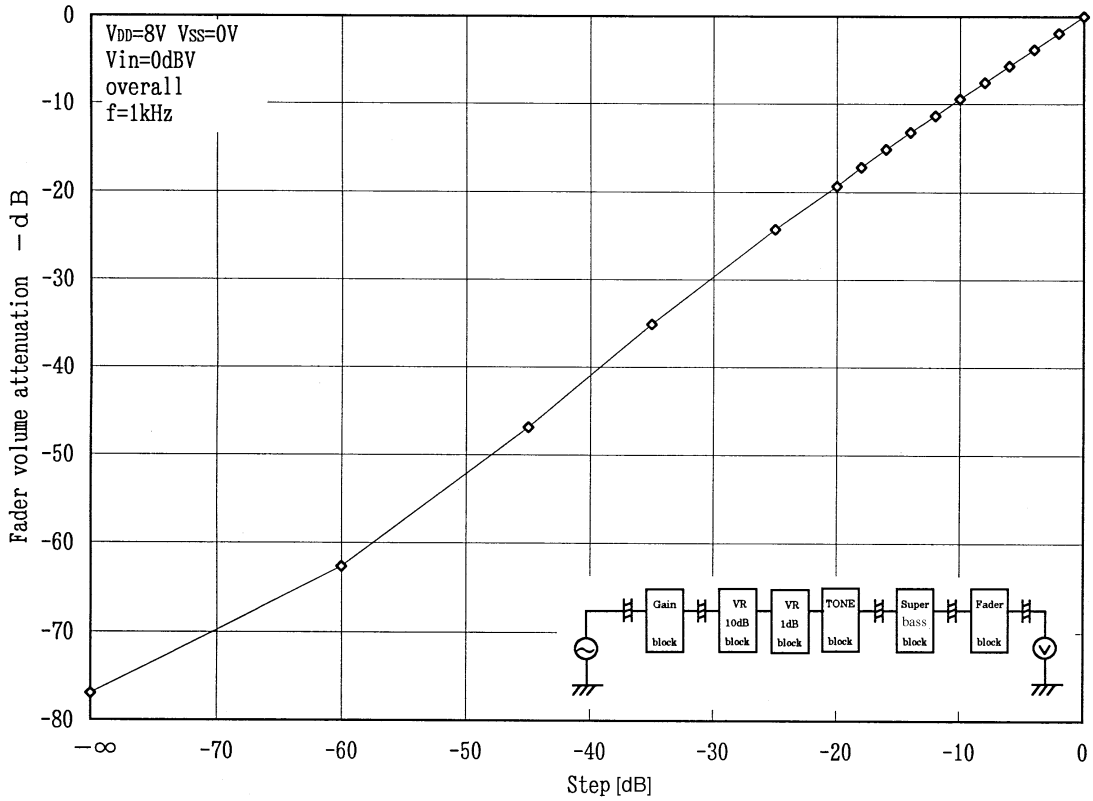


Note: 1. The bits D36 to D43 are LSI test bits and must be set to 0.
2. Concerning super bass switching
If the Q for super bass 1 is to be set to a relatively large value
If the Q for super bass 2 can be set to a relatively small value without problem

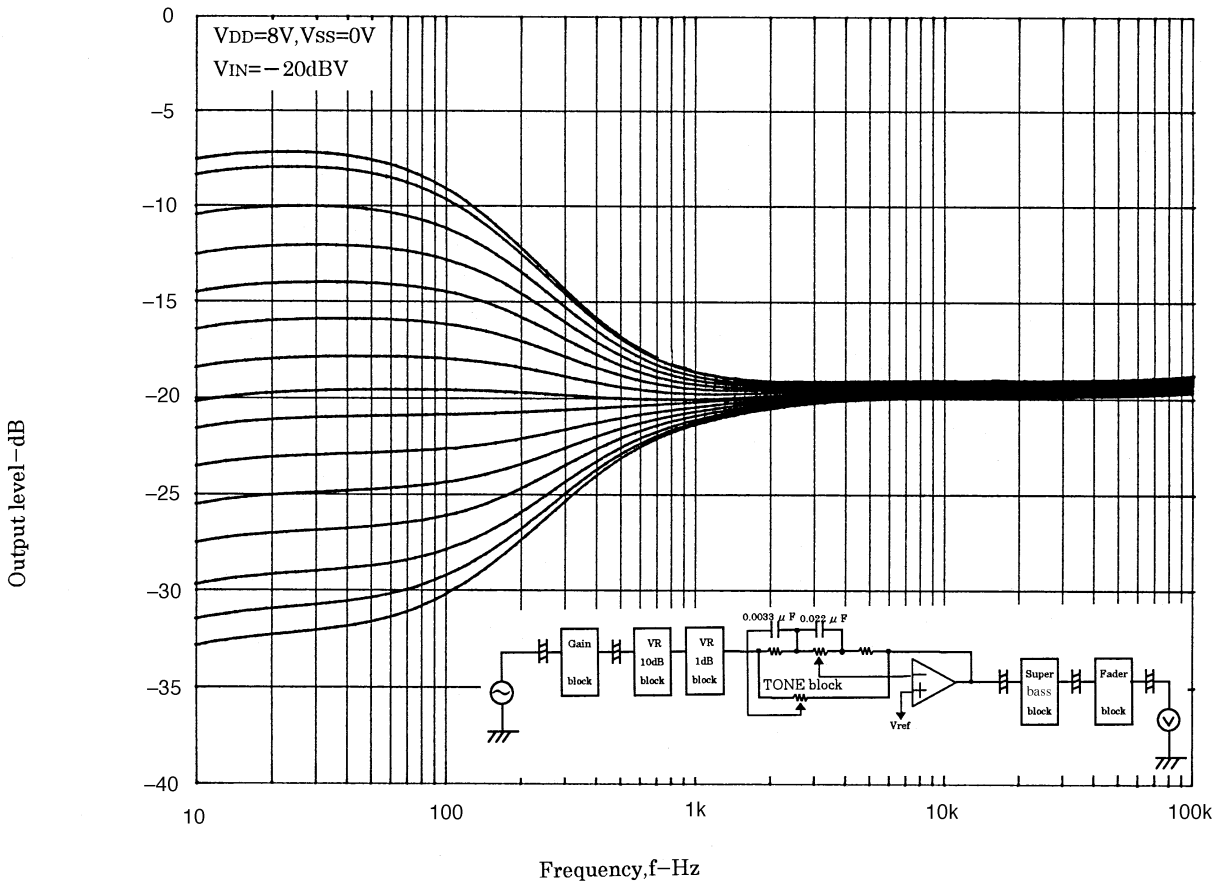

Main volume control characteristics
VDD=8V,VSS=0V
Vin=0dBV
overall
f=1kHz
Main volume attenuation – dB
0
-10
-20
-30
-40
-50
-60
-70
-80
–∞
-70
-60
-50
-40
-30
-20
-10
0
Step [dB]
Gain block
VR 10dB block
VR 1dB block
TONE block
Super bass block
Fader block


Gain step characteristics
VDD=8V VSS=0V
Vin=-20dBV
overall
f=1kHz
Gain step output level – dB
20
18
16
14
12
10
8
6
4
2
0
0
2
4
6
8
10
12
14
16
18
20
Step [dB]
Gain block
VR 10dB block
VR 1dB block
TONE block
Super bass block
Fader block

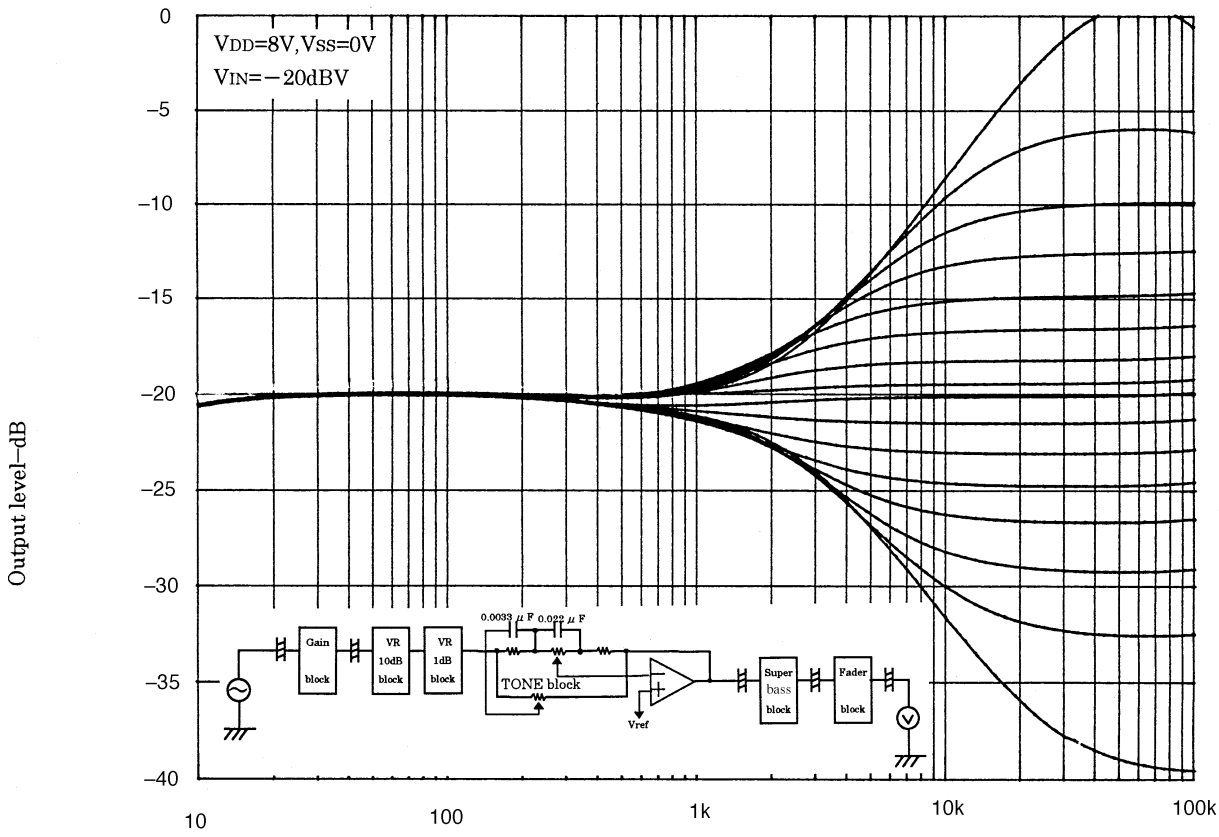
Fader volume control step characteristics



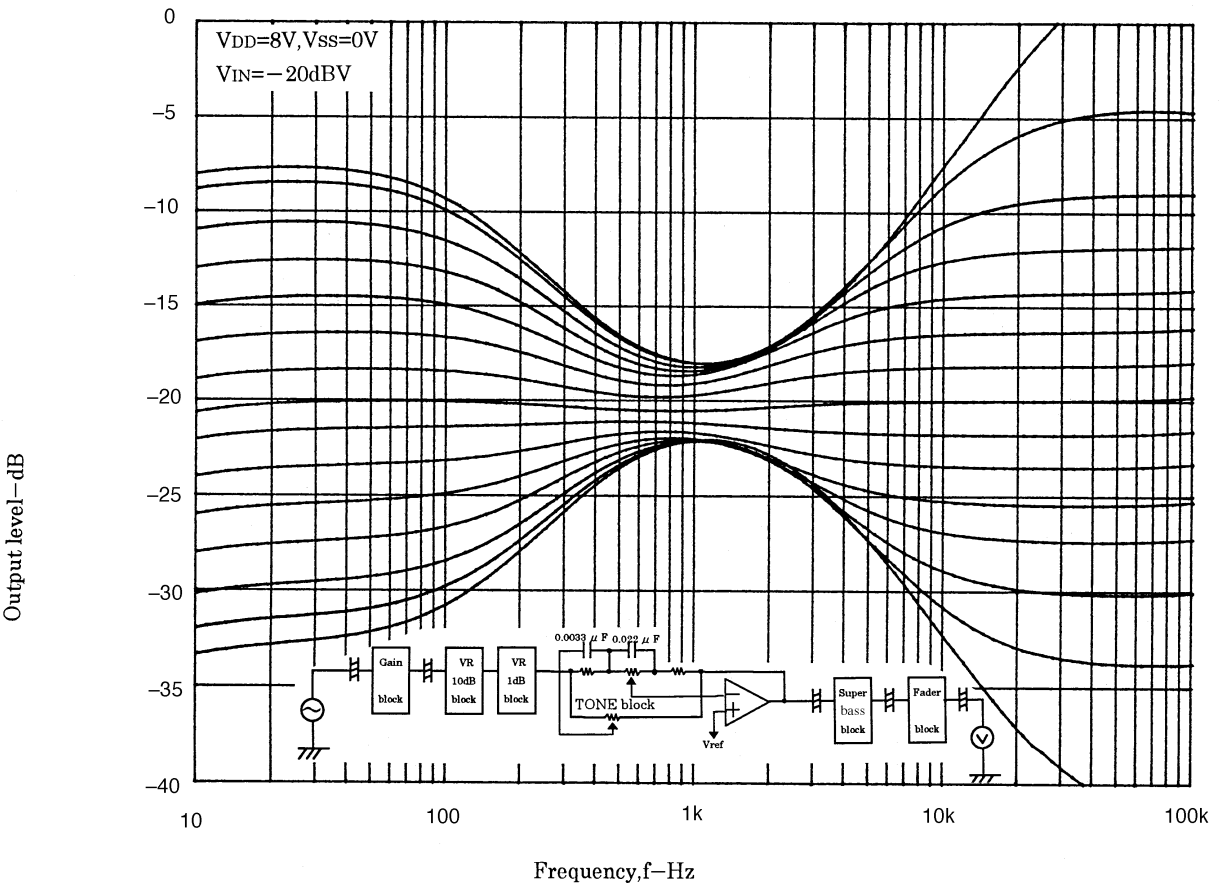
Bass control characteristics



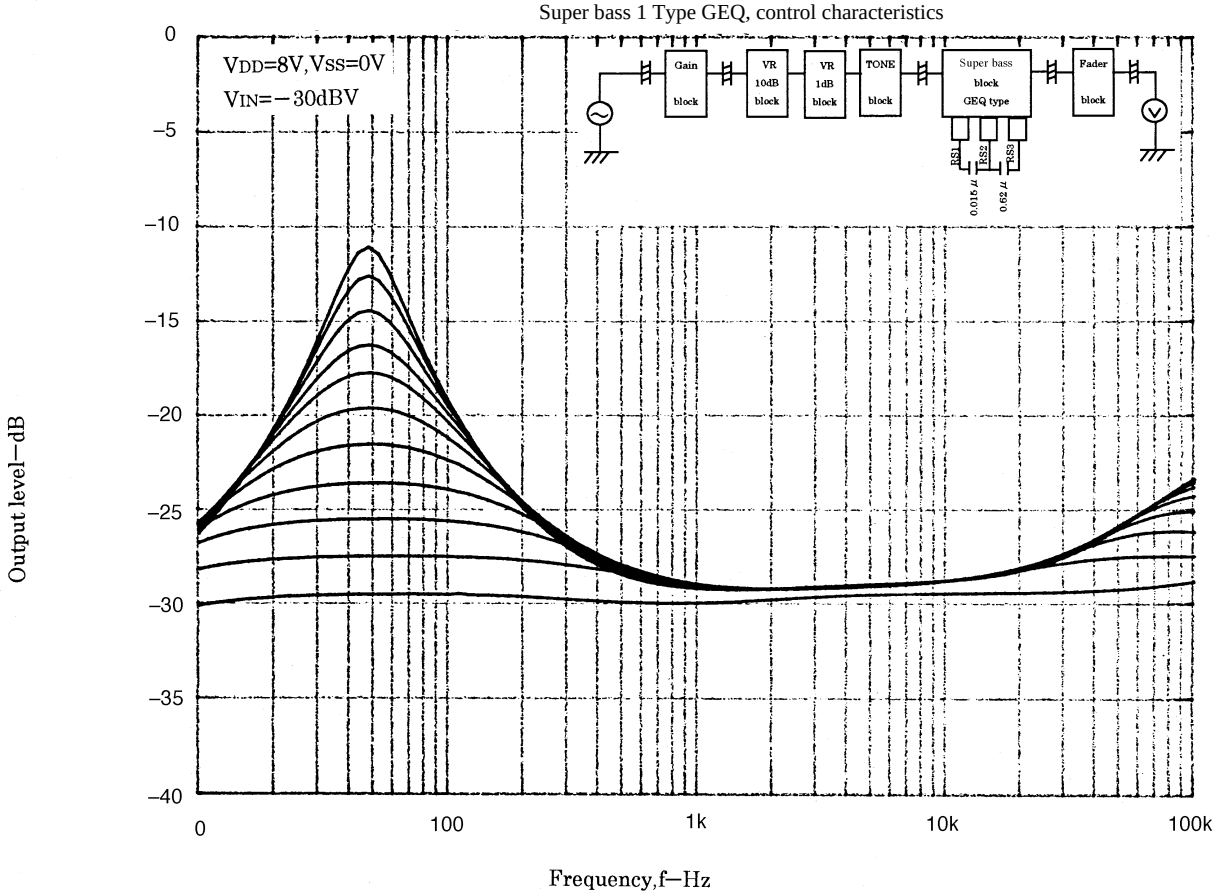
Treble control characteristics



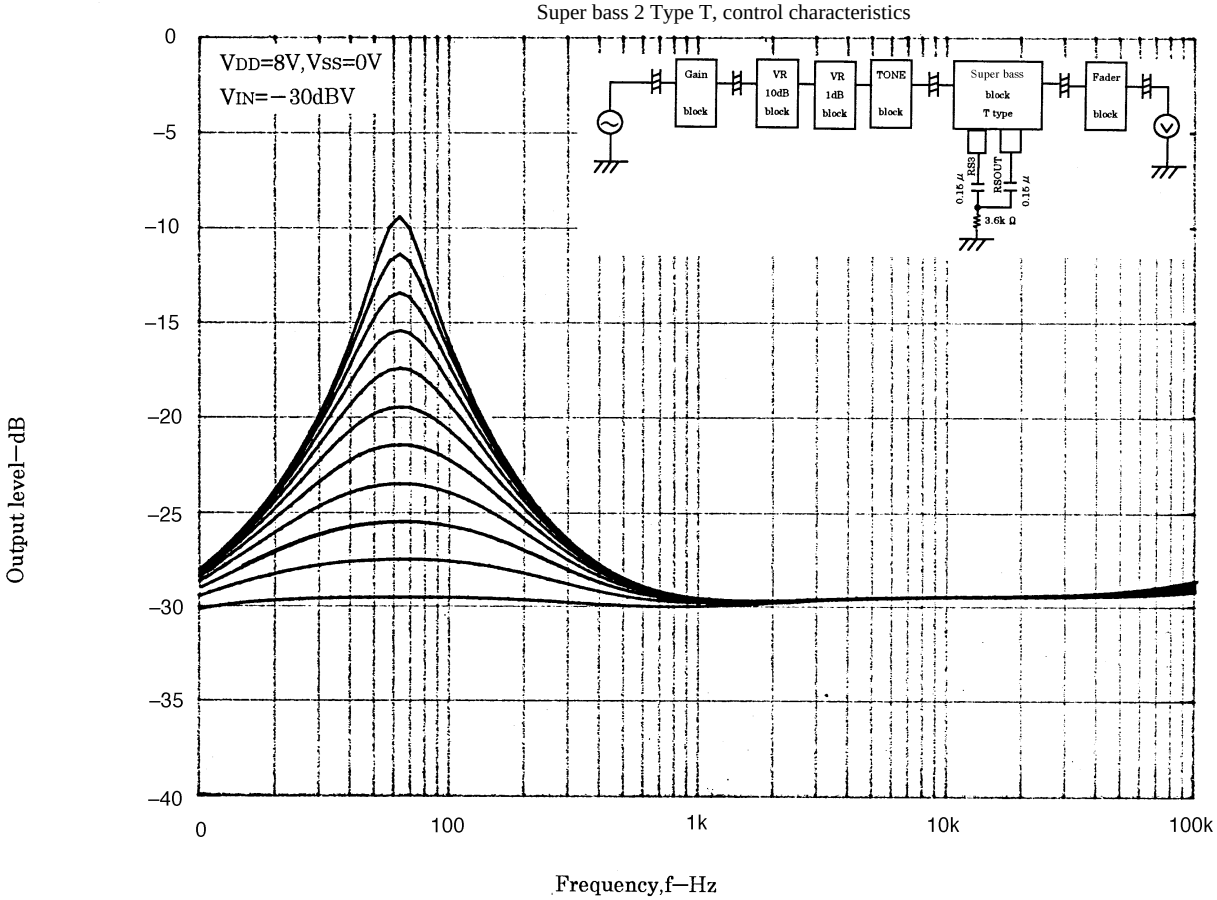
Tone control characteristics



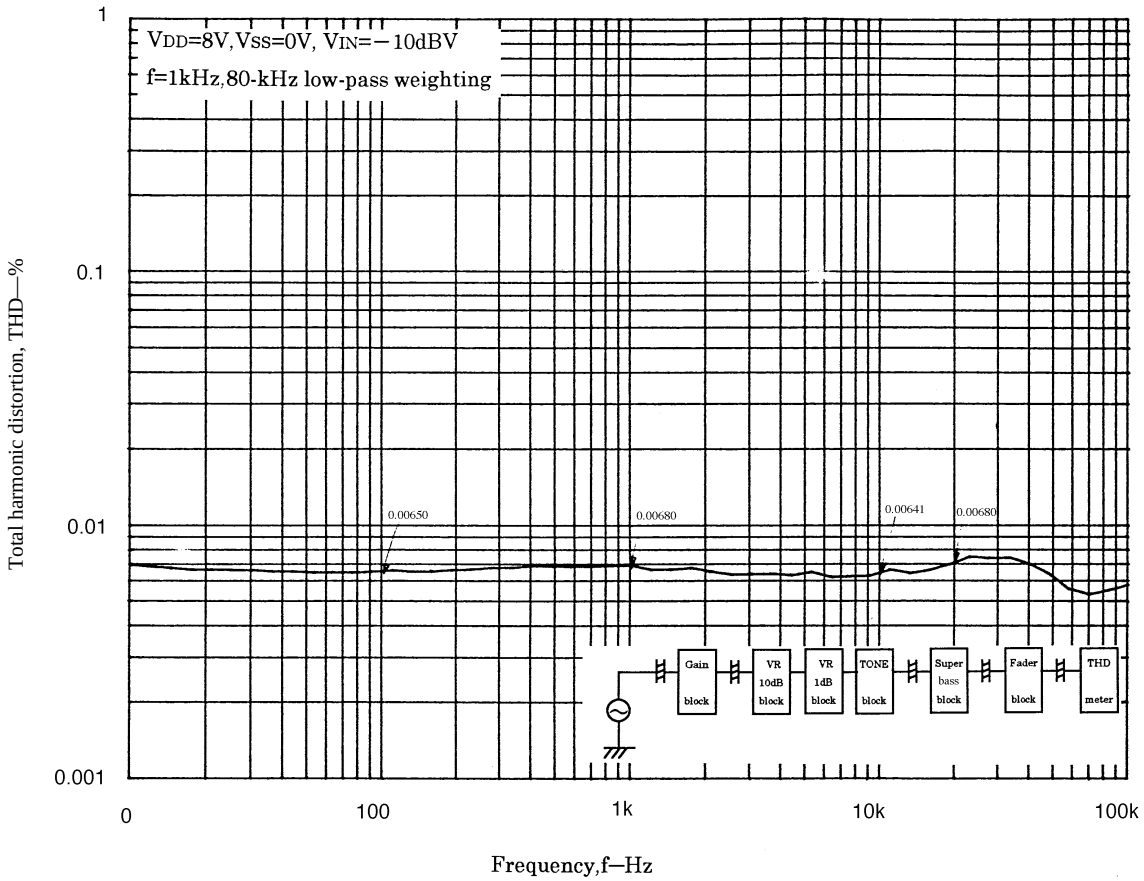
Super bass 1 Type GEQ, control characteristics



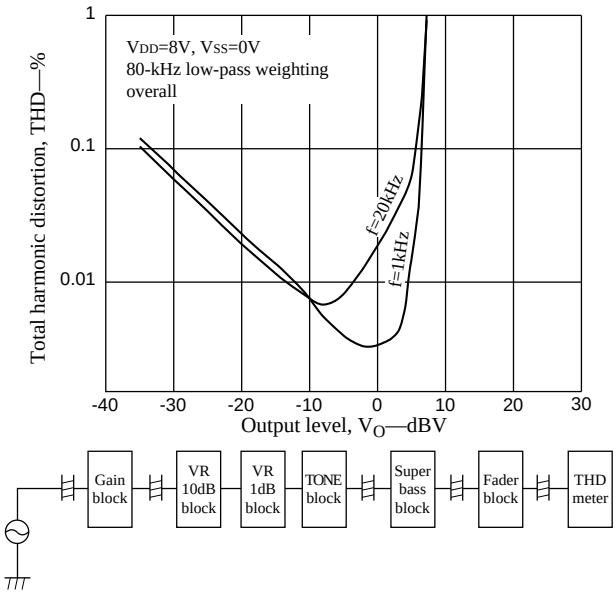
Super bass 2 Type T, control characteristics



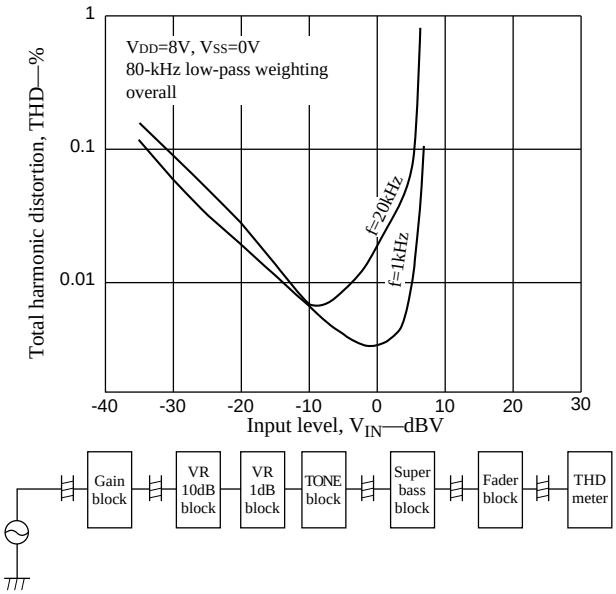
THD—Frequency characteristics



THD—Output level characteristics



THD—Input level characteristics



Usage Notes

1. The states of the internal analog switches are undefined when power is first applied. Use an external muting circuit or other technique to mute the outputs until correct control data has been set up in the LC75373E.
2. Either cover the lines connected to the CL, DI, and CE pins with the ground pattern or use shielded cable for those lines to prevent the high-frequency digital signals on those lines from entering the analog system.