Quad Supply Voltage Supervisors with Programmable Delay and Watchdog Timer

Check for Samples: TPS386000-Q1

FEATURES

- **Qualified for Automotive Applications**
- **4 Complete SVS Modules on 1 Silicon Platform**
- **Programmable Delay Time: 1.4ms to 10s**
- **Very Low Quiescent Current: 12μA typ**
- **Threshold Accuracy: 0.25% typ**
- **SVS-1: Manual Reset ($\overline{\text{MR}}$) Input**
- **SVS-1,2,3: Adjustable Threshold Down to 0.4V**
- **SVS-4: Adjustable Threshold at Any Positive/Negative Voltage with VREF (1.2V)**
- **SVS-4: Window Comparator**
- **Watchdog Timer with Dedicated Output**
- **Well-Controlled $\overline{\text{RESETn}}$ Output During Power-Up**
- **Open-Drain $\overline{\text{RESETn}}$ and $\overline{\text{WDO}}$**
- **Package: 4mm x 4mm, 20-pin QFN**

DESCRIPTION

The TPS386000-Q1 family of voltage supervisors can monitor four power rails that are greater than 0.4V and one power rail less than 0.4V (including negative voltage) with a 0.25% (typical) threshold accuracy. Each of the four supervisory circuits (SVS-n) assert a $\overline{\text{RESETn}}$ or RESETn output signal when the SENSEm input voltage drops below the programmed threshold. With external resistors, the threshold of each SVS-n can be programmed (where *n* = 1, 2, 3, 4 and *m* = 1, 2, 3, 4L, 4H).

Each SVS-n has a programmable delay before releasing $\overline{\text{RESETn}}$ or RESETn, and the delay time can be set from 1.4ms to 10s through the CTn pin connection. Only SVS-1 has an active-low manual reset ($\overline{\text{MR}}$) input; a logic-low input to $\overline{\text{MR}}$ asserts $\overline{\text{RESET1}}$ or RESET1.

SVS-4 monitors the threshold window using two comparators. The extra comparator can be configured as a fifth SVS to monitor negative voltage with voltage reference output VREF.

The TPS386000-Q1 has a very low quiescent current of 12μA (typical) and is available in a small, 4mm x 4mm, QFN-20 package.

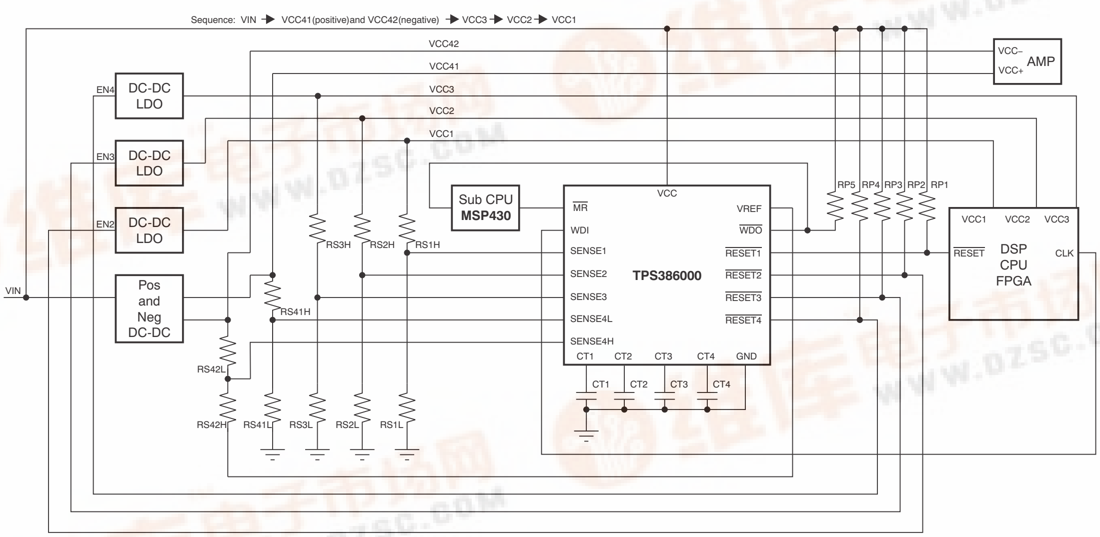


Figure 1. TPS386000-Q1 Typical Application Circuit

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	DESCRIPTION	PACKAGE-LEAD	PACKAGE DESIGNATOR(2)	TEMPERATURE RANGE	PACKAGE MARKING	TRANSPORT MEDIA, QUANTITY
TPS386000QRGPRQ1	Open-drain, active low	VQFN-20	RGP	–40°C to +125°C	TPS386000Q	Reel, 3000

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating junction temperature range, unless otherwise noted.

	TPS386000-Q1	UNIT
Input voltage range, V_{VCC}	–0.3 to 7.0	V
CT pin voltage range, V_{CT1}, V_{CT2}, V_{CT3}, V_{CT4}	–0.3 to V_{VCC} + 0.3	V
Other voltage ranges: V_{RESET1}, V_{RESET2}, V_{RESET3}, V_{RESET4}, V_{MR}, V_{SENSE1}, V_{SENSE2}, V_{SENSE3}, $V_{SENSE4L}$, $V_{SENSE4H}$, V_{WDI}, V_{WDO}	–0.3 to 7.0	V
$\overline{\text{RESETn}}$, RESETn, $\overline{\text{WDO}}$, WDO, VREF pin current	5	mA
Continuous total power dissipation	See *Thermal Information Table*	
Operating virtual junction temperature range, T_J (2)	–40 to +150	°C
Operating ambient temperature range	–40 to +125	°C
Storage temperature range, T_{STG}	–65 to +150	°C
Latch-up performance meets 100mA per AEC-Q100	Class I	

(1) Stresses beyond those listed under the *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the recommended operating conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS386000-Q1 RGP PACKAGE 20 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	50.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	1.5	
θ_{JB}	Junction-to-board thermal resistance	21.0	
ψ_{JT}	Junction-to-top characterization parameter	42.8	
ψ_{JB}	Junction-to-board characterization parameter	8.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	21.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

Over the operating temperature range of T_J = –40°C to +125°C, 1.8V < V_{VCC} < 6.5V, R_{RESETn} (*n* = 1, 2, 3, 4) = 100kΩ to V_{VCC}, C_{RESETn} (*n* = 1, 2, 3, 4L, 4H) = 50pF to GND, R_{WDO} = 100kΩ to V_{VCC}, C_{WDO} = 50pF to GND, V_{MR} = 100kΩ to V_{VCC}, WDI = GND, and CTn (*n* = 1, 2, 3, 4) = open, unless otherwise noted. Typical values are at T_J = +25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VCC}	Input supply range		1.8		6.5	V
I_{VCC}	Supply current (current into VCC pin)	V_{VCC} = 3.3V, $\overline{\text{RESETn}}$ or RESETn not asserted, WDI toggling[(1)], no output load, and VREF open		11	19	µA
		V_{VCC} = 6.5V, $\overline{\text{RESETn}}$ or RESETn not asserted, WDI toggling[(1)], no output load, and VREF open		13	22	µA
	Power-up reset voltage[(2)(3)]	V_{OL} (max) = 0.2V, I_{RESETn} = 15µA			0.9	V
V_{ITN}	Negative-going input threshold voltage	SENSE1, SENSE2, SENSE3, SENSE4L	396	400	404	mV
V_{ITP}	Positive-going input threshold voltage	SENSE4H	396	400	404	mV
V_{HYSN}	Hysteresis (positive-going) on V_{ITN}	SENSE1, SENSE2, SENSE3, SENSE4L		3.5	10	mV
V_{HYSP}	Hysteresis (negative-going) on V_{ITP}	SENSE4H		3.5	10	mV
I_{SENSE}	Input current at SENSEm pin	V_{SENSEm} = 0.42V	–25	±1	+25	nA
I_{CT}	CTn pin charging current: CT1	C_{CT1} > 220pF, V_{CT1} = 0.5V[(4)]	245	300	355	nA
	CTn pin charging current: CT2, CT3, CT4	C_{CTn} > 220pF, V_{CTn} = 0.5V[(4)]	235	300	365	nA
$V_{TH(CTn)}$	CTn pin threshold	C_{CTn} > 220pF	1.180	1.238	1.299	V
V_{IL}	$\overline{\text{MR}}$ and WDI logic low input		0		$0.3V_{VCC}$	V
V_{IH}	$\overline{\text{MR}}$ and WDI logic high input		$0.7V_{VCC}$			V
V_{OL}	Low-level $\overline{\text{RESETn}}$ or RESETn output voltage	I_{OL} = 1mA			0.4	V
		SENSEn = 0V, 1.3V < V_{VCC} < 1.8V, I_{OL} = 0.4mA[(2)]			0.3	V
	Low-level WDO output voltage	I_{OL} = 1mA			0.4	V
I_{LKG}	$\overline{\text{RESETn}}$, RESETn, $\overline{\text{WDO}}$, and WDO leakage current	V_{RESETn} = 6.5V, $\overline{\text{RESETn}}$, RESETn, $\overline{\text{WDO}}$, and WDO are logic high	–300		300	nA
V_{REF}	Reference voltage output	1µA < I_{VREF} < 0.2mA (source only, no sink)	1.18	1.20	1.22	V
C_{IN}	Input pin capacitance	CTn: 0V to V_{VCC}, other pins: 0V to 6.5V		5		pF
t_W	Input pulse width to SENSEm and $\overline{\text{MR}}$ pins	SENSEm: $1.05V_{ITN} \rightarrow 0.95V_{ITN}$ or $0.95V_{ITP} \rightarrow 1.05V_{ITP}$		4		µs
		$\overline{\text{MR}}$: $0.7V_{CC} \rightarrow 0.3V_{VCC}$		1		ns
t_D	$\overline{\text{RESETn}}$ or RESETn delay time	CTn = open	14	20	24	ms
		CTn = V_{VCC}	225	300	375	ms
t_{WDT}	Watchdog timer timeout period	Start from $\overline{\text{RESET1}}$ or RESET1 release or last WDI transition	450	600	750	ms

(1) Toggling WDI for a period less than t_{WDT} negatively affects I_{VCC}.
(2) These specifications are beyond the recommended V_{VCC} range, and only define $\overline{\text{RESETn}}$ or RESETn output performance during VCC ramp up.
(3) The lowest supply voltage (V_{VCC}) at which $\overline{\text{RESETn}}$ or RESETn becomes active; t_{RISE}(VCC) ≥ 15µs/V.
(4) CTn (where *n* = 1, 2, 3, or 4) are constant current charging sources working from a range of 0V to $V_{TH(CTn)}$, and the device is tested at V_{CTn} = 0.5V. For I_{CT} performance between 0V and $V_{TH(CTn)}$, see Figure 23.

FUNCTIONAL BLOCK DIAGRAM

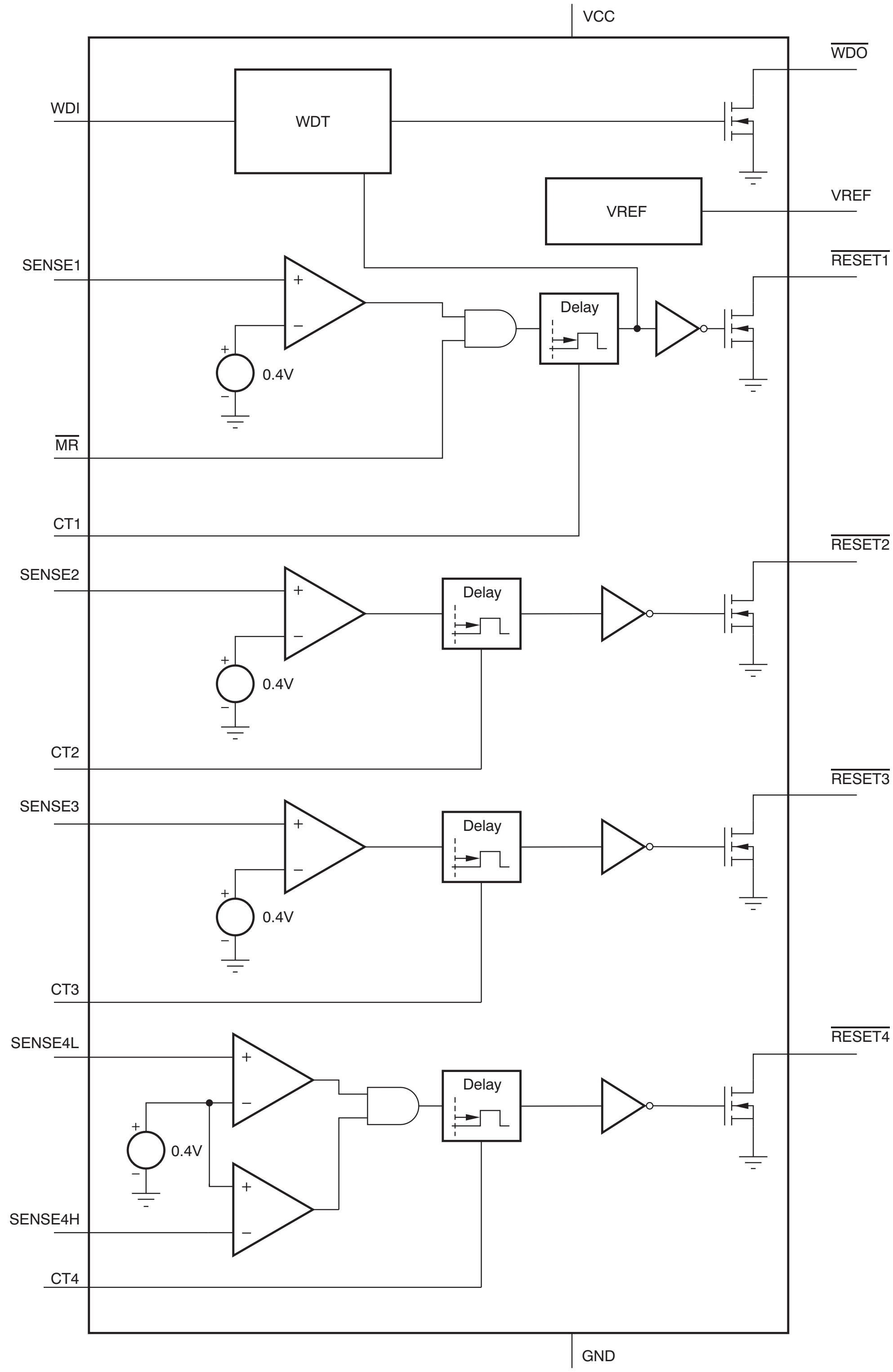
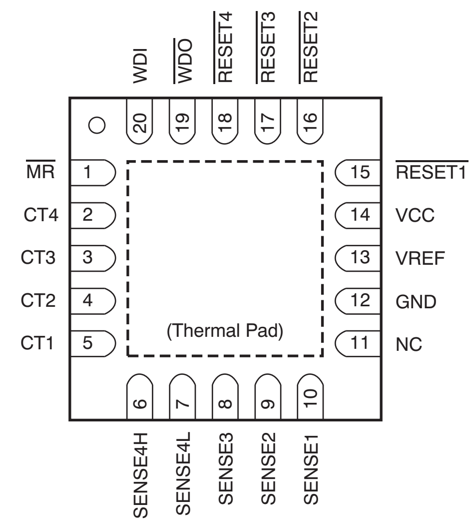


Figure 2. TPS386000

PIN CONFIGURATIONS

**RGP PACKAGE
QFN-20
(TOP VIEW)**



PIN ASSIGNMENTS

PIN NAME	PIN NO.	DESCRIPTION	
VCC	14	Supply voltage. Connecting a 0.1μF ceramic capacitor close to this pin is recommended.	
GND	12	Ground	
SENSE1	10	Monitor voltage input to SVS-1	When the voltage at this terminal drops below the threshold voltage (V_{ITN}), $\overline{RESET1}$ is asserted.
SENSE2	9	Monitor voltage input to SVS-2	When the voltage at this terminal drops below the threshold voltage (V_{ITN}), $\overline{RESET2}$ is asserted.
SENSE3	8	Monitor voltage input to SVS-3	When the voltage at this terminal drops below the threshold voltage (V_{ITN}), $\overline{RESET3}$ is asserted.
SENSE4L	7	Falling monitor voltage input to SVS-4. When the voltage at this terminal drops below the threshold voltage (V_{ITN}), $\overline{RESET4}$ or RESET4 is asserted.	
SENSE4H	6	Rising monitor voltage input to SVS-4. When the voltage at this terminal exceeds the threshold voltage (V_{ITP}), $\overline{RESET4}$ or RESET4 is asserted. This pin can also be used to monitor the negative voltage rail in combination with VREF pin.	
CT1	5	Reset delay programming pin for SVS-1	Connecting this pin to VCC through a 40kΩ to 200kΩ resistor, or leaving it open, selects a fixed delay time (see the Electrical Characteristics). Connecting a capacitor > 220pF between this pin and GND selects the programmable delay time (see the Reset Delay Time section).
CT2	4	Reset delay programming pin for SVS-2	
CT3	3	Reset delay programming pin for SVS-3	
CT4	2	Reset delay programming pin for SVS-4	
VREF	13	Reference voltage output. By connecting a resistor network between this pin and the negative power rail, SENSE4H can monitor the negative power rail. This pin is intended to only source current into resistor(s). Do not connect only capacitors and do not connect resistor(s) to a higher voltage than this pin.	
$\overline{MR}$	1	Manual reset input for SVS-1. Logic low level of this pin asserts $\overline{RESET1}$ or RESET1.	
WDI	20	Watchdog timer (WDT) trigger input. Inputting either a positive or negative logic edge every 610ms (typ) prevents WDT time out at the $\overline{WDO}$ or WDO pin. Timer starts from releasing event of $\overline{RESET1}$ or RESET1.	
NC	11	Not connected. It is recommended to connect this pin to the GND pin (pin 12), which is next to this pin.	
(Thermal Pad)	(PAD)	This is the IC substrate. This pad must be connected only to GND or to the floating thermal pattern on the printed circuit board (PCB).	

PIN ASSIGNMENTS (continued)

PIN		DESCRIPTION	
NAME	NO.		
$\overline{\text{RESET1}}$	15	Active low reset output of SVS-1	$\overline{\text{RESETn}}$ is an open-drain output pin. When $\overline{\text{RESETn}}$ is asserted, this pin remains in a low-impedance state. When $\overline{\text{RESETn}}$ is released, this pin goes to a high-impedance state after the delay time programmed by CTn.
$\overline{\text{RESET2}}$	16	Active low reset output of SVS-2	
$\overline{\text{RESET3}}$	17	Active low reset output of SVS-3	
$\overline{\text{RESET4}}$	18	Active low reset output of SVS-4	
$\overline{\text{WDO}}$	19	Watchdog timer output. This is an open-drain output pin. When WDT times out, this pin goes to a low-impedance state to GND. If there is no WDT timeout, this pin stays in a high-impedance state.	

TYPICAL CHARACTERISTICS

At T_A = +25°C, and V_{CC} = 3.3V, unless otherwise noted.

TPS386000-Q1
SUPPLY CURRENT vs SUPPLY VOLTAGE

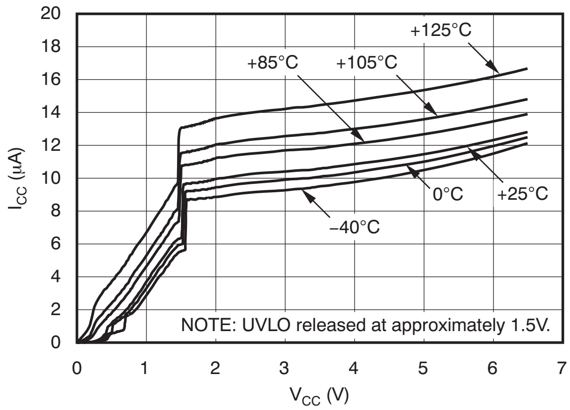


Figure 3.

TPS386000-Q1
RESETn TIMEOUT Period vs CTn

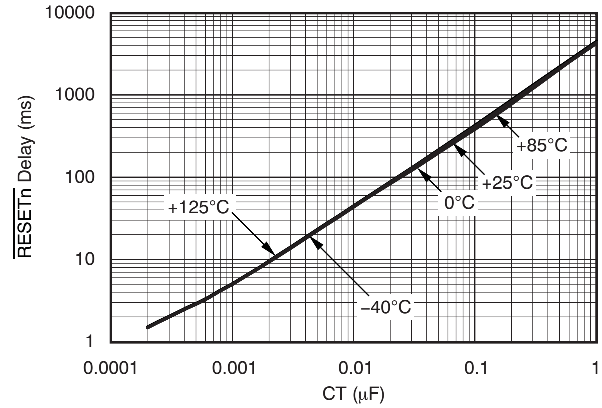


Figure 4.

TPS386000-Q1
RESETn TIMEOUT PERIOD vs TEMPERATURE (CTn = Open)

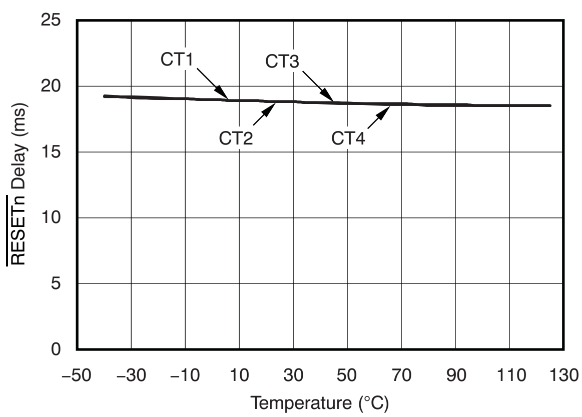


Figure 5.

TPS386000-Q1
RESETn TIMEOUT PERIOD vs TEMPERATURE (CTn = V_{CC})

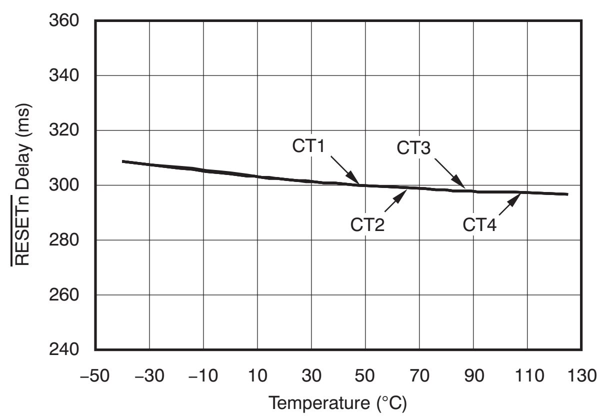


Figure 6.

TPS386000-Q1
RESETn TIMEOUT PERIOD vs TEMPERATURE (CTn = 0.1µF)

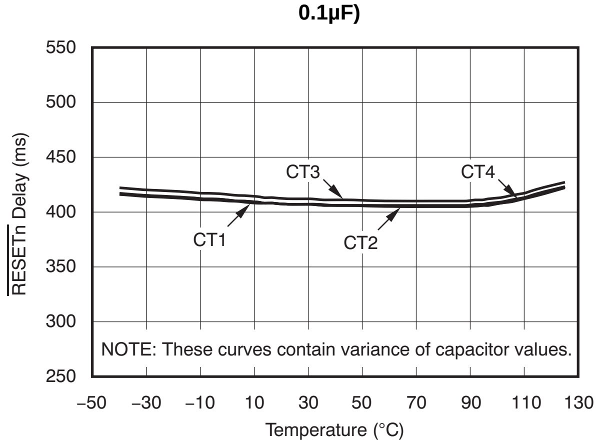


Figure 7.

TPS386000-Q1
WDO TIMEOUT PERIOD vs TEMPERATURE

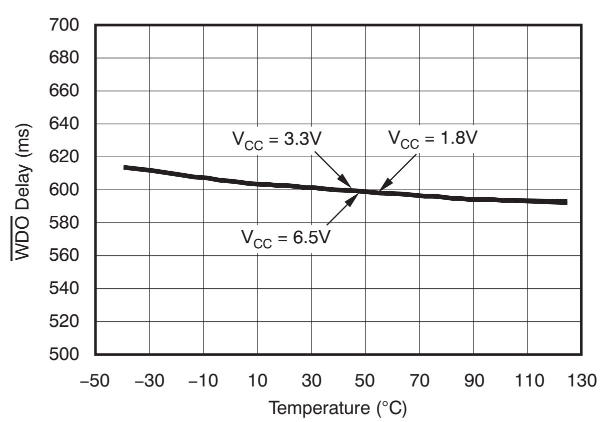


Figure 8.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, and V_{CC} = 3.3V, unless otherwise noted.

TPS386000-Q1
SENSEn MINIMUM PULSE WIDTH
vs SENSEn THRESHOLD OVERDRIVE VOLTAGE

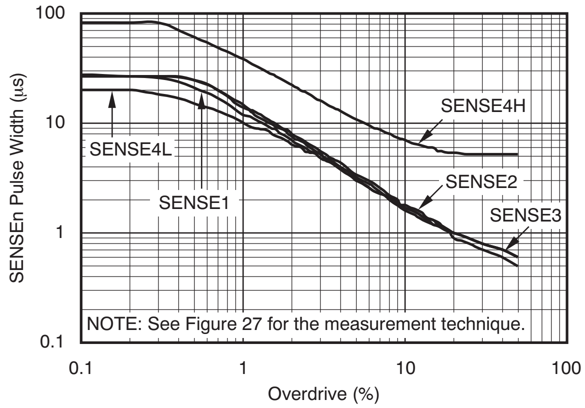


Figure 9.

TPS386000-Q1
SENSE1 THRESHOLD VOLTAGE vs TEMPERATURE

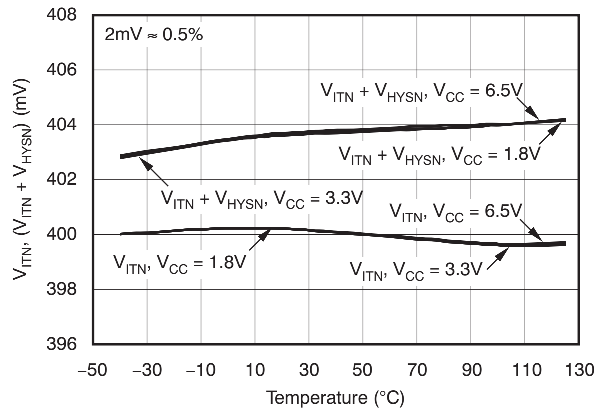


Figure 10.

TPS386000-Q1
SENSE2 THRESHOLD VOLTAGE vs TEMPERATURE

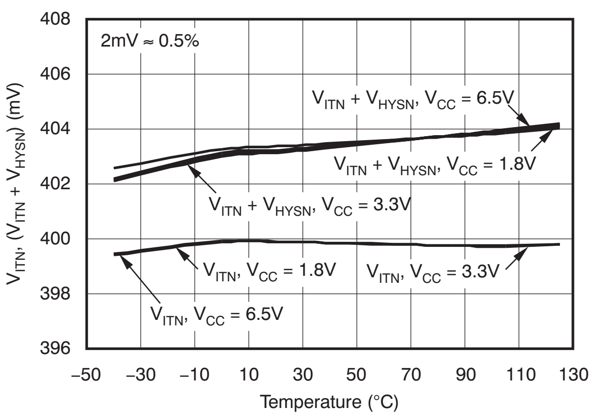


Figure 11.

TPS386000-Q1
SENSE3 THRESHOLD VOLTAGE vs TEMPERATURE

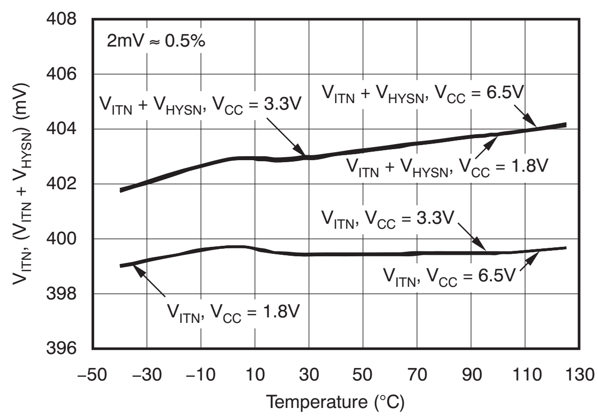


Figure 12.

TPS386000-Q1
SENSE4L THRESHOLD VOLTAGE vs TEMPERATURE

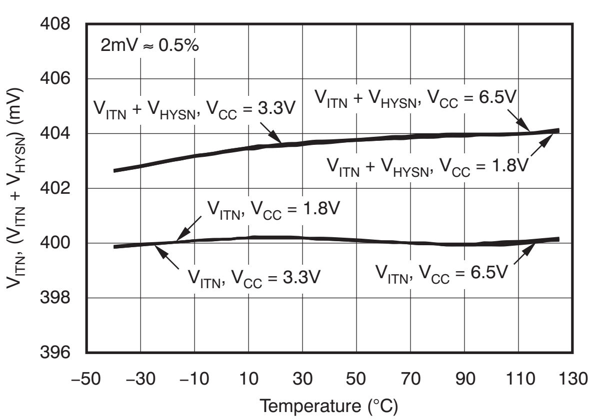


Figure 13.

TPS386000-Q1
SENSE4H THRESHOLD VOLTAGE vs TEMPERATURE

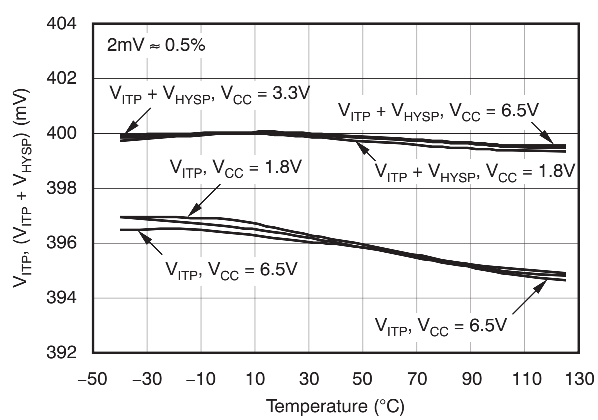


Figure 14.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, and V_{CC} = 3.3V, unless otherwise noted.

OUTPUT VOLTAGE LOW vs OUTPUT CURRENT

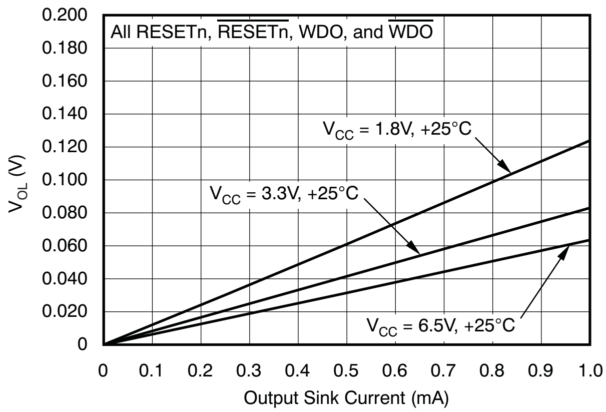


Figure 15.

OUTPUT VOLTAGE LOW AT 1mA vs TEMPERATURE

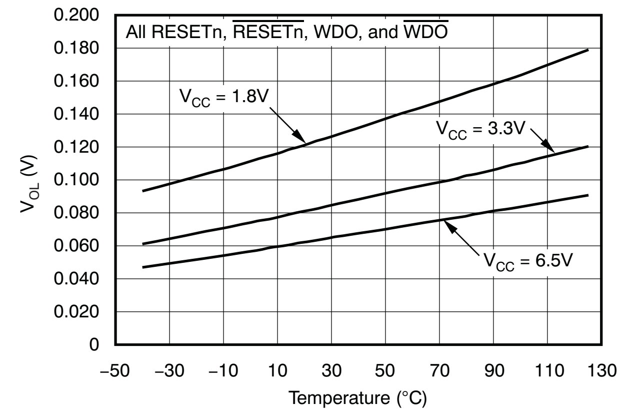


Figure 16.

OUTPUT VOLTAGE HIGH vs OUTPUT CURRENT

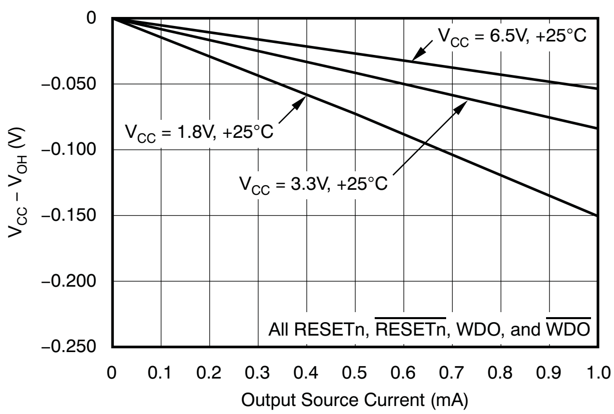


Figure 17.

OUTPUT VOLTAGE HIGH AT 1mA vs TEMPERATURE

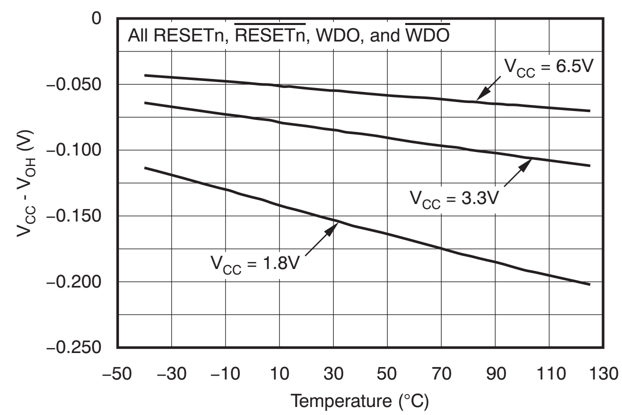


Figure 18.

TPS386000-Q1
V_{REF} OUTPUT LOAD REGULATION (V_{CC} = 1.8V)

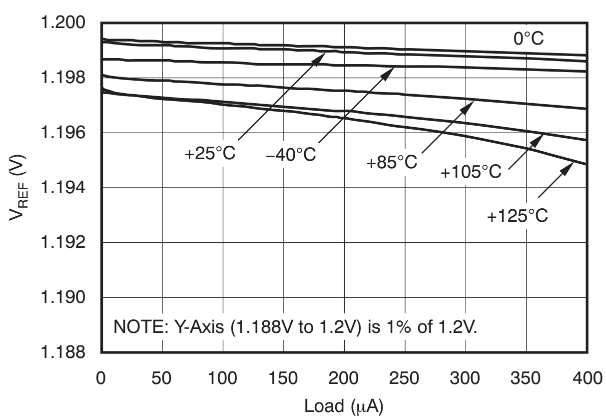


Figure 19.

TPS386000-Q1
V_{REF} OUTPUT LOAD REGULATION (V_{CC} = 3.3V)

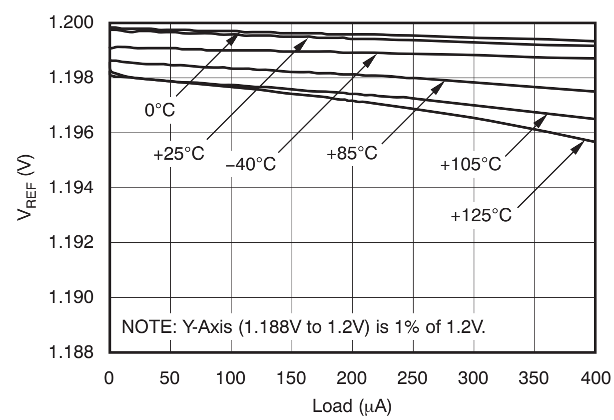


Figure 20.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, and V_{CC} = 3.3V, unless otherwise noted.

TPS386000-Q1
V_{REF} OUTPUT LOAD REGULATION (V_{CC} = 6.5V)

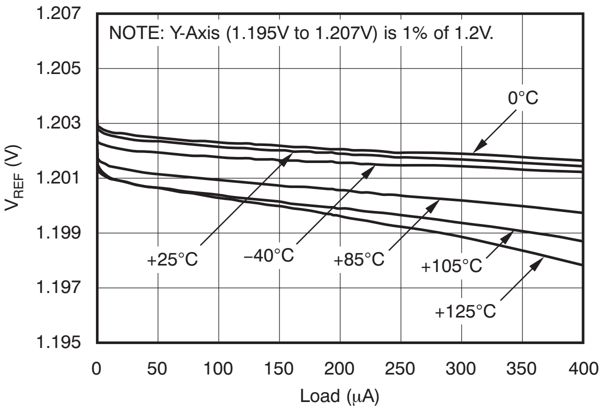


Figure 21.

TPS386000-Q1
V_{REF} AT 0µA vs TEMPERATURE

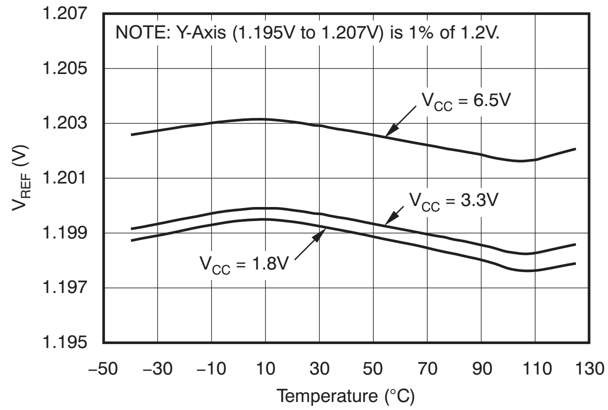


Figure 22.

TPS386000-Q1
CT1 TO CT4 PIN CHARGING CURRENT vs TEMPERATURE OVER CT PIN VOLTAGE

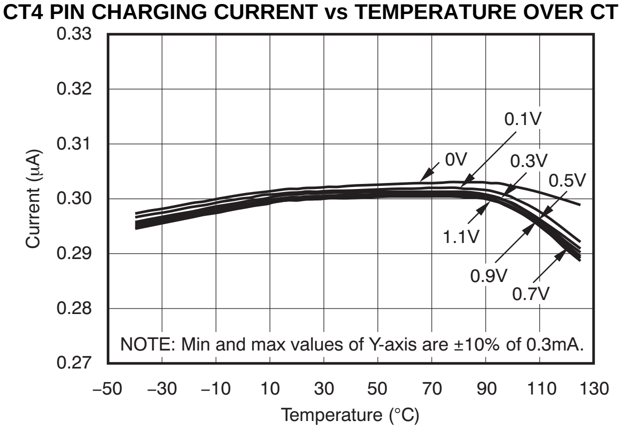


Figure 23.

PARAMETRIC MEASUREMENT INFORMATION

TEST CIRCUIT

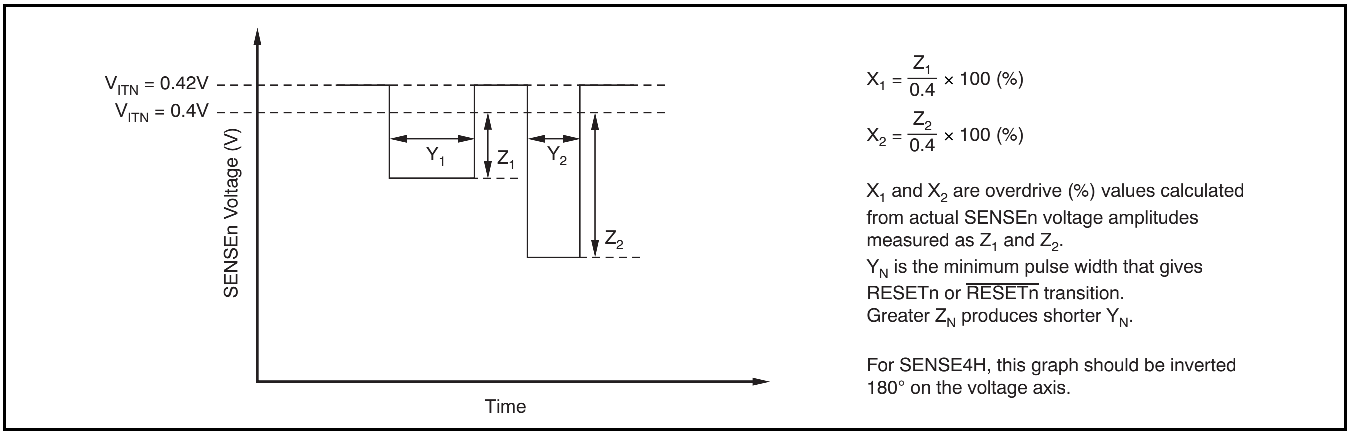


Figure 24.

GENERAL DESCRIPTION

The TPS386000-Q1 multi-channel supervisory device family combines four complete SVS function sets into one IC. The design of each SVS channel is based on the single-channel supervisory device series, TPS3808. The TPS386000-Q1 is designed to assert RESETn or $\overline{\text{RESETn}}$ signals, as shown in Table 1, Table 2, Table 3, and Table 4. The RESETn or $\overline{\text{RESETn}}$ outputs remain asserted during a user-configurable delay time after the event of reset release (see the Reset Delay Time section). Each SENSEm (m = 1, 2, 3, 4L) pin can be set to any voltage threshold above 0.4V using an external resistor divider. The SENSE4H pin can be used for any overvoltage detection greater than 0.4V, or for negative voltage detection using an external resistor divider (see the *Sensing Voltage Less Than 0.4V* section). A broad range of voltage threshold and reset delay time adjustments can be supported, allowing these devices to be used in a wide array of applications.

Table 1. SVS-1 Truth Table

CONDITION		OUTPUT	STATUS
		TPS386000-Q1	
$\overline{\text{MR}}$ = Low	SENSE1 < V_{ITN}	$\overline{\text{RESET1}}$ = Low	Reset asserted
$\overline{\text{MR}}$ = Low	SENSE1 > V_{ITN}	$\overline{\text{RESET1}}$ = Low	Reset asserted
$\overline{\text{MR}}$ = High	SENSE1 < V_{ITN}	$\overline{\text{RESET1}}$ = Low	Reset asserted
$\overline{\text{MR}}$ = High	SENSE1 > V_{ITN}	$\overline{\text{RESET1}}$ = High	**Reset released after delay**

Table 2. SVS-2 Truth Table

CONDITION	OUTPUT	STATUS
	TPS386000-Q1	
SENSE2 < V_{ITN}	$\overline{\text{RESET2}}$ = Low	Reset asserted
SENSE2 > V_{ITN}	$\overline{\text{RESET2}}$ = High	**Reset released after delay**

Table 3. SVS-3 Truth Table

CONDITION	OUTPUT TPS386000-Q1	STATUS
SENSE3 < V_{ITN}	$\overline{\text{RESET3}}$ = Low	Reset asserted
SENSE3 > V_{ITN}	$\overline{\text{RESET3}}$ = High	**Reset released after delay**

Table 4. SVS-4 Truth Table

CONDITION		OUTPUT TPS386000-Q1	STATUS
SENSE4L < V_{ITN}	SENSE4H > V_{ITP}	$\overline{\text{RESET4}}$ = Low	Reset asserted
SENSE4L < V_{ITN}	SENSE4H < V_{ITP}	$\overline{\text{RESET4}}$ = Low	Reset asserted
SENSE4L > V_{ITN}	SENSE4H > V_{ITP}	$\overline{\text{RESET4}}$ = Low	Reset asserted
SENSE4L > V_{ITN}	SENSE4H < V_{ITP}	$\overline{\text{RESET4}}$ = High	**Reset released after delay**

Table 5. Watchdog Timer (WDT) Truth Table

CONDITION				OUTPUT	STATUS
$\overline{\text{WDO}}$	WDO	$\overline{\text{RESET1}}$ OR RESET1	WDI PULSE INPUT	TPS386000-Q1	
Low	High	Asserted	Toggling	$\overline{\text{WDO}}$ = low	Remains in WDT timeout
Low	High	Asserted	610ms after last WDI↑ or WDI↓	$\overline{\text{WDO}}$ = low	Remains in WDT timeout
Low	High	Released	Toggling	$\overline{\text{WDO}}$ = low	Remains in WDT timeout
Low	High	Released	610ms after last WDI↑ or WDI↓	$\overline{\text{WDO}}$ = low	Remains in WDT timeout
High	Low	Asserted	Toggling	$\overline{\text{WDO}}$ = high	Normal operation
High	Low	Asserted	610ms after last WDI↑ or WDI↓	$\overline{\text{WDO}}$ = high	Normal operation
High	Low	Released	Toggling	$\overline{\text{WDO}}$ = high	Normal operation
High	Low	Released	610ms after last WDI↑ or WDI↓	$\overline{\text{WDO}}$ = low	Enters WDT timeout

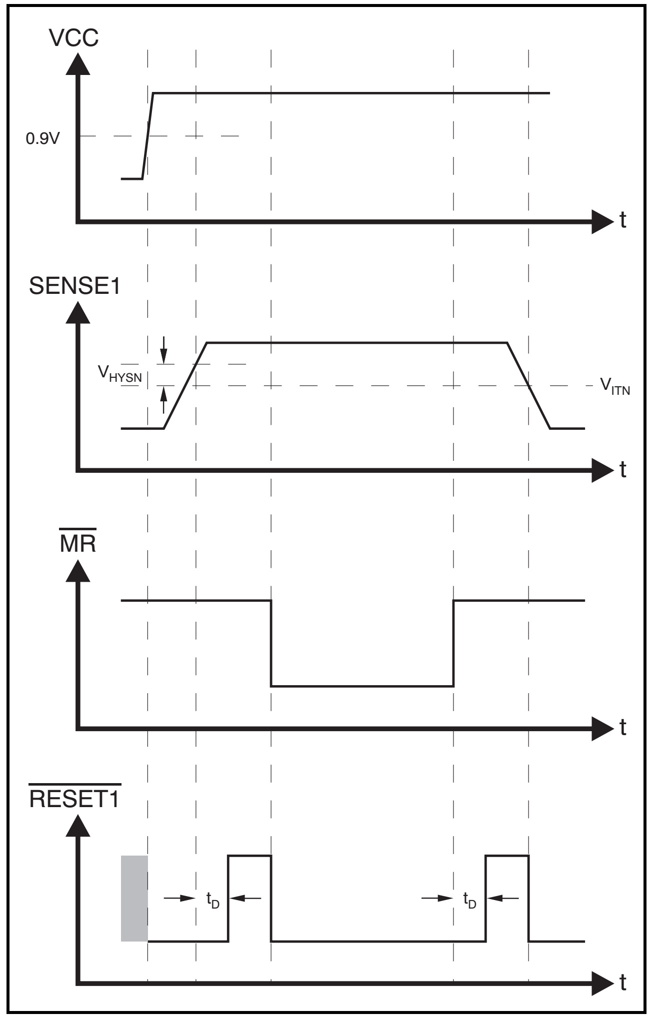
RESET OUTPUT

In a typical TPS386000-Q1 application, $\overline{\text{RESETn}}$ or RESETn outputs are connected to the reset input of a processor (DSP, CPU, FPGA, ASIC, etc.), or connected to the enable input of a voltage regulator (DC-DC, LDO, etc.)

The TPS386000-Q1 provides open-drain reset outputs. Pull-up resistors must be used to hold these lines high when $\overline{\text{RESETn}}$ is not asserted, or when RESETn is asserted. By connecting pull-up resistors to the proper voltage rails (up to 6.5V), $\overline{\text{RESETn}}$ or RESETn output nodes can be connected to the other devices at the correct interface voltage levels. The pull-up resistor should be no smaller than 10kΩ because of the safe operation of the output transistors. By using wired-OR logic, any combination of $\overline{\text{RESETn}}$ can be merged into one logic signal.

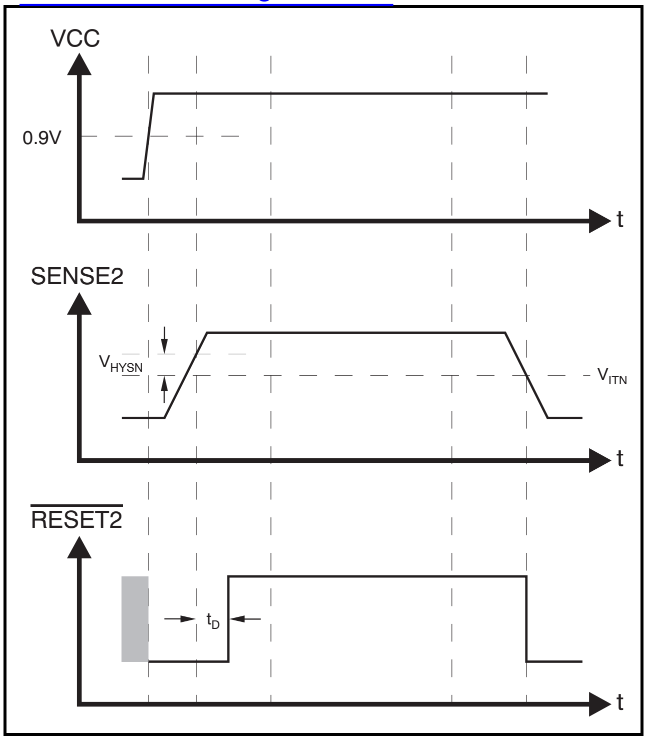
The TPS386000-Q1 provides push-pull reset outputs. The logic high level of the outputs is determined by the VCC voltage. With this configuration, pull-up resistors are not required and some board area can be saved. However, all the interface logic levels should be examined. All $\overline{\text{RESETn}}$ or RESETn connections must be compatible with the VCC logic level.

The $\overline{\text{RESETn}}$ or RESETn outputs are defined for VCC voltage higher than 0.9V. To ensure that the target processor(s) are properly reset, the VCC supply input should be fed by the available power rail as early as possible in application circuits. Table 1, Table 2, Table 3, and Table 4 are truth tables that describe how the outputs are asserted or released. Figure 25, Figure 26, Figure 27, and Figure 28 show the SVS-n timing diagrams. When the condition(s) are met, the device changes the state of SVS-n from asserted to released after a user-configurable delay time. However, the transitions from released-state to asserted-state are performed almost immediately with minimal propagation delay. Figure 27 describes relationship between threshold voltages (V_{ITN} and V_{HYSN}) and SENSEm voltage; and all SVS-1, SVS-2, SVS-3, and SVS-4 have the same behavior of Figure 27.



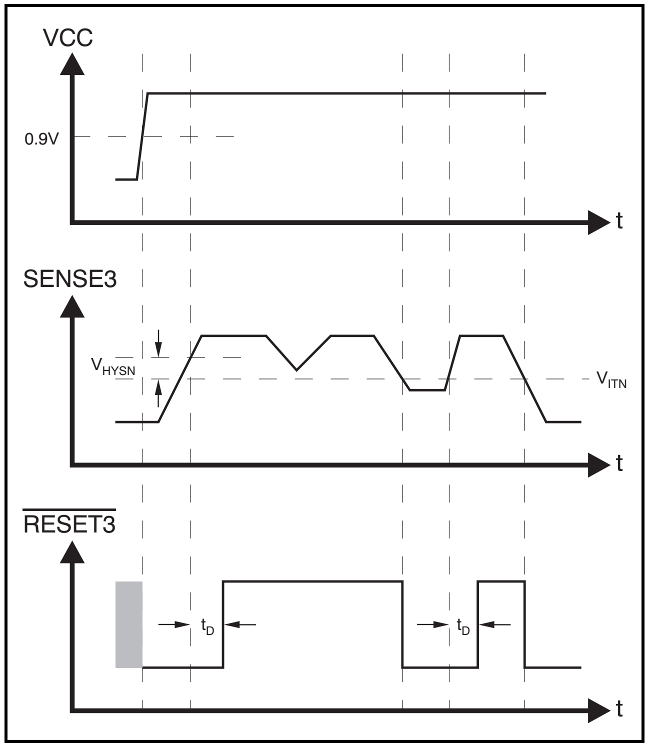
NOTE: The TPS386000-Q1 is shown here using $\overline{\text{RESETn}}$.

Figure 25. SVS-1 Timing Diagram



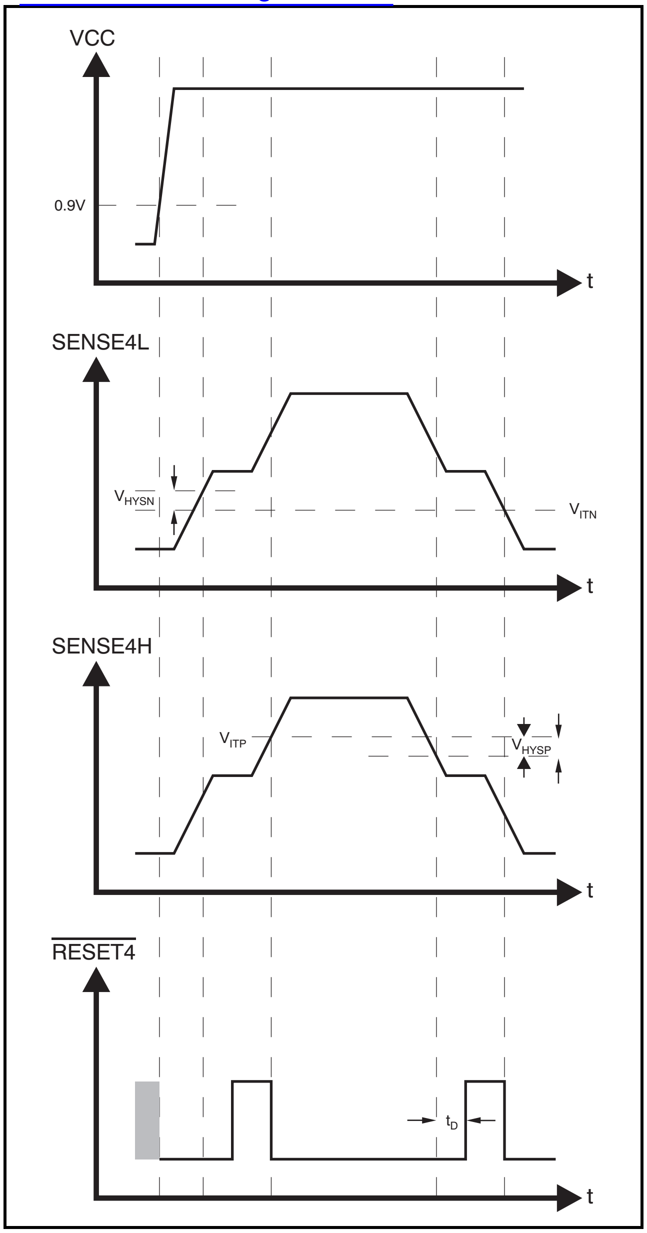
NOTE: The TPS386000-Q1 is shown here using $\overline{\text{RESETn}}$.

Figure 26. SVS-2 Timing Diagram



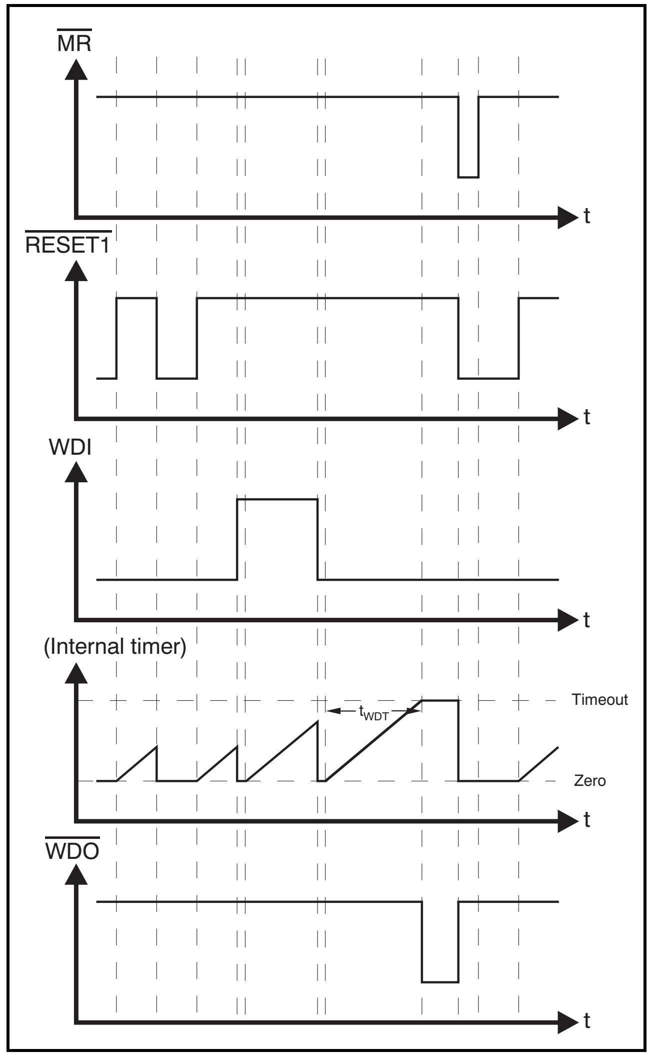
NOTE: The TPS386000-Q1 is shown here using $\overline{\text{RESETn}}$.

Figure 27. SVS-3 Timing Diagram



NOTE: The TPS386000-Q1 is shown here using $\overline{\text{RESETn}}$.

Figure 28. SVS-4 Timing Diagram



NOTE: The TPS386000-Q1 is shown here using $\overline{\text{RESETn}}$ and $\overline{\text{WDO}}$.

Figure 29. WDT Timing Diagram

SENSE INPUT

The SENSEm inputs are pins that allow any system voltages to be monitored. If the voltage at the SENSE1, SENSE2, SENSE3, or SENSE4L pins drops below V_{ITN}, then the corresponding reset outputs are asserted. If the voltage at the SENSE4H pin exceeds V_{ITP}, then $\overline{RESET4}$ or RESET4 is asserted. The comparators have a built-in hysteresis to ensure smooth reset output assertions and deassertions. Although not required in most cases, for extremely noise applications, it is good analog design practice to place a 1nF to 10nF bypass capacitor at the SENSEm input in order to reduce sensitivity to transients, layout parasitics, and interference between power rails monitored by this device. A typical connection of resistor dividers are shown in Figure 30. All the SENSEm pins can be used to monitor voltage rails down to 0.4V. Threshold voltages can be calculated by following equations:

$VCC1\_target = (1 + R_{S1H}/R_{S1L}) \times 0.4$ (V) (1)

$VCC2\_target = (1 + R_{S2H}/R_{S2L}) \times 0.4$ (V) (2)

$VCC3\_target = (1 + R_{S3H}/R_{S3L}) \times 0.4$ (V) (3)

VCC4_target1 = {1+ R_{S4H}/®$_{S4M}$ + R_{S4L})} × 0.4 (V) (4)

VCC4_target2 = {1+ ®$_{S4H}$ + R_{S4M})/R_{S4L}} × 0.4 (V) (5)

Where VCC4_target1 is the undervoltage threshold, and VCC4_target2 is the overvoltage threshold.

WINDOW COMPARATOR

The comparator at the SENSE4H pin has the opposite comparison polarity to the other SENSEm pins. In the configuration shown in Figure 30, this comparator monitors overvoltage of the VCC4 node; combined with the comparator at SENSE4L, SVS-4 forms a window comparator.

SENSING VOLTAGE LESS THAN 0.4V

By using voltage reference output VREF, the SVS-4 comparator can monitor negative voltage or positive voltage lower than 0.4V. Figure 1 shows this usage in an application circuit. SVS-4 monitors the positive and negative voltage power rail (for example, +15V and –15V supply to an op amp) and the $\overline{RESET4}$ or RESET4 output status continues to be as described in Table 4. Note that R_{S42H} is located at higher voltage position than R_{S42L}. The threshold voltage calculations are shown in the following equations:

$VCC41\_target = (1 + R_{S41H}/R_{S41L}) \times 0.4$ (V) (6)

$VCC42\_target = (1 + R_{S42L}/R_{S42H}) \times 0.4 - R_{S42L}/R_{S42H} \times V_{REF}$ (7)

$= 0.4 - R_{S42L}/R_{S42H} \times 0.8$ (V) (8)

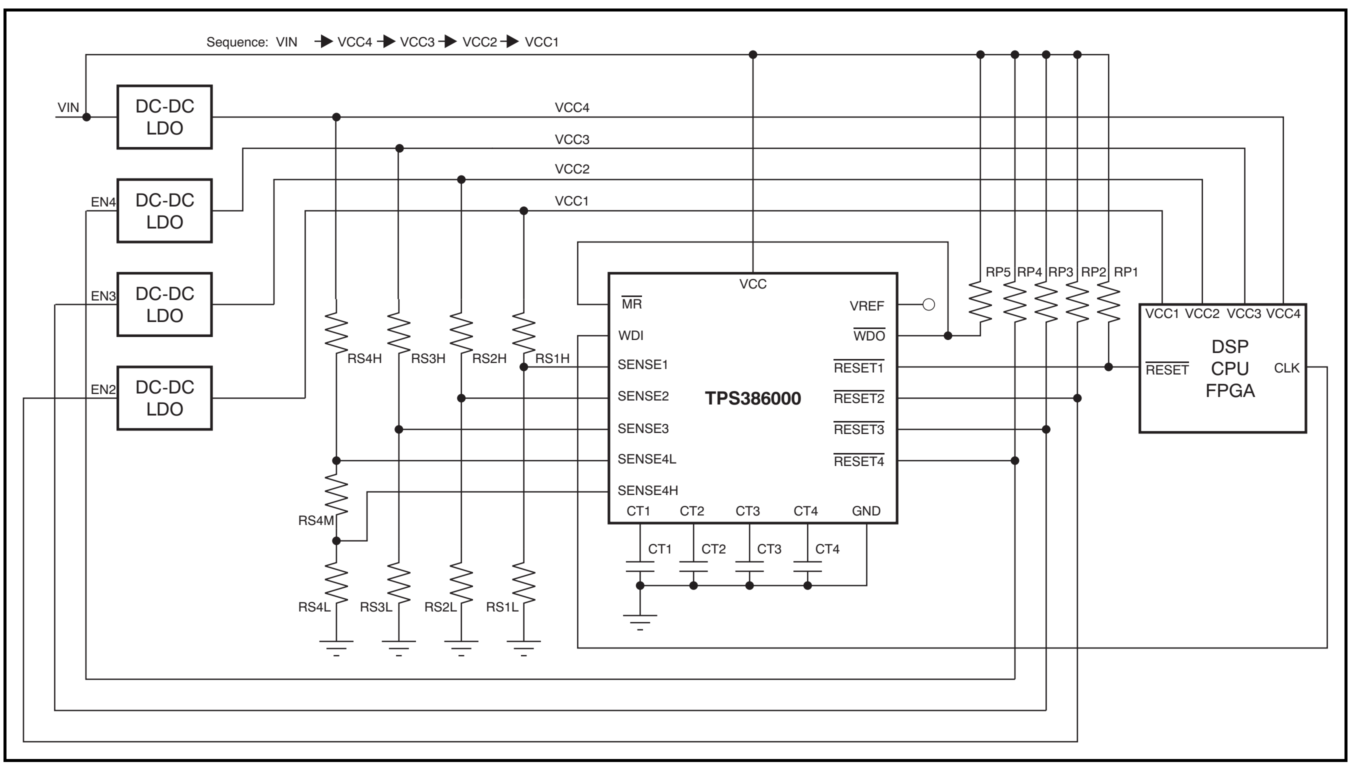


Figure 30. Typical Application Circuit (SVS-4: Window Comparator)

RESET DELAY TIME

Each of the SVS-n channels can be configured independently in one of three modes. Table 6 describes the delay time settings.

Table 6. Delay Timing Selection

CTn CONNECTION	DELAY TIME
Pull-up to VCC	300ms (typ)
Open	20 ms (typ)
Capacitor to GND	Programmable

To select the 300ms fixed delay time, the CTn pin should be pulled up to VCC using a resistor from 40kΩ to 200kΩ. Note that there is a pulldown transistor from CTn to GND that turns on every time the device powers on to determine and confirm CTn pin status; therefore, a direct connection of CTn to VCC causes a large current flow. To select the 20ms fixed delay time, the CTn pin should be left open. To program a user-defined adjustable delay time, an external capacitor must be connected between CTn and GND. The adjustable delay time can be calculated by the following equation:

$$C_{CT}\ (\text{nF}) = [t_{DELAY}\ (\text{ms}) - 0.5(\text{ms})] \times 0.242 \qquad (9)$$

Using this equation, a delay time can be set to between 1.4ms to 10s. The external capacitor should be greater than 220pF (nominal) so that the TPS386000-Q1 can distinguish it from an open CT pin. The reset delay time is determined by the time it takes an on-chip, precision 300nA current source to charge the external capacitor to 1.24V. When the $\overline{\text{RESETn}}$ or RESETn outputs are asserted, the corresponding capacitors are discharged. When the condition to release $\overline{\text{RESETn}}$ or RESETn occurs, the internal current sources are enabled and begin to charge the external capacitors. When the CTn voltage on a capacitor reaches 1.24V, the corresponding $\overline{\text{RESETn}}$ or RESETn pins are released. Note that a low leakage type capacitor (such as ceramic) should be used, and that stray capacitance around this pin may cause errors in the reset delay time.

MANUAL RESET

The manual reset ($\overline{\text{MR}}$) input allows external logic signal from other processors, logic circuits, and/or discrete sensors to initiate a device reset. Because $\overline{\text{MR}}$ is connected to SVS-1, the $\overline{\text{RESET1}}$ or RESET1 pin is intended to be connected to processor(s) as a primary reset source. A logic low at $\overline{\text{MR}}$ causes $\overline{\text{RESET1}}$ or RESET1 to assert. After $\overline{\text{MR}}$ returns to a logic high and SENSE1 is above its reset threshold, $\overline{\text{RESET1}}$ or RESET1 is released after the user-configured reset delay time. Note that unlike the TPS3808 series, the TPS386000-Q1 does not integrate an internal pull-up resistor between $\overline{\text{MR}}$ and VCC.

To control the $\overline{\text{MR}}$ function from more than one logic signal, the logic signals can be combined by wired-OR into the $\overline{\text{MR}}$ pin using multiple NMOS transistors and one pull-up resistor.

WATCHDOG TIMER

The TPS386000-Q1 provides a watchdog timer with a dedicated watchdog error output, $\overline{\text{WDO}}$ or WDO. The $\overline{\text{WDO}}$ or WDO output enables application board designers to easily detect and resolve the hang-up status of a processor. As with $\overline{\text{MR}}$, the watchdog timer function of the device is also tied to SVS-1. Figure 29 shows the timing diagram of the WDT function. Once $\overline{\text{RESET1}}$ or RESET1 is released, the internal watchdog timer starts its countdown. Inputting a logic level transition at WDI resets the internal timer count and the timer restarts the countdown. If the TPS386000-Q1 fails to receive any WDI rising or falling edge within the WDT period, the WDT times out and asserts $\overline{\text{WDO}}$ or WDO. After $\overline{\text{WDO}}$ or WDO is asserted, the device holds the status with the internal latch circuit. To clear this timeout status, a reset assertion of $\overline{\text{RESET1}}$ or RESET is required. That is, a negative pulse to $\overline{\text{MR}}$, a SENSE1 voltage less than V_{ITN}, or a VCC power-down is required.

To reset the processor by WDT timeout, $\overline{\text{WDO}}$ can be combined with $\overline{\text{RESET1}}$ by using the wired-OR with the TPS386000-Q1 option.

For legacy applications where the watchdog timer timeout causes $\overline{\text{RESET1}}$ to assert, connect $\overline{\text{WDO}}$ to $\overline{\text{MR}}$; see Figure 30 for the connections and see Figure 31 and Figure 32 for the timing diagram. This legacy support configuration is available with the TPS386000-Q1.

IMMUNITY TO SENSEn VOLTAGE TRANSIENTS

The TPS386000-Q1 is relatively immune to short negative transients on the SENSEn pin. Sensitivity to transients depends on threshold overdrive, as shown in the typical performance graph *TPS386000-Q1 SENSEn Minimum Pulse Width vs SENSEn Threshold Overdrive Voltage* (Figure 9).

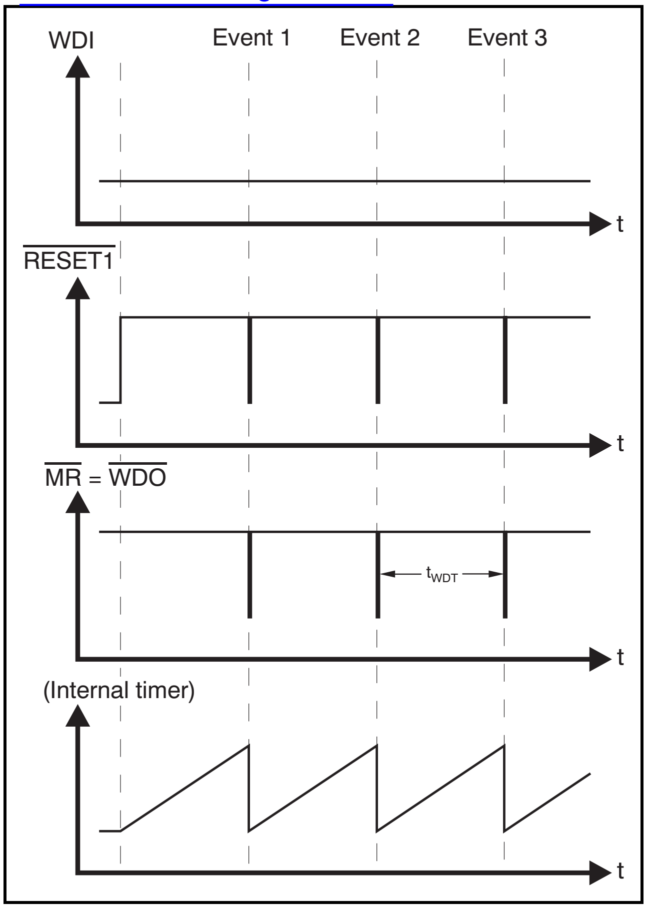


Figure 31. Legacy WDT Configuration Timing Diagram

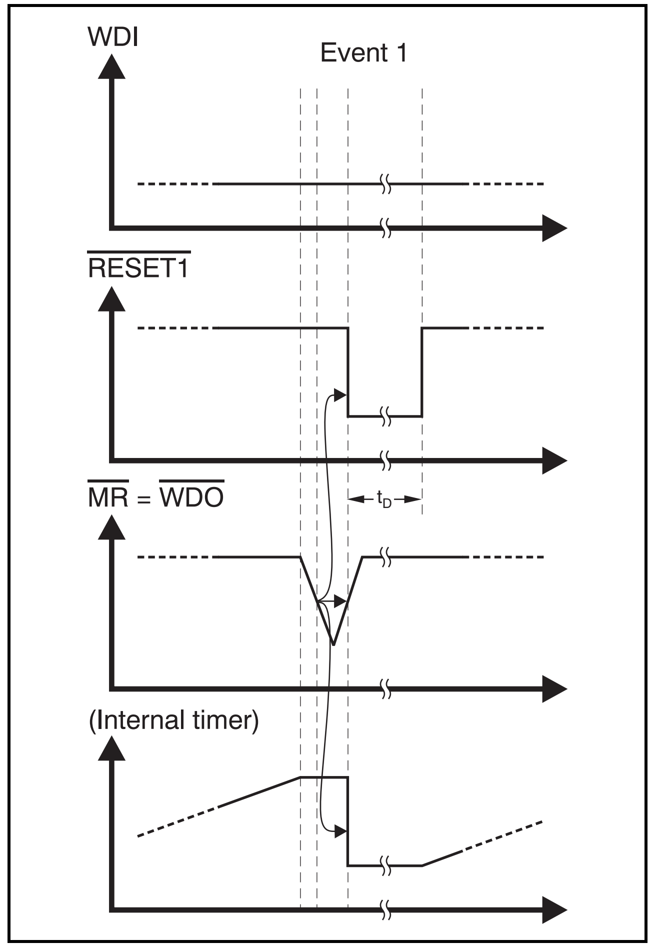


Figure 32. Enlarged View of Event 1 from Figure 31

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Pea
TPS386000QRGPRQ1	ACTIVE	QFN	RGP	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.t information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable fo
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retard in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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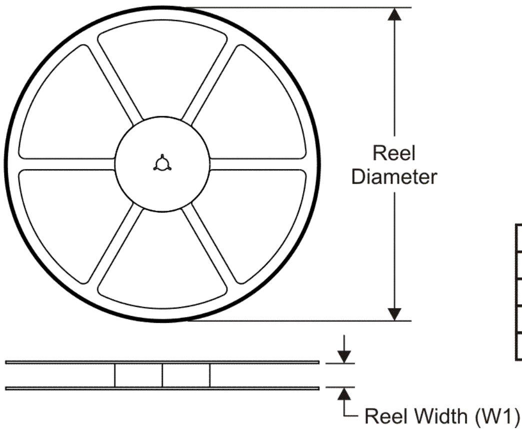
OTHER QUALIFIED VERSIONS OF TPS386000-Q1 :

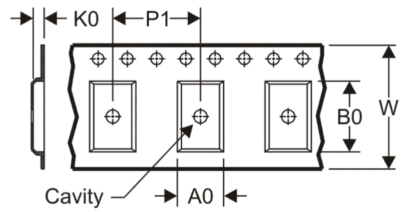
- Catalog: TPS386000

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

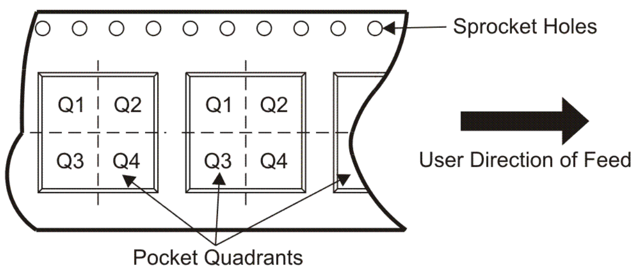
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

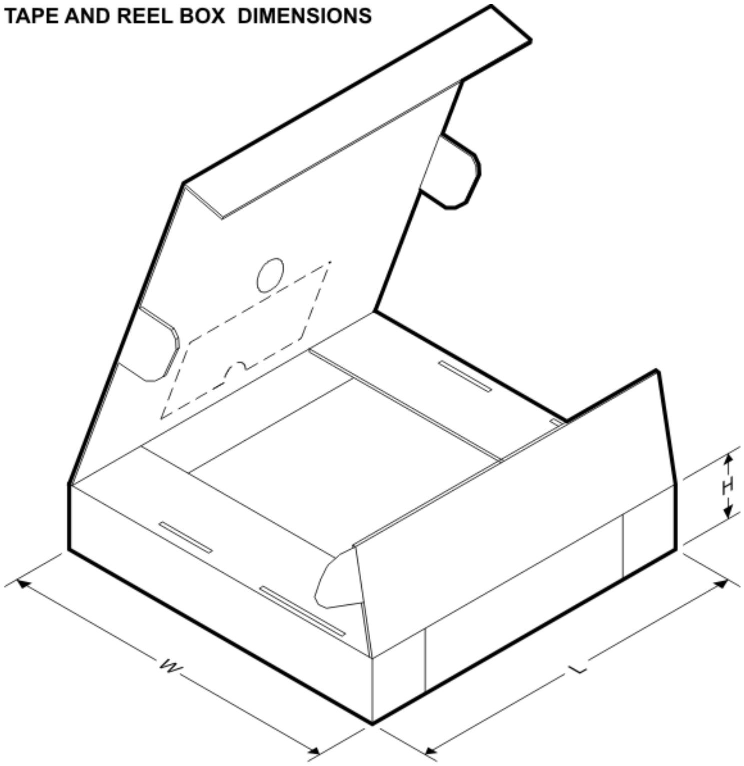
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS386000QRGPRQ1	QFN	RGP	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

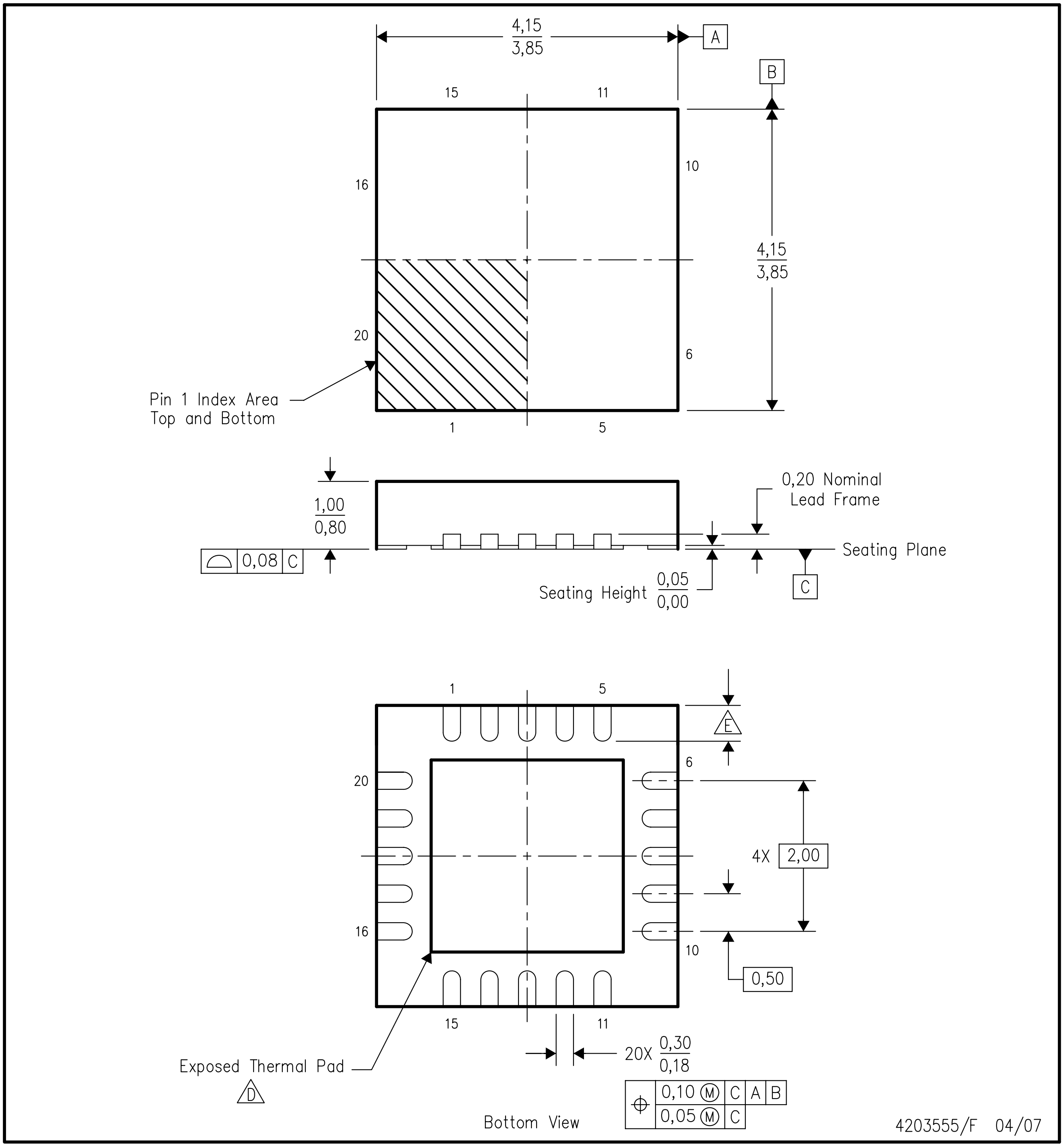


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS386000QRGPRQ1	QFN	RGP	20	3000	346.0	346.0	29.0

查询"TPS386000-Q1"供应商

RGP (S–PQFP–N20) PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.

B. This drawing is subject to change without notice.

C. QFN (Quad Flatpack No–Lead) package configuration.

D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

E. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

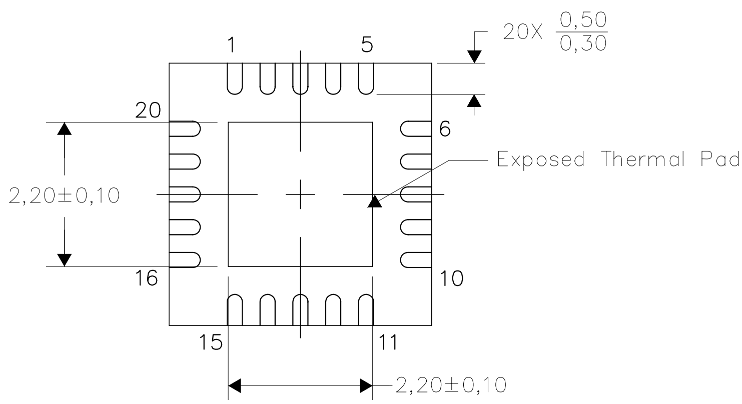
RGP (S-PVQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



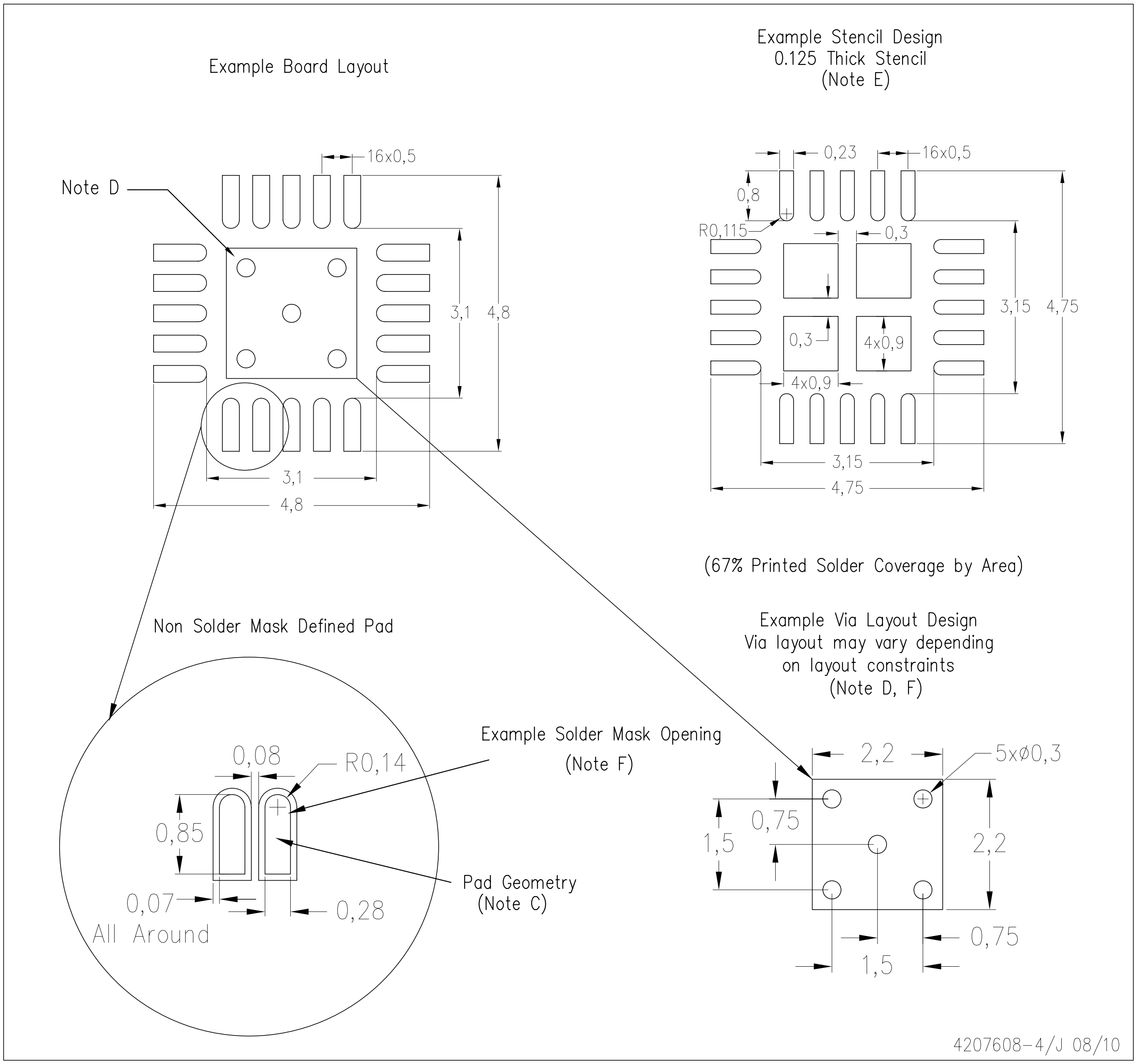
Bottom View

Exposed Thermal Pad Dimensions

4206346-4/U 08/10

NOTES: A. All linear dimensions are in millimeters

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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