

IGBT Chip in NPT-technology

FEATURES:

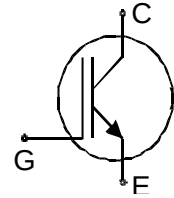
- 600V NPT technology
- 100µm chip
- short circuit prove
- positive temperature coefficient
- easy paralleling

This chip is used for:

- IGBT-Modules

Applications:

- drives



Chip Type	V _{CE}	I _{CN}	Die Size	Package	Ordering Code
SIGC61T60NC	600V	75A	6.99 x 8.79 mm ²	sawn on foil	Q67050-A4160-A001

MECHANICAL PARAMETER:

Raster size	6.99 x 8.79	mm ²
Area total / active	61.44 / 53.7	
Emitter pad size	2x(2.98x5.48)	
Gate pad size	0.8 x 1.5	
Thickness	100	µm
Wafer size	150	mm
Flat position	90	deg
Max.possible chips per wafer	200	
Passivation frontside	Photoimide	
Emitter metallization	3200 nm Al Si 1%	
Collector metallization	1400 nm Ni Ag –system suitable for epoxy and soft solder die bonding	
Die bond	electrically conductive glue or solder	
Wire bond	Al, ≤500µm	
Reject Ink Dot Size	Ø 0.65mm ; max 1.2mm	
Recommended Storage Environment	store in original container, in dry nitrogen, < 6 month at an ambient temperature of 23°C	

MAXIMUM RATINGS:

Parameter	Symbol	Value	Unit
Collector-emitter voltage, $T_j=25^\circ\text{C}$	V_{CE}	600	V
DC collector current, limited by T_{jmax}	I_C	¹⁾	A
Pulsed collector current, t_p limited by T_{jmax}	I_{Cpuls}	225	A
Gate emitter voltage	V_{GE}	± 20	V
Operating junction and storage temperature	T_j, T_{stg}	-55 ... +150	$^\circ\text{C}$

¹⁾ depending on thermal properties of assembly

STATIC CHARACTERISTICS (tested on chip), $T_j=25^\circ\text{C}$, unless otherwise specified:

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Collector-emitter breakdown voltage	$V_{(BR)CES}$	$V_{GE}=0\text{V}, I_C=3\text{mA}$	600			V
Collector-emitter saturation voltage	$V_{CE(sat)}$	$V_{GE}=15\text{V}, I_C=75\text{A}$	1.7	2.1	2.5	
Gate-emitter threshold voltage	$V_{GE(th)}$	$I_C=1.5\text{mA}, V_{GE}=V_{CE}$	4.5	5.5	6.5	
Zero gate voltage collector current	I_{CES}	$V_{CE}=600\text{V}, V_{GE}=0\text{V}$			5.2	μA
Gate-emitter leakage current	I_{GES}	$V_{CE}=0\text{V}, V_{GE}=20\text{V}$			210	nA

DYNAMIC CHARACTERISTICS (tested at component):

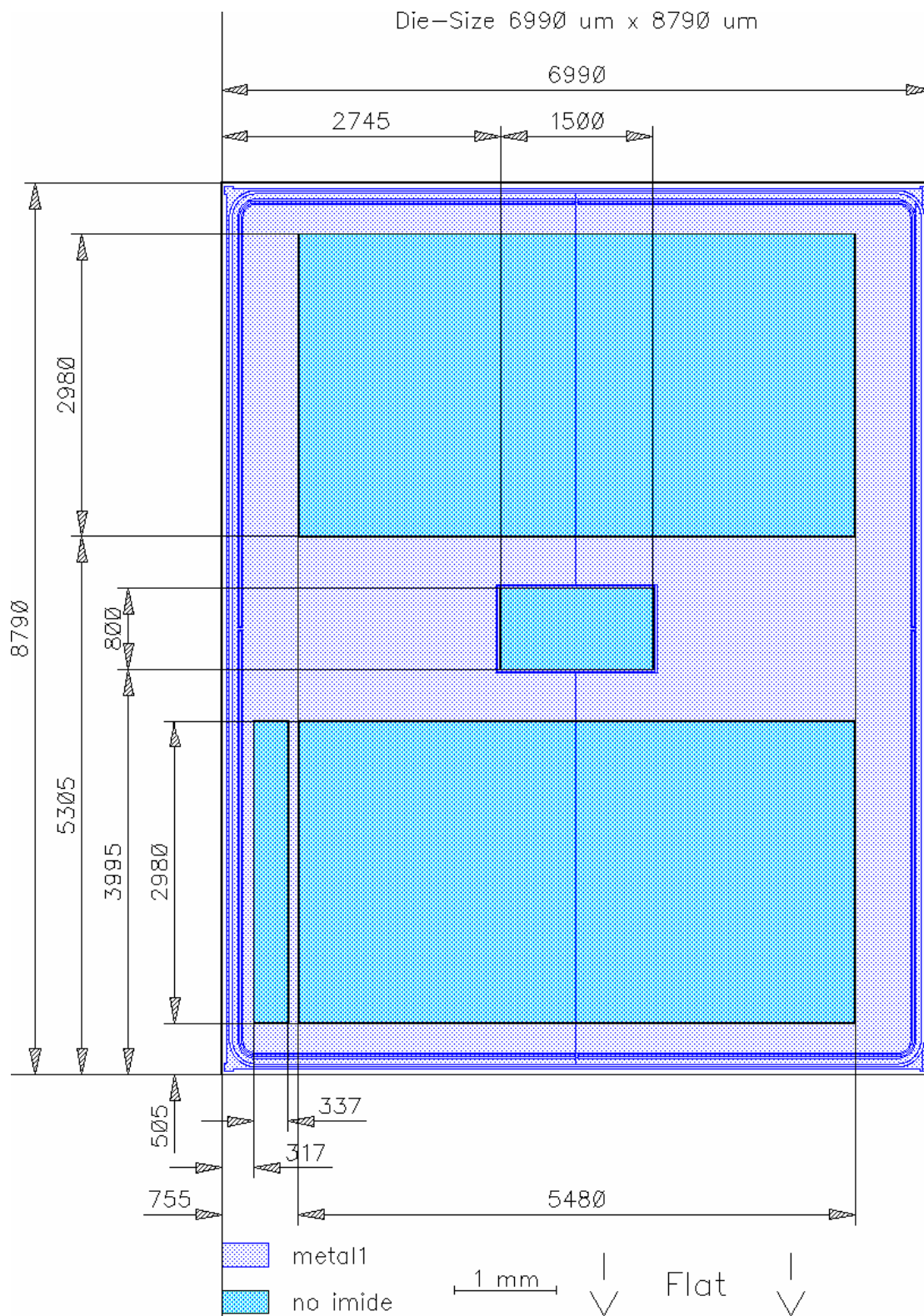
Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Input capacitance	C_{iss}	$V_{CE}=25\text{V}$	-	3300	-	pF
Output capacitance	C_{oss}	$V_{GE}=0\text{V}$	-	tbd	-	
Reverse transfer capacitance	C_{rss}	$f=1\text{MHz}$	-	300	-	

SWITCHING CHARACTERISTICS (tested at component), Inductive Load:

Parameter	Symbol	Conditions ¹⁾	Value			Unit
			min.	typ.	max.	
Turn-on delay time	$t_{d(on)}$	$T_j=125^\circ\text{C}$ $V_{CC}=300\text{V}$ $I_C=75\text{A}$ $V_{GE}=\pm 15\text{V}$ $R_G=3\Omega$	-	65	-	ns
Rise time	t_r		-	25	-	
Turn-off delay time	$t_{d(off)}$		-	170	-	
Fall time	t_f		-	35	-	

¹⁾ values also influenced by parasitic L- and C- in measurement and package.

CHIP DRAWING:



FURTHER ELECTRICAL CHARACTERISTICS:

This chip data sheet refers to the device data sheet

BSM 75 GD 60 DLC

Econo Pack2 short pin

Description:

AQL 0,65 for visual inspection according to failure catalog

Electrostatic Discharge Sensitive Device according to MIL-STD 883

Test-Normen Villach/Prüffeld

Published by
Infineon Technologies AG,
Bereich Kommunikation
St.-Martin-Strasse 53,
D-81541 München
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