4-CHANNEL 8:16 MULTIPLEXER/DEMULTIPLEXER PCI EXPRESS SWITCH

Check for Samples: TS2PCIE412

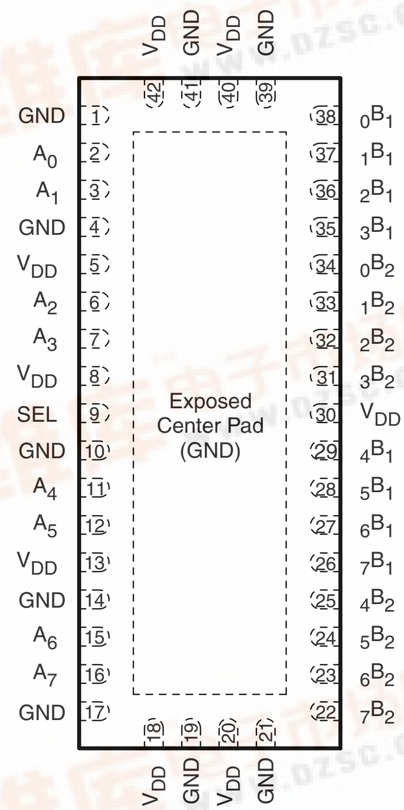
FEATURES

- Compatible With PCI Express (PCIe) Standard
- Wide Bandwidth of over 3 Gbps
- Low Crosstalk (X_{TALK} = –32 dB Typ at 1.25 GHz)
- O_{IRR} = –36.3 dB Typical at 1.25 GHz
- Low Bit-to-Bit Skew ($t_{sk(O)}$ = 0.06 ns Typical)
- V_{DD} Operating Range: 1.5 V to 2 V
- I_{off} Supports Partial Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

APPLICATIONS

- PCIe Bus Multiplexing and Expansion
- Routing PCI Express Data and/or Display Port Signals
- Notebook PCs
- Desktop PCs
- Servers/Storage Area Networks

RUA PACKAGE (TOP VIEW)



If the exposed center pad is used, it must be connected to ground.

DESCRIPTION/ ORDERING INFORMATION

The TS2PCIE412 is a 4-channel PCIe 2:1 multiplexer/demultiplexer switch that can be used to route one PCIe data lane between two possible destinations or two PCIe data lanes to one destination. Each channel consists of differential pairs of receive (RX) and transmit (TX) signals and operates at a signal-processing bandwidth speed, which supports the PCIe standard of 2.5 Gbps. The device is controlled with one select input (SEL) pin, where SEL controls the data path of the multiplexer/demultiplexer and can be connected to any GPIO in the system. The unselected channel is set in a high-impedance state.

ORDERING INFORMATION

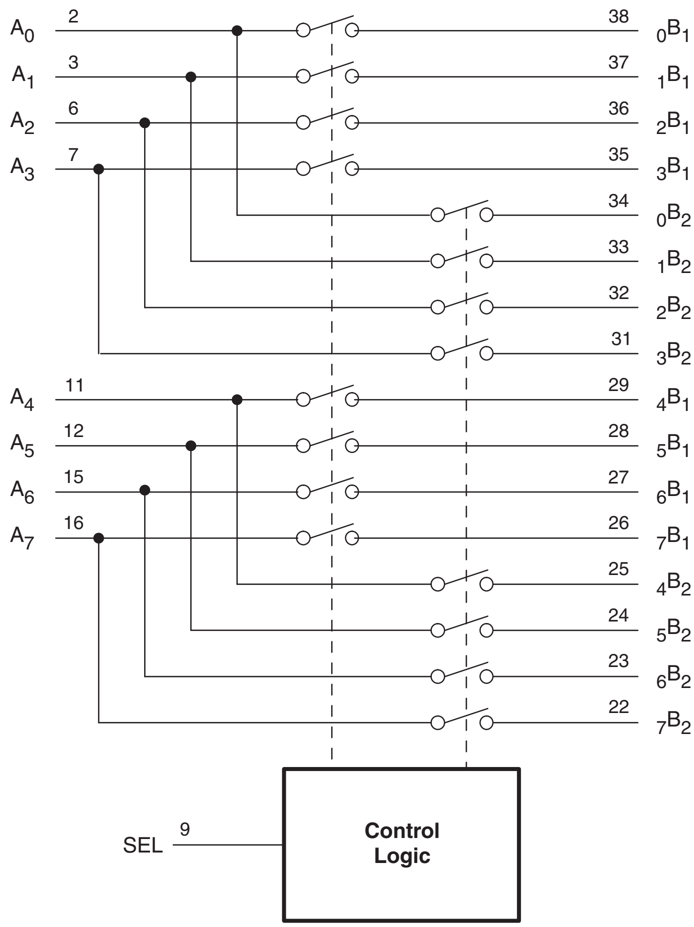
T_A	PACKAGE (1) (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RUA	Tape and reel	TS2PCIE412RUAR	SH412

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTION TABLE

SEL	FUNCTION
L	A_n to ${}_nB_1$
H	A_n to ${}_nB_2$

FUNCTIONAL DIAGRAM



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
A_n,	2, 3, 6, 7, 11, 12, 15, 16	I/O	Data I/Os
${}_nB_m$	22–29, 31–38	I/O	Data I/Os
SEL	9	I	Select input
V_{DD}	5, 8, 13, 18, 20, 30, 40, 42	–	Power supply
GND	1, 4, 10, 14, 17, 19, 21, 39, 41, Exposed center pad	–	Ground

ABSOLUTE MAXIMUM RATINGS[1] [2]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Supply voltage range		–0.5	2.5	V
V_{IN}	Control input voltage range[2] [3]		–0.5	2.5	V
$V_{I/O}$	Switch I/O voltage range[2] [3] [4]		–0.5	2.5	V
I_{IK}	Control input clamp current	V_{IN} < GND		–50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O}$ < GND		–50	mA
$I_{I/O}$	ON-state switch current[5]			100	mA
I_{DD}	Continuous current through V_{DD}			100	mA
I_{GND}	Continuous current through GND			–100	mA
T_{stg}	Storage temperature range.		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND unless otherwise specifed.
(3) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.

PACKAGE THERMAL IMPEDANCE

over operating free-air temperature range (unless otherwise noted)

				UNIT
θ_{JA}	Package thermal impedance[1]	RUA package	51.2	°C/W

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage	1.5	1.8	2	V
V_{IH}	High-level control input voltage (SEL)	$0.65 \times V_{DD}$			V
V_{IL}	Low-level control input voltage (SEL)			$0.35 \times V_{DD}$	V
V_{IO}	Switch input/output voltage	0		V_{DD}	V
T_A	Operating free air temperature	0		85	°C

ELECTRICAL CHARACTERISTICS FOR 1.8-V SUPPLY(1)

V_{DD} = 1.5 V to 2.0 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP(2)	MAX	UNIT
V_{IK}	SEL	V_{DD} = 2.0 V,	I_{IN} = –18 mA			–0.7	–1.3	V
I_{IH}	SEL	V_{DD} = 2.0 V,	$V_{IN} = V_{DD}$				±1	µA
I_{IL}	SEL	V_{DD} =2.0 V,	V_{IN} = GND				±1	µA
I_{off}		V_{DD} = 0,	V_O = 0 to 2 V,	V_I = 0			1	µA
I_{CC}		V_{DD} = 2.0 V,	$I_{I/O}$ = 0,	Switch ON or OFF		200	400	µA
C_{IN}	SEL	f = 10 MHz, V_{IN} = 0 V				1		pF
C_{OFF}	B port	V_I = 0 V, f = 10 MHz,	Outputs open,	Switch OFF		1.5	1.5	pF
C_{ON}		V_I = 0 V, f = 10 MHz,	Outputs open,	Switch ON		4.5	4.5	pF
r_{ON}		V_{DD} = 1.8 V,	GND ≤ V_I ≤ V_{DD},	I_O = –40 mA		12	18	Ω
$r_{ON(flat)}$ (3)		V_{DD} = 1.8 V,	V_I = 1.65 to 1.8 V,	I_O = –40 mA		0.5		Ω
Δr_{ON} (4)		V_{DD} = 1.8 V,	GND ≤ V_I ≤ V_{DD},	I_O = –40 mA		0.2	0.8	Ω
Dynamic								
X_{TALK}		R_L = 100 Ω, f = 10 MHz		See Figure 9		–81		dB
		R_L = 100 Ω, f = 1.25 GHz				–32		
O_{IRR}		R_L = 100 Ω, f = 10 MHz		See Figure 10		–74		dB
		R_L = 100 Ω, f = 1.25 GHz				–36		
BW		R_L = 50 Ω,	See Figure 8			2.1		GHz
Max data rate		R_L = 50 Ω,	See Figure 8			4.2		Gbps

(1) V_I, V_O, I_I, and I_O refer to I/O pins. V_{IN} refers to the control inputs.
(2) All typical values are at V_{DD} = 1.8 V (unless otherwise noted), T_A = 25°C.
(3) $r_{ON(flat)}$ is the difference of r_{ON} in a given channel at specific voltages.
(4) Δr_{ON} is the difference of ron from center ports to any other port.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{DD} = 1.5 V to 2.0 V, R_L = 200 Ω, C_L = 10 pF (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP(1)	MAX	UNIT
t_{pd} (2) (3)	A_n or $_nB_n$	$_nB_n$ or A_n		0.28		ns
t_{PZH}, t_{PZL}	SEL	A_n or $_nB_n$		7.8	9	ns
t_{PHZ}, t_{PLZ}	SEL	A_n or $_nB_n$		2.5	4	ns
$t_{sk(O)}$ (4)	A_n or $_nB_n$	$_nB_n$ or A_n		0.06	0.1	ns
$t_{sk(p)}$ (5) (6)				0.06	0.1	ns

(1) All typical values are at V_{DD} = 1.8 V (unless otherwise noted) T_A = 25°C.
(2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
(3) See Figure 6
(4) Output skew between center port to any other port
(5) Skew between opposite transitions of the same output in a given device $|t_{PHL} – t_{PLH}|$
(6) See Figure 7

TYPICAL PERFORMANCE

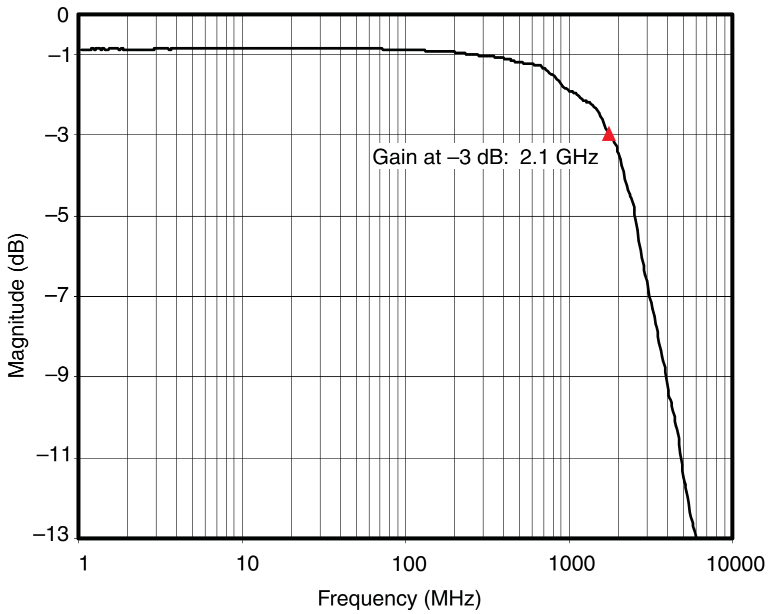


Figure 1. Frequency Response (Insertion Loss)

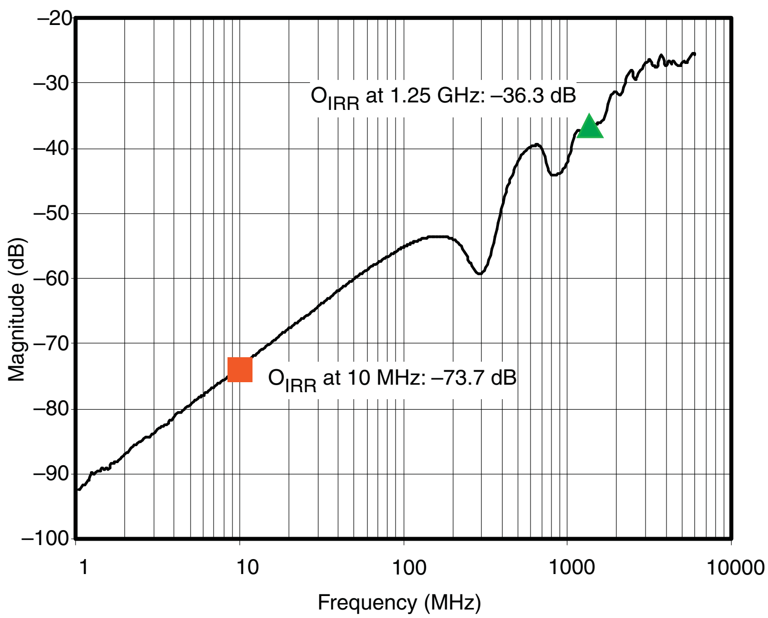


Figure 2. OFF Isolation vs Frequency

TYPICAL PERFORMANCE (continued)

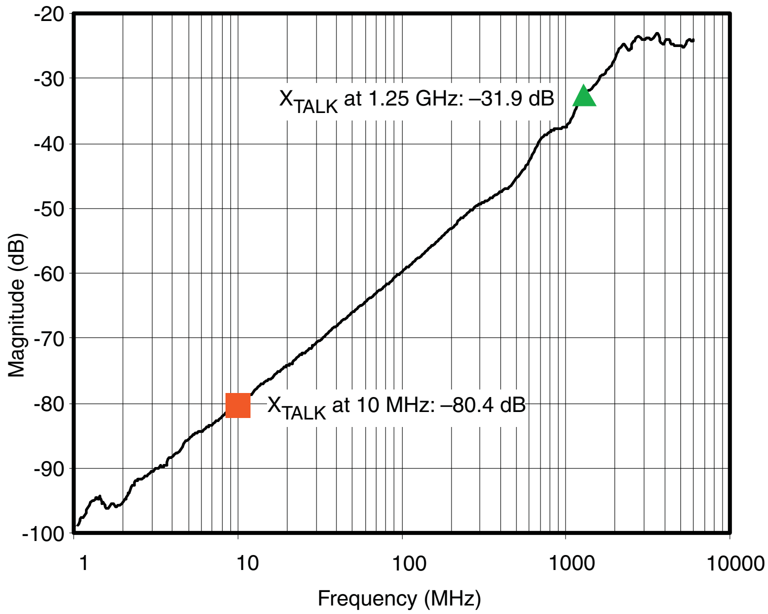


Figure 3. Crosstalk vs Frequency

Eye Diagrams

10-inch trace board for real implementation, V_{DD} = 1.8 V, f = 1.25 GHz, transitional signal and non-transitional signal eye from Tektronix TDS6154C and Tektronix RT-Eye = software

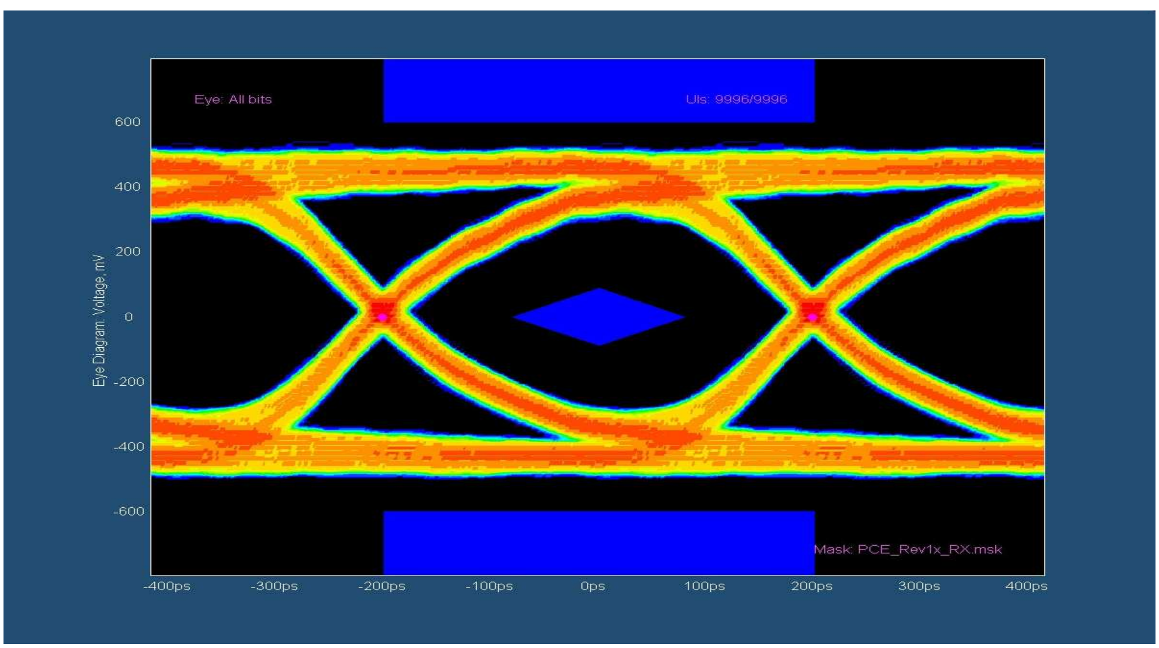


Figure 4. Transitional Signal Eye for TS2PCIE412 Using a 10-inch Trace

TYPICAL PERFORMANCE (continued)

10-inch trace board for real implementation, V_{DD} = 1.8 V, f = 1.25 GHz, transitional signal and non-transitional signal eye from Tektronix TDS6154C and Tektronix RT-Eye = software

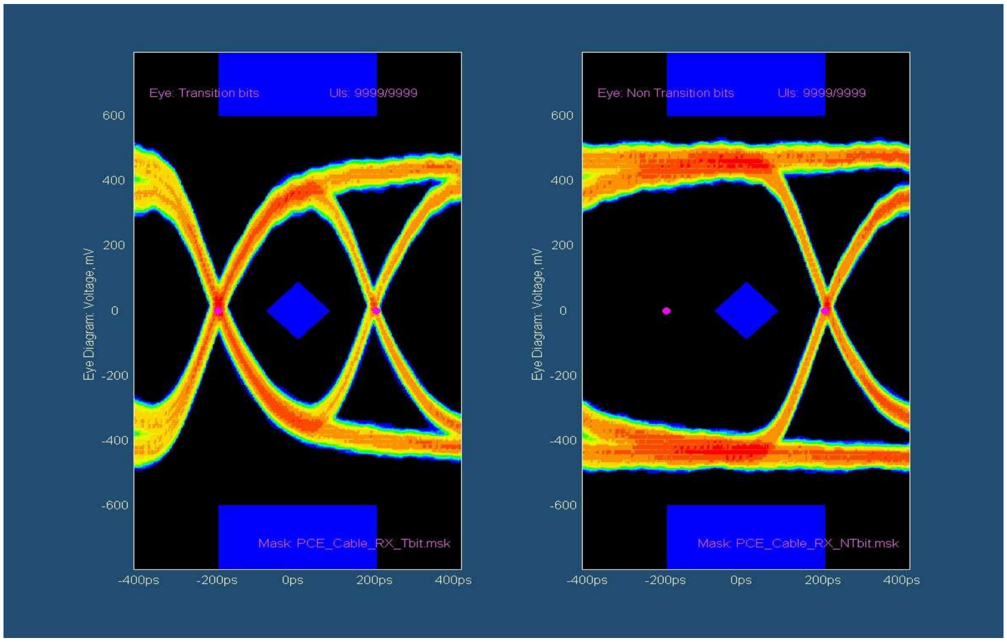
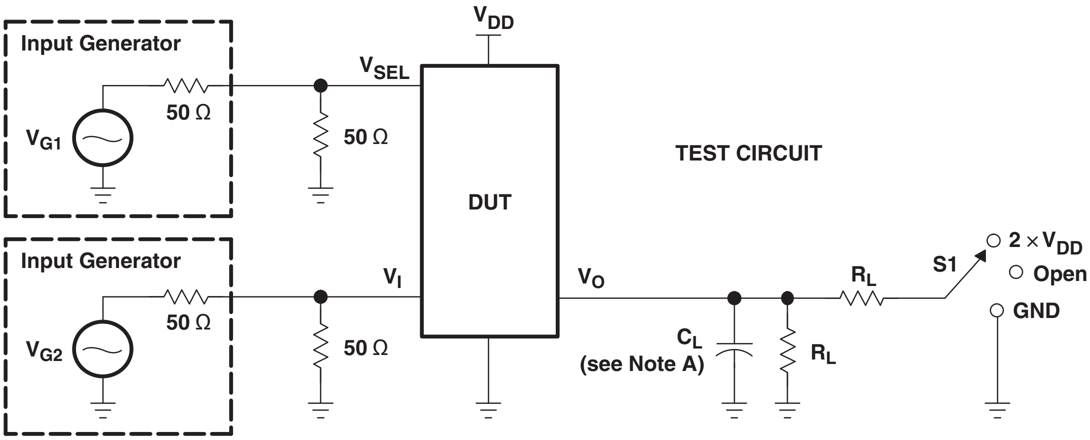
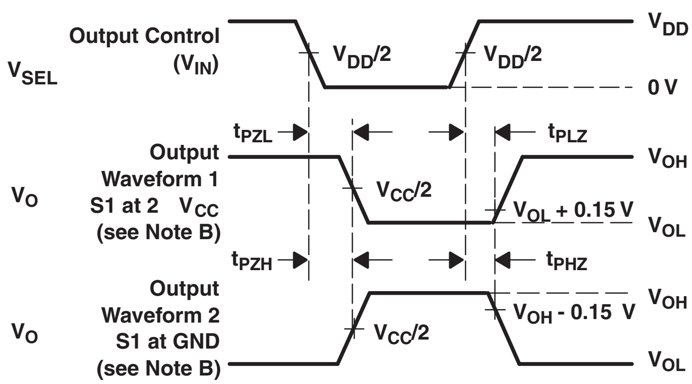


Figure 5. Transitional Signal Eye (Left) and Non-Transitional Signal Eye (Right) for TS2PCIE412 Using a 10-inch Trace

PARAMETER MEASUREMENT INFORMATION (Enable and Disable Times)



TEST	V_{DD}	S1	R_L	V_I	C_L	V_Δ
t_{PLZ}/t_{PZL}	1.5 V to 2 V	2 × V_{DD}	200 Ω	GND	10 pF	0.15 V
t_{PHZ}/t_{PZH}	1.5 V to 2 V	GND	200 Ω	V_{DD}	10 pF	0.15 V



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤2.5 ns.

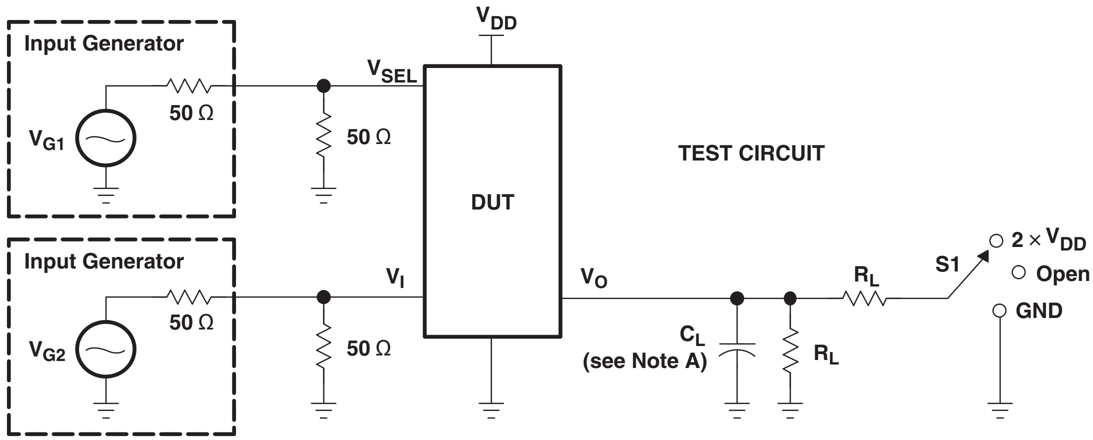
D. The outputs are measured one at a time, with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

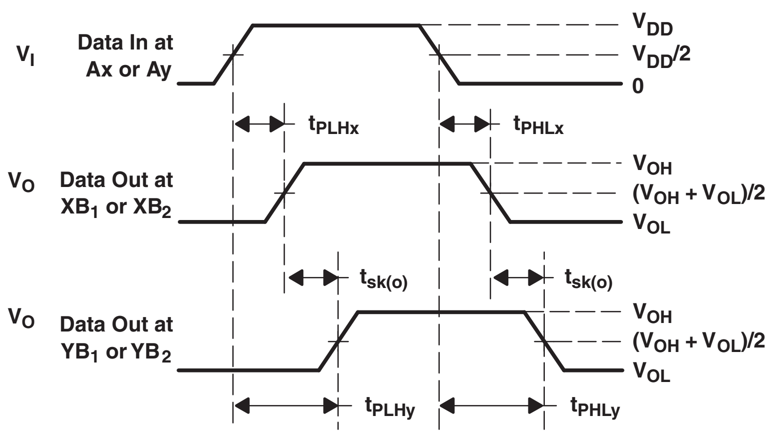
F. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 6. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
(Skew)

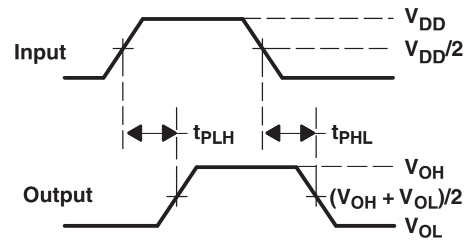


TEST	V_{DD}	S1	R_L	V_{SEL}	C_L
$t_{sk(o)}$	1.5 V to 2 V	Open	200 Ω	V_{DD} or GND	10 pF
$t_{sk(p)}$	1.5 V to 2 V	Open	200 Ω	V_{DD} or GND	10 pF



$t_{sk(o)} = t_{PLHy} - t_{PLHx}$ or $t_{PHLy} - t_{PHLx}$

VOLTAGE WAVEFORMS
OUTPUT SKEW ($t_{sk(o)}$)



$t_{sk(p)} = t_{PHL} - t_{PLH}$

VOLTAGE WAVEFORMS
PULSE SKEW [$t_{sk(p)}$]

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤2.5 ns.

D. The outputs are measured one at a time, with one transition per measurement.

Figure 7. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

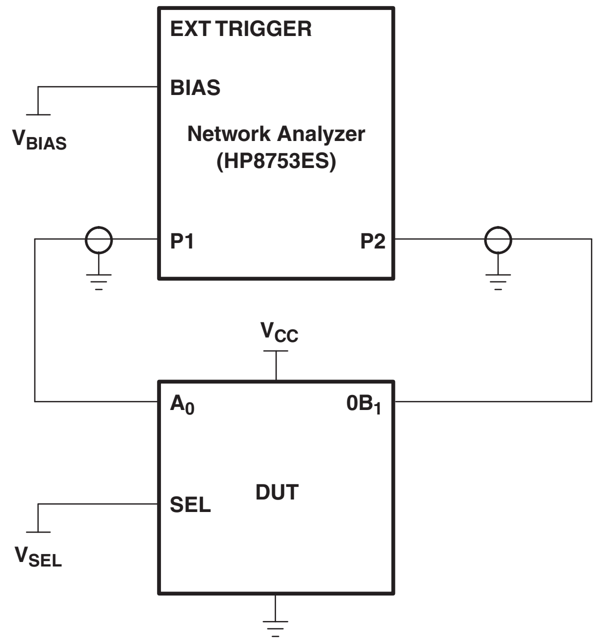


Figure 8. Test Circuit for Frequency Response (BW)

Frequency response is measured at the output of the ON channel. For example, when V_{SEL} = 0 V and A_0 is the input, the output is measured at $0B_1$. All unused analog I/O ports are left open.

HP8753ES Setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

PARAMETER MEASUREMENT INFORMATION (continued)

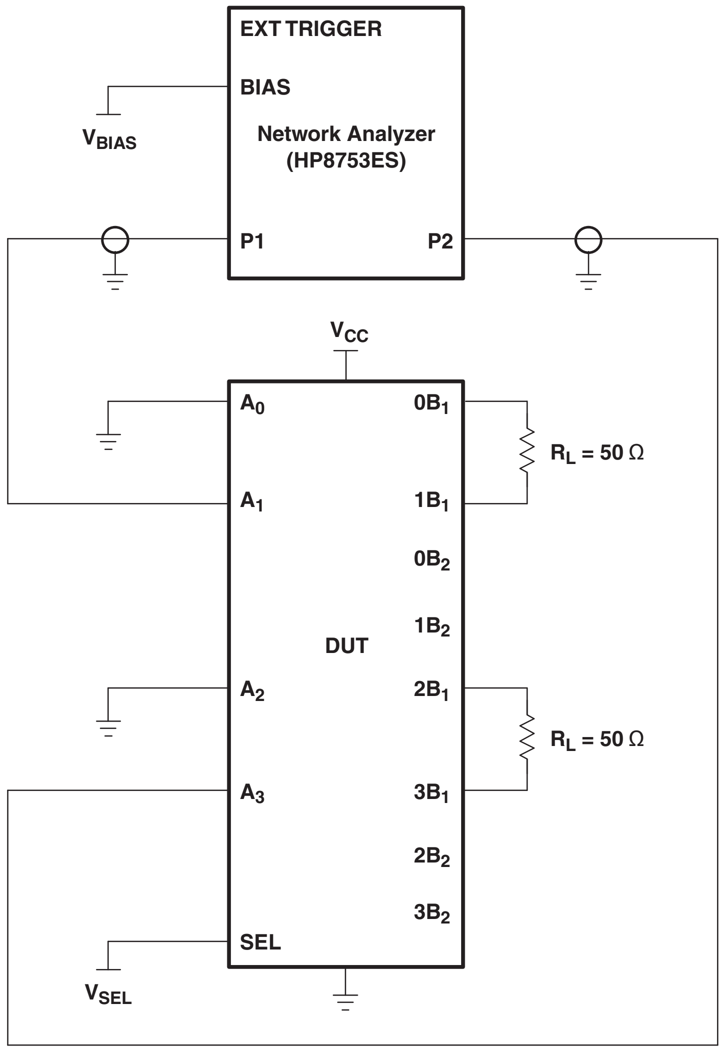


Figure 9. Test Circuit for Crosstalk (X_{TALK})

Crosstalk is measured at the input of the nonadjacent ON channel. For example, when V_{SEL} = 0 V and A_1 is the input, the output is measured at A_3. All unused analog input (A) ports are connected to GND, and output (B) ports are connected to GND through 50-Ω pulldown resistors.

HP8753ES Setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

PARAMETER MEASUREMENT INFORMATION (continued)

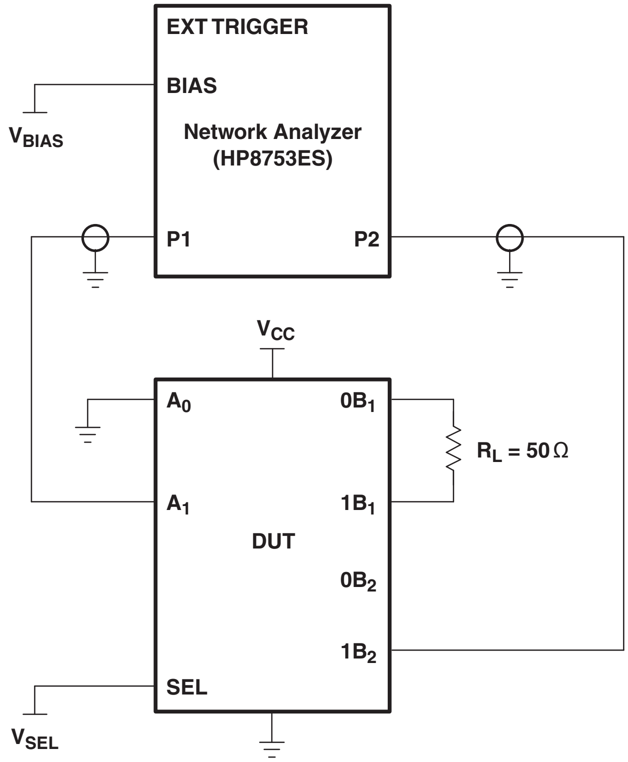


Figure 10. Test Circuit for Off Isolation (O_{IRR})

OFF isolation is measured at the output of the OFF channel. For example, when V_{SEL} = 0 V and A_1 is the input, the output is measured at $1B_2$. All unused analog input (A) ports are left open, and output (B) ports are connected to GND through 50-Ω pulldown resistors.

HP8753ES Setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

查询"TS2PCIE412"供应商

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Pea
TS2PCIE412RUAR	ACTIVE	WQFN	RUA	42	3000	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.t
information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all
lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable fo
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package,
the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retard
in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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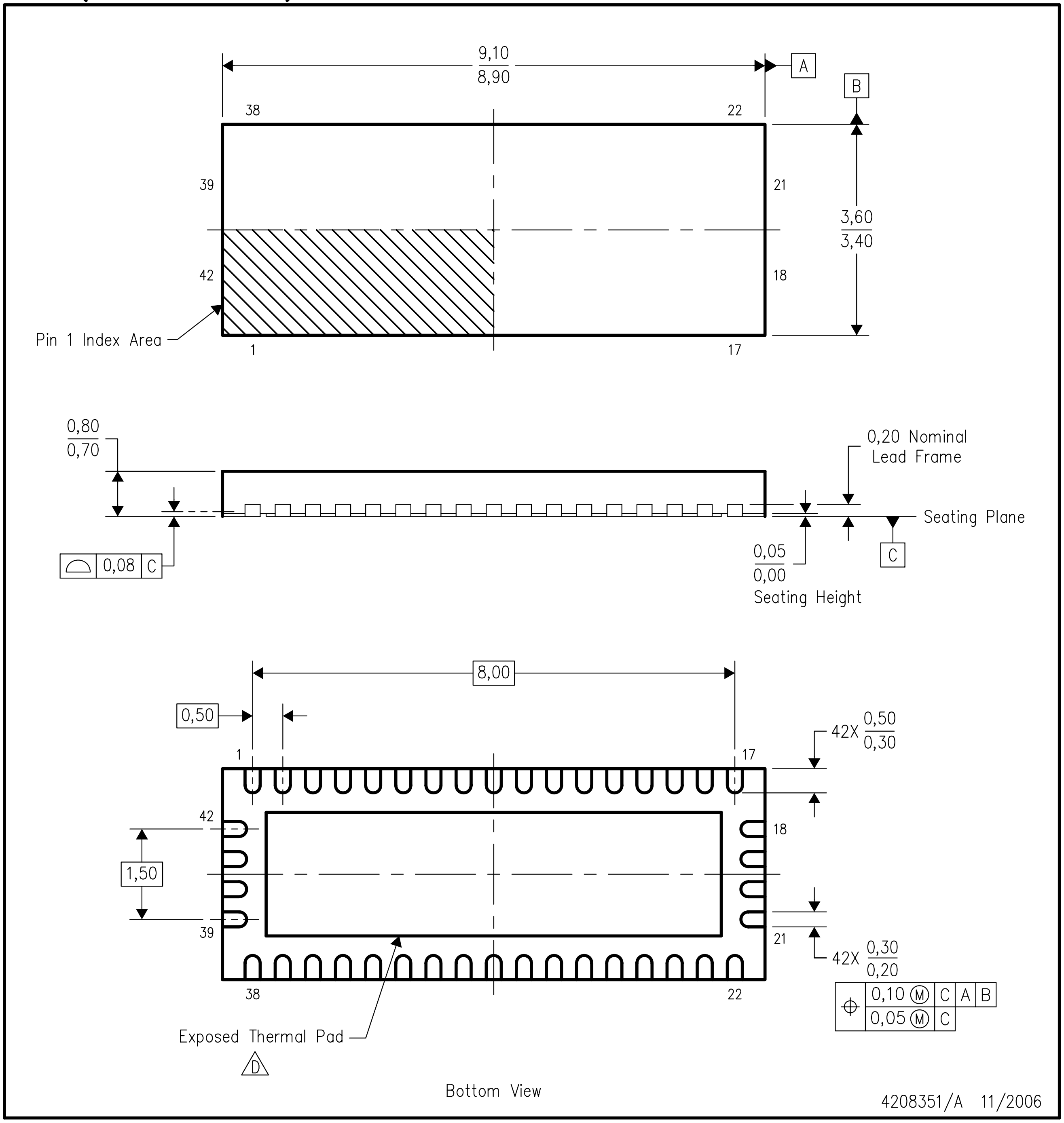
RUA (R-PQFP-N42) PLASTIC QUAD FLATPACK



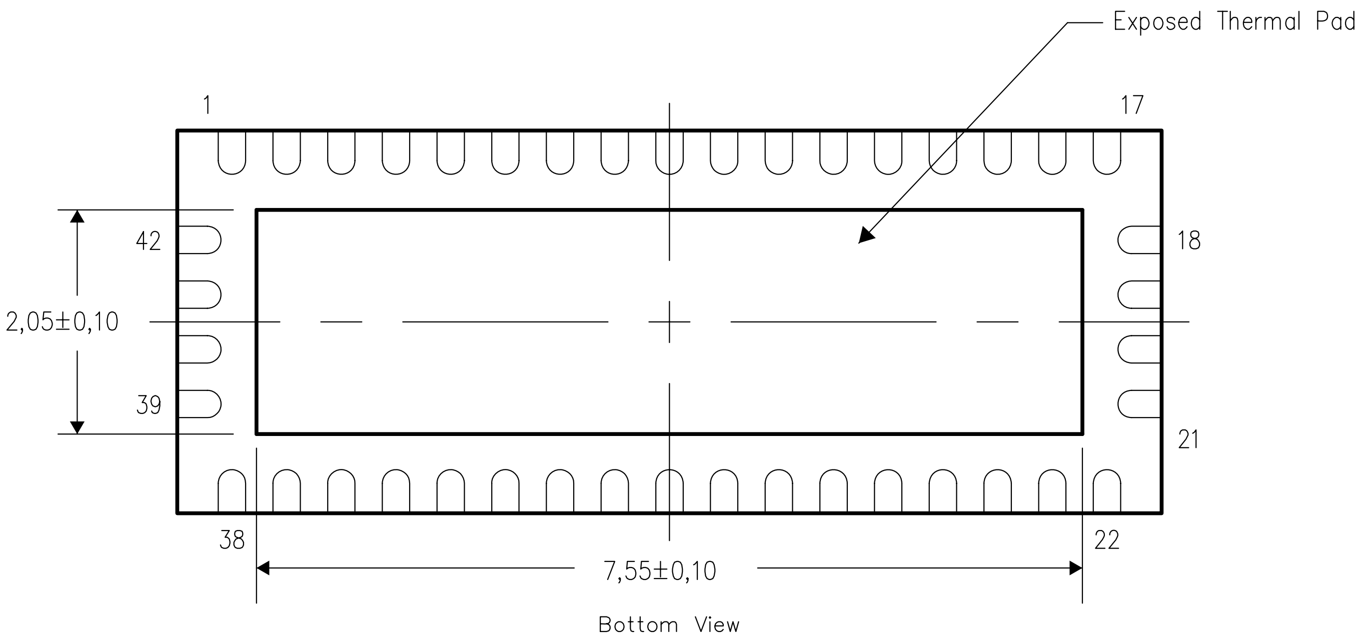
NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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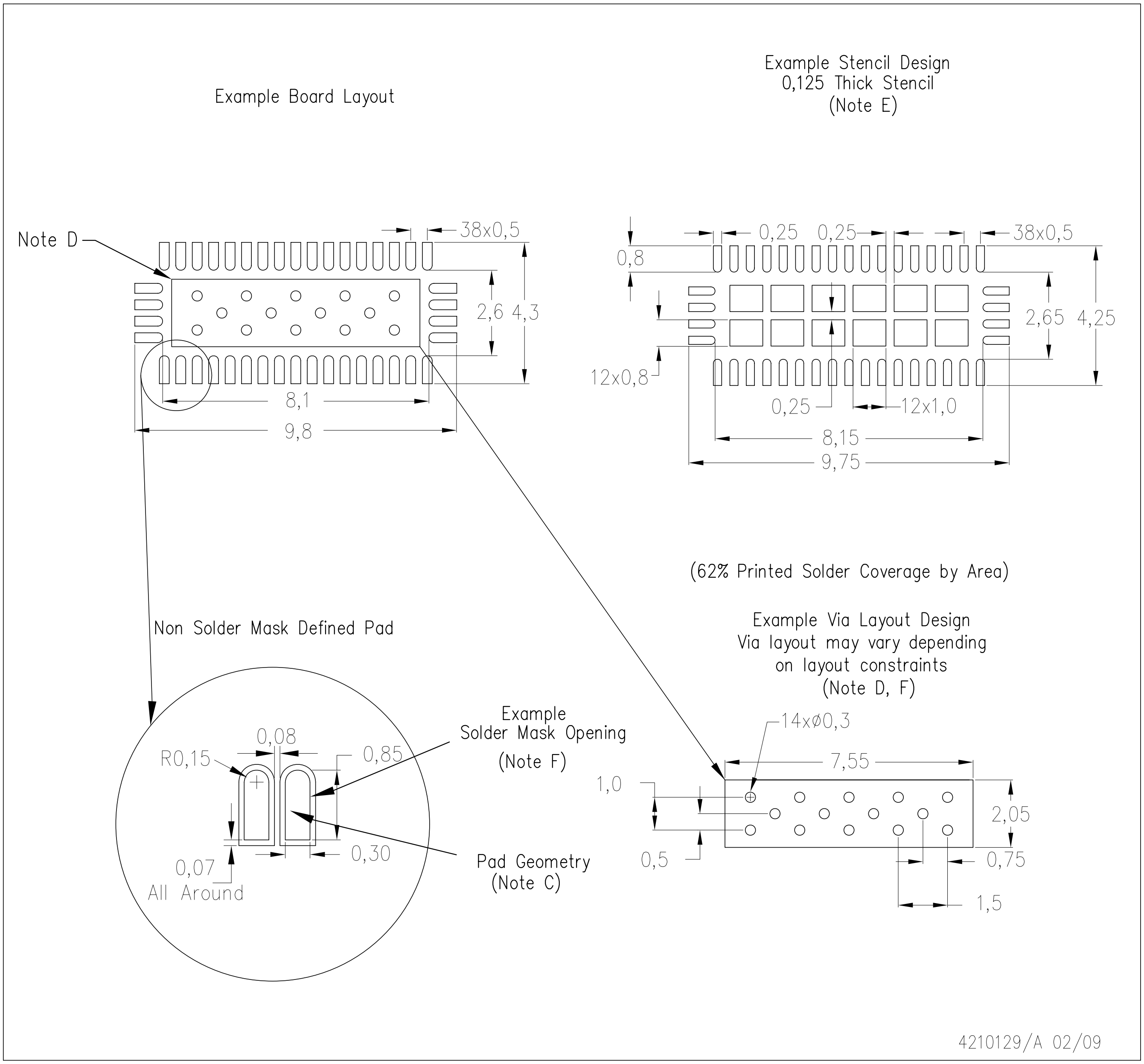
RUA (R–PWQFN–N42)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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