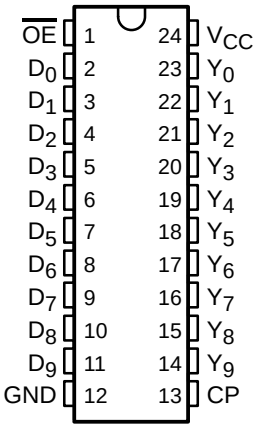
SCCS033A – MAY 1994 – REVISED OCTOBER 2001

- **Function, Pinout, and Drive Compatible With FCT, F Logic, and AM29821**
- **Reduced V_{OH} (Typically = 3.3 V) Version of Equivalent FCT Functions**
- **Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Matched Rise and Fall Times**
- **Fully Compatible With TTL Input and Output Logic Levels**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**
- **64-mA Output Sink Current**
  32-mA Output Source Current
- **High-Speed Parallel Register With Positive-Edge-Triggered D-Type Flip-Flops**

P, Q, OR SO PACKAGE
(TOP VIEW)



description

This bus-interface register is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The CY74FCT821T is a 10-bit-wide buffered version of the popular CY74FCT374 function. This device is ideal for use as an output port requiring high I_{OL}/I_{OH}.

This device is designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. Outputs are designed for low-capacitance bus loading in the high-impedance state.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

PIN DESCRIPTION

NAME	I/O	DESCRIPTION
D	I	D flip-flop data inputs
CP	O	Clock pulse for the register. Enters data into the register on the low-to-high clock transition.
Y	O	Register 3-state outputs
$\overline{OE}$	I	Output control. When $\overline{OE}$ is high, the Y outputs are in the high-impedance state. When $\overline{OE}$ is low, true register data is present at the Y outputs.

SCCS033A – MAY 1994 – REVISED OCTOBER 2001

ORDERING INFORMATION

T_A	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QSOP – Q	Tape and reel	6	CY74FCT821CTQCT	FCT821C
	SOIC – SO	Tube	6	CY74FCT821CTSOC	FCT821C
		Tape and reel	6	CY74FCT821CTSOCT	
	DIP – P	Tube	7.5	CY74FCT821BTPC	CY74FCT821BTPC
	SOIC – SO	Tube	7.5	CY74FCT821BTSOC	FCT821B
		Tape and reel	7.5	CY74FCT821BTSOCT	
	QSOP – Q	Tape and reel	10	CY74FCT821ATQCT	FCT821A
	SOIC – SO	Tube	10	CY74FCT821ATSOC	FCT821A
		Tape and reel	10	CY74FCT821ATSOCT	

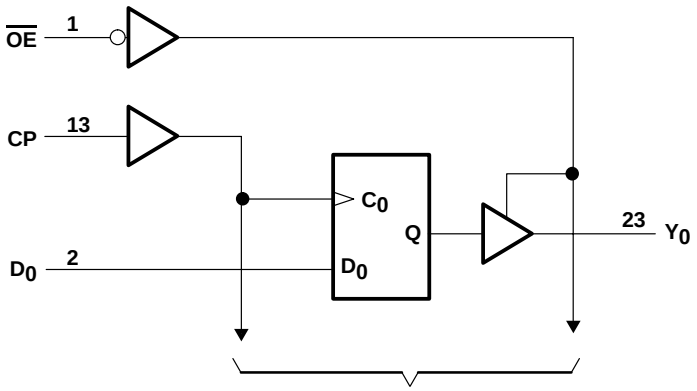
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS			INTERNAL OUTPUTS		FUNCTION
$\overline{OE}$	D	CP	Q	Y	
H	X	↑	L	Z	Z
H	L	↑	L	Z	Load
H	H	↑	H	Z	
L	L	↑	L	L	
L	H	↑	H	H	

H = High logic level, L = Low logic level, X = Don't care,
NC = No change, ↑ = Low-to-high transition,
Z = High-impedance state

logic diagram (positive logic)



absolute maximum rating over operating free-air temperature range (unless otherwise noted)†

Supply voltage range to ground potential . . . . . –0.5 V to 7 V
DC input voltage range . . . . . –0.5 V to 7 V
DC output voltage range . . . . . –0.5 V to 7 V
DC output current (maximum sink current/pin) . . . . . 120 mA
Package thermal impedance, θ_{JA} (see Note 1): P package . . . . . 67°C/W
(see Note 2): Q package . . . . . 61°C/W
(see Note 2): SO package . . . . . 46°C/W
Ambient temperature range with power applied, T_A . . . . . –65°C to 135°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The package thermal impedance is calculated in accordance with JESD 51-3.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–32	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	–40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_{IN} = –18 mA			–0.7	–1.2	V
V_{OH}	V_{CC} = 4.75 V	I_{OH} = –32 mA		2			V
		I_{OH} = –15 mA		2.4	3.3		
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 64 mA			0.3	0.55	V
V_{hys}	All inputs				0.2		V
I_I	V_{CC} = 5.25 V,	V_{IN} = V_{CC}				5	µA
I_{IH}	V_{CC} = 5.25 V,	V_{IN} = 2.7 V				±1	µA
I_{IL}	V_{CC} = 5.25 V,	V_{IN} = 0.5 V				±1	µA
I_{OZH}	V_{CC} = 5.25 V,	V_{OUT} = 2.7 V				10	µA
I_{OZL}	V_{CC} = 5.25 V,	V_{OUT} = 0.5 V				–10	µA
I_{OS}‡	V_{CC} = 5.25 V,	V_{OUT} = 0 V		–60	–120	–225	mA
I_{off}	V_{CC} = 0 V,	V_{OUT} = 4.5 V				±1	µA
I_{CC}	V_{CC} = 5.25 V,	V_{IN} ≤ 0.2 V,	V_{IN} ≥ V_{CC} – 0.2 V		0.1	0.2	mA
ΔI_{CC}	V_{CC} = 5.25 V, V_{IN} = 3.4 V§, f_1 = 0, Outputs open				0.5	2	mA
I_{CCD}¶	V_{CC} = 5.25 V, One bit switching at 50% duty cycle, Outputs open, $\overline{OE}$ = $\overline{EN}$ = GND, V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} – 0.2 V				0.06	0.12	mA/ MHz
I_C#	V_{CC} = 5.25 V, Outputs open, $\overline{OE}$ = $\overline{EN}$ = GND	One bit switching at f_1 = 5 MHz at 50% duty cycle	V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} – 0.2 V		0.7	1.4	mA
			V_{IN} = 3.4 V or GND		1.2	3.4	
		Eight bits switching at f_1 = 2.5 MHz at 50% duty cycle	V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} – 0.2 V		1.6	3.2‖	
			V_{IN} = 3.4 V or GND		3.9	12.2‖	
C_i					5	10	pF
C_o					9	12	pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND

¶ This parameter is derived for use in total power-supply calculations.

$I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

I_C = Total supply current
I_{CC} = Power-supply current with CMOS input levels
ΔI_{CC} = Power-supply current for a TTL high input (V_{IN} = 3.4 V)
D_H = Duty cycle for TTL inputs high
N_T = Number of TTL inputs at D_H
I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)
f_0 = Clock frequency for registered devices, otherwise zero
f_1 = Input signal frequency
N_1 = Number of inputs changing at f_1

All currents are in milliamperes and all frequencies are in megahertz.

‖ Values for these conditions are examples of the I_{CC} formula.

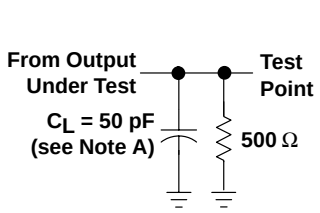
timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER			TEST LOAD	CY74FCT821AT		CY74FCT821BT		CY74FCT821CT		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CP	C_L = 50 pF, R_L = 500 Ω	7		6		6		ns
t_{su}	Setup time, before CP↑	Data	C_L = 50 pF, R_L = 500 Ω	4		3		3		ns
t_h	Hold time, after CP↑	Data	C_L = 50 pF, R_L = 500 Ω	2		1.5		1.5		ns

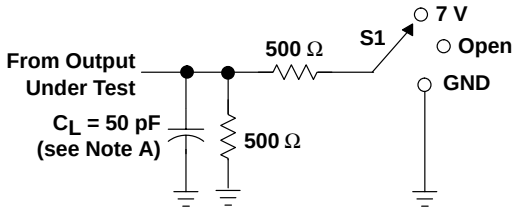
switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST LOAD	CY74FCT821AT		CY74FCT821BT		CY74FCT821CT		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	CP	Y	C_L = 50 pF, R_L = 500 Ω		10		7.5		6	ns
t_{PHL}					10		7.5		6	
t_{PLH}	CP	Y	C_L = 300 pF, R_L = 500 Ω		20		15		12.5	ns
t_{PHL}					20		15		12.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF, R_L = 500 Ω		12		8		7	ns
t_{PZL}					12		8		7	
t_{PZH}	$\overline{OE}$	Y	C_L = 300 pF, R_L = 500 Ω		23		15		12.5	ns
t_{PZL}					23		15		12.5	
t_{PHZ}	$\overline{OE}$	Y	C_L = 5 pF, R_L = 500 Ω		7		6.5		6	ns
t_{PLZ}					7		6.5		6	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF, R_L = 500 Ω		8		7.5		6.5	ns
t_{PLZ}					8		7.5		6.5	

PARAMETER MEASUREMENT INFORMATION

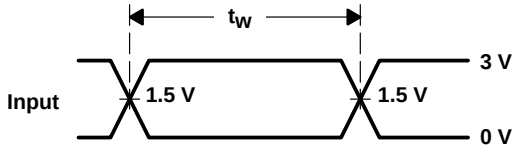


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

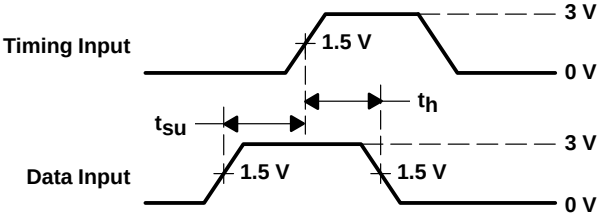


LOAD CIRCUIT FOR
3-STATE OUTPUTS

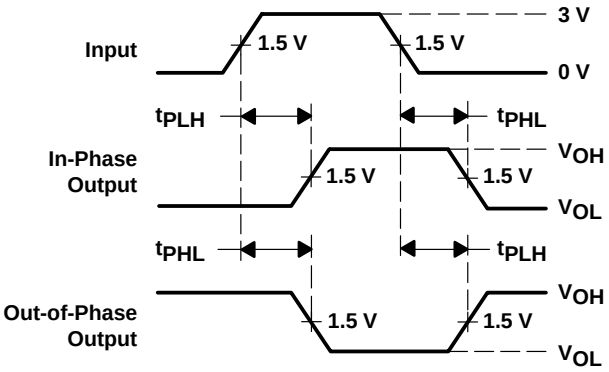
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



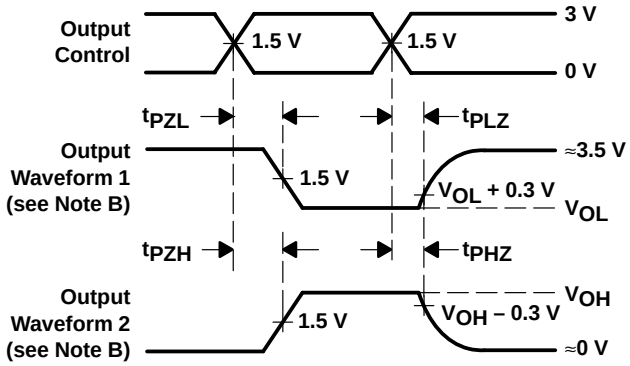
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265