57C401/13 57C402/23 57C4033

Military CMOS Zero Power FIFOs

64x4, 64x5 Memory, 12 MHz (Cascadable)

Conforms to MIL-STD-883, Class B (Latest Revision)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Zero standby power**
- **High-speed 12 MHz shift-in/shift-out data rates**
- **Very low active power consumption**
- **Choice of 4-bit or 5-bit data width**
- **TTL-compatible inputs and outputs**
- **Readily expandable in word width and depth**
- **RAM-based architecture for short fall-through delay**
- **Full CMOS 8-transistor cell for maximum noise immunity**
- **Asynchronous operation**
- **Output Enable feature (57C4013/23/33)**

GENERAL DESCRIPTION

The 57C40X/XX series devices are high-performance CMOS RAM-based First-In First-Out buffer memory products organized as 64 words by 4 or 5 bits wide. These devices use Advanced Micro Devices' CMOS process technology and meet the demands for high-reliability, high-speed, low-power operation. By utilizing an on-chip, dual-port RAM, a very short fall-through time is realized, improving overall system performance. Separate on-chip Read and Write pointers address each memory location, allowing the data to propagate to the outputs in much less time than in traditional register-based FIFOs. These FIFOs are easily integrated into many applications and perform particularly well in high-speed disk controllers, graphics, and communication systems. The 550 µwatt standby power of these devices makes them ideal for ultra-low-powered and battery-powered systems.

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CONNECTION DIAGRAMS

For Ceramic DIP Packages

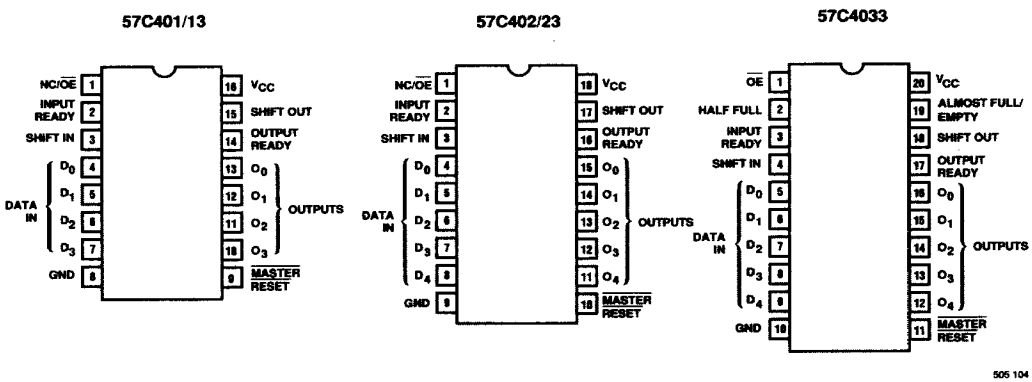


Figure 1.

Publication #	Rev.	Amendment
11710	A	/0

Issue Date: February 1989

ORDERING INFORMATION

57 C 401 3 –12 J /883B

TEMPERATURE CODE
57 = –55°C to 125°C

CMOS FIFO FAMILY

PART NUMBER

OUTPUT TYPE
Blank = Totem Pole
3 = Three State

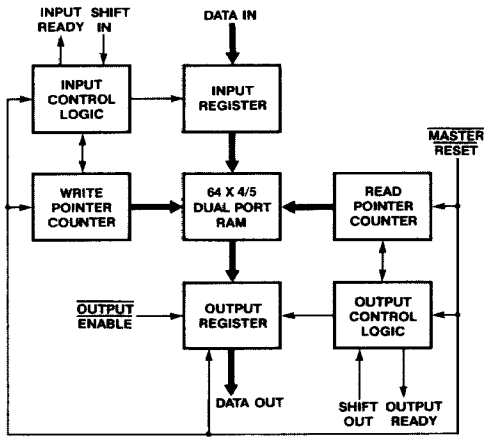
SPEED
(MHz)

PACKAGE
J = 57C401-12 - CD 016
J = 57C401-13 - CD 016
J = 57C402-12 - CD 018
J = 57C4023-12 - CD 018
J = 57C4033-12 - CD 020

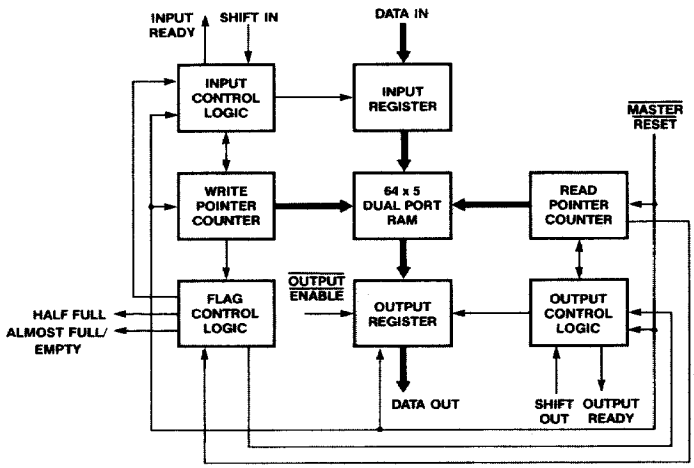
PROCESSING
/883B = MIL-STD-883, Class B

BLOCK DIAGRAMS

57C401/13 57C402/23



57C4033



ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC} ..... -0.5 V to +7.0 V
Input voltage range ..... -1.5 V to +7.0 V
Off-state output voltage ..... -0.5 V to +6.0 V
Storage temperature ..... -65°C to +150°C

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability. Absolute maximum ratings are for system design reference; parameters given are not tested.

OPERATING CONDITIONS

Symbol	Parameter	Figure	Min	Max	Unit
V_{CC}	Supply Voltage		4.5	5.5	V
t_{SIH}	Shift-In HIGH Time	1	16		ns
t_{SIL}	Shift-In LOW Time	1	25		ns
t_{IDS}	Input Data Setup to SI (Shift In)	1	0		ns
t_{IDH}	Input Data Hold Time to SI (Shift In)	1	40		ns
t_{RIDS}	Input Data Setup to IR (Input Ready)	3	0		ns
t_{RIDH}	Input Data Hold Time to IR (Input Ready)	3	30		ns
f_{IN}	Shift-In Rate	1	12		MHz
f_{OUT}	Shift-Out Rate	4	12		MHz
t_{SOH}	Shift-Out HIGH Time	4	27		ns
t_{SOL}	Shift-Out LOW Time	4	25		ns
t_{MRW}**	Master Reset Pulse	8	45		ns
t_{MRS}***	Master Reset to SI	8	75		ns
V_{IL}*	Low Level Input Voltage			0.8	V
V_{IH}*	High Level Input Voltage		2.0		V
T_A†	Operating Temperature		–55	125	°C

* V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

** If the FIFO is not full (IR HIGH) $\overline{MR}$ LOW forces IR LOW, followed by IR returning high when $\overline{MR}$ goes high.

*** t_{MRS} is measured on initial characterization lots only and is not directly tested in production.

† Instant-On Case Temperature.

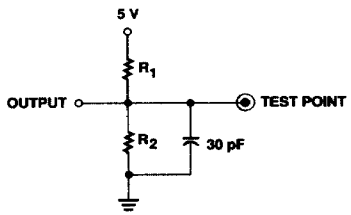
Conforms to MIL-STD-883; Group A, Subgroups 1, 2, and 3.

DC CHARACTERISTICS over Operating Conditions

Symbol	Parameter	Test Conditions		Min	Max	Unit
I_{IN}	Input Current	V_{CC} = MAX	0 V<V_{IN} <5.5 V	–1	1	µA
V_{OL}	Low-Level Output Voltage	V_{CC} = MIN	I_{OL} = 20 µA		0.1	V
			I_{OL} = 8 mA		0.4	
V_{OH}	High-Level Output Voltage	V_{CC} = MIN	I_{OH} = –20 µA	V_{CC}–0.1		V
			I_{OH} = –4 mA	2.4		
I_{OZ}	Off-State Output Current ('4013, '4023, '4033 devices)	V_{CC} = MAX	0 V≤V_{OUT}≤5.5 V	-5	5	µA
I_{OS}*	Output Short-Circuit Current	V_{CC} = MAX	V_O = 0 V	–20	–90	mA
I_{CC}op**	Maximum Operating Current	V_{CC} = MAX, All outputs open, f = 12 MHz			40	mA
I_{CC}stby	Maximum Standby Current ("CZ" devices only)	V_{CC} = MAX, All outputs open.			100	µA

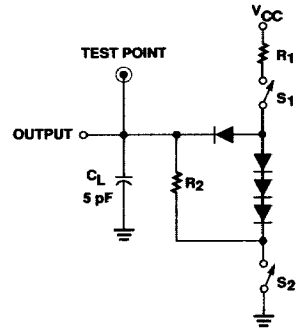
* No more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
** Tested on initial qualification lot only .

STANDARD TEST LOAD*



Input Pulse Amplitude = 3 V
Input Rise and Fall Time (10% – 90%) = 2.5 ns
Measurement made at 1.5 V

THREE STATE TEST LOAD*



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*Equivalent test load may be used for automatic testing.

RESISTOR VALUES

I_{OL}	R_1	R_2
8 mA	600 Ω	1200 Ω

Conforms to MIL-STD-883; Group A, Subgroups 9, 10, and 11.

SWITCHING CHARACTERISTICS

Symbol	Parameter	Figure	Min	Max	Unit
t_{IRL}†	Shift In ↑ to Input Ready LOW	1		70	ns
t_{IRH}†	Shift In ↓ to Input Ready HIGH	1		65	ns
t_{ORL}†	Shift Out ↑ to Output Ready LOW	4		65	ns
t_{ORH}†	Shift Out ↓ to Output Ready HIGH	4		60	ns
t_{ODH}†	Output Data Hold (previous word)	4	5		ns
t_{ODS}	Output Data Shift (next word)	4		40	ns
t_{PT}	Data Throughput	3,6		110	ns
t_{MRORL}	Master Reset ↓ to Output Ready LOW	8		120	ns
t_{MRIRH}*	Master Reset ↑ to Input Ready HIGH	8		120	ns
t_{MRO}	Master Reset ↓ to Outputs LOW	8		45	ns
t_{MRHFL}	Master Reset ↓ to Half-Full Flag LOW ('4033 only)	9		120	ns
t_{MRAEH}	Master Reset ↓ to Almost Empty Flag HIGH ('4033 only)	9		120	ns
t_{IPH}	Input Ready Pulse HIGH	3	12		ns
t_{OPH}	Output Ready Pulse HIGH	6	10		ns
t_{ORD}	Output Ready ↑ to Data Valid	4		0	ns
t_{AEH}	Shift Out ↑ to AF/E High ('4033 only)	10		125	ns
t_{AEL}	Shift In ↑ to AF/E LOW ('4033 only)	10		125	ns
t_{AFL}	Shift Out ↑ to AF/E LOW ('4033 only)	11		125	ns
t_{AFH}	Shift In ↑ to AF/E HIGH ('4033 only)	11		125	ns
t_{HFH}	Shift In ↑ to HF HIGH ('4033 only)	12		125	ns
t_{HFL}	Shift Out ↑ to HF LOW ('4033 only)	12		125	ns
t_{PHZ}**	Output Disable Delay ('4013, '4023, '4033 devices only)	A		30	ns
t_{PLZ}**				30	
t_{PZL}	Output Enable Delay ('4013, '4023, '4033 devices only)	A		35	ns
t_{PZH}				35	

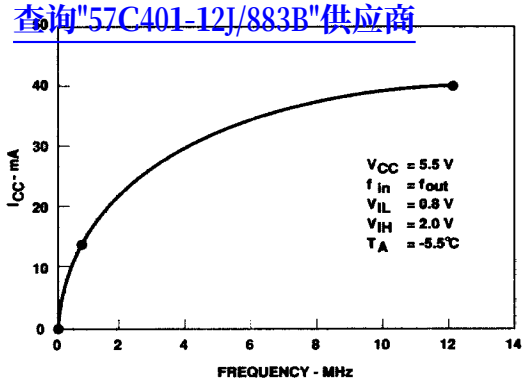
* If the FIFO is not full (IR HIGH), $\overline{MR}$ LOW forces IR LOW, followed by IR returning high when $\overline{MR}$ goes high.
** Actual test limits may be different to compensate for ATE.
† See timing diagram for explanation of parameters

CAPACITANCES*

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 4.5 V		10	pF
C_{OUT}	Output Capacitance			7	pF

* These parameters are not tested in production but are evaluated at initial characterization and anytime the design is modified where capacitance may be affected.

I_{CC} vs. FREQUENCY



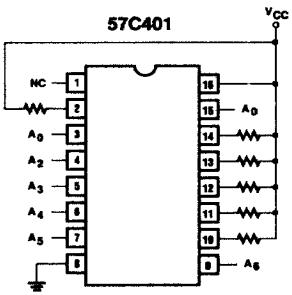
MILITARY CASE OUTLINES

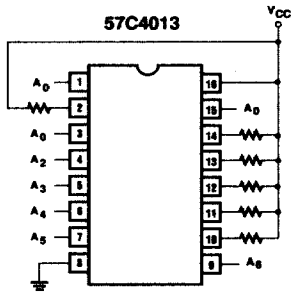
Device	Package	
	J (Cerdip)	
	Package Outline	Conforms to MIL-M-38510 Appendix C Case
57C401	16J	D-2
57C4013	16J	D-2
57C402	18J	D-6
57C4023	18J	D-6
57C4033	20J	D-8

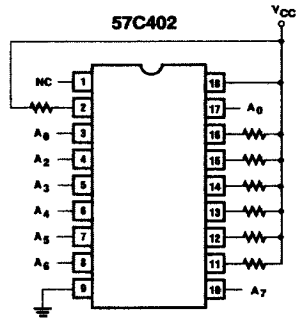
MILITARY BURN-IN

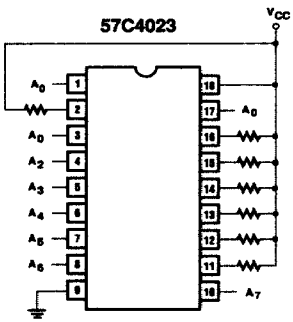
Military burn-in is in accordance with the current revision of MIL-STD-833, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

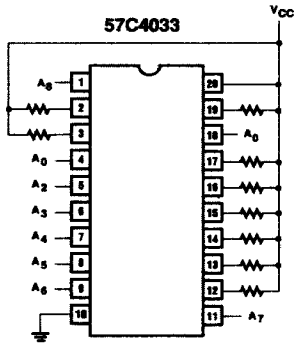
DYNAMIC BURN-IN CIRCUITRY







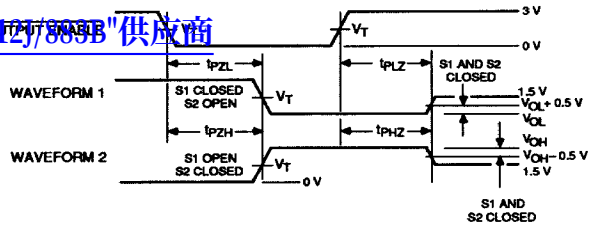




$T_{ambient}$ = 125°C
V_{CC} = 5.25 ± 0.25 V
Square wave pulses on A_0 to A_8 are:

1. 50% ± 15% duty cycle
2. Logic "0" = –1 V to 0.7 V
3. Logic "1" = 2.4 V to V_{CC}
4. Frequency of each address is to be one-half of each preceding input, with A_0 beginning at 100 kHz.

   e.g., A_0 = 100 kHz
   A_1 = 50 kHz ± 10%
   A_2 = 25 kHz ± 10%
   A_n = 1/2 A_{n-1} ±10%, etc.



Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

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Figure A. Enable and Disable (57C4013/23/33 Only)

FUNCTIONAL DESCRIPTION

Data Input

The FIFO consists of a dual-port RAM and two ring counters for read and write. After power-up, the Master Reset should be pulsed LOW, which internally resets both the read and write counters. When the Input Ready (IR) is HIGH, the FIFO is ready to accept DATA from the D_x inputs. Data then present at the inputs is written into the first location of the RAM when Shift-In (SI) is brought HIGH. An SI HIGH signal causes the IR to go LOW. When the SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. The write pointer now points to the next location in the RAM. If the memory is full, then IR will remain LOW.

Data Output

Data is read from the O_x outputs. Just after the first shift-in, the first data word is available at the outputs, which is indicated by the Output Ready (OR) going HIGH. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the read pointer to point to the next location in the RAM, and also the OR to go LOW. Valid data is maintained while the SO is HIGH. When the SO is brought LOW, the OR goes HIGH, indicating the presence of new valid data. If the FIFO is emptied, OR stays LOW and O_x remains as before, (i.e., data does not change if the FIFO is empty). A dual port RAM inside the chip provides the capability of simultaneous and asynchronous writes (Shift-Ins) and reads (Shift-outs).

AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1 µF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input-Ready combination, as well as the Shift-Out-Output-Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input Ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time (t_{IDH}) and the next activity of Input Ready (t_{IRL}) to be extended relative to Shift-In going HIGH. This same type of situation occurs with t_{IRH}, t_{ORL}, t_{ORH}, and the Status Flag timing as related to Shift-In and Shift-Out. For high-speed applications, proper grounding technique is essential.

HF AND AF/AE STATUS FLAGS (57C4033 Only)

The Half-Full (HF) will be high only when the net balance of words shifted into the FIFO exceeds the number of words shifted out by thirty-two or more (i.e., when the FIFO contains thirty-two or more words). The Almost-Full/Empty (AF/AE) flag will be HIGH when the FIFO contains fifty-six or more words or when the FIFO contains eight or fewer words (see Figures 10, 11 and 12).

Care should be exercised in using the status flags because they are capable of producing arbitrarily short pulses. For example, if the FIFO contains thirty-one words, and SI and SO pulses are applied simultaneously, the HF flag may produce an arbitrarily short pulse, depending on the precise phase of SI and SO.

The flags will always settle to the correct state after the appropriate delay (e.g., t_{HFL}, t_{HFH} in this example). This property of the status flags will clearly be a function of dynamic relation between SI and SO. Generally, the use of level-sensitive, rather than edge-sensitive status detection circuits will alleviate this hazard.

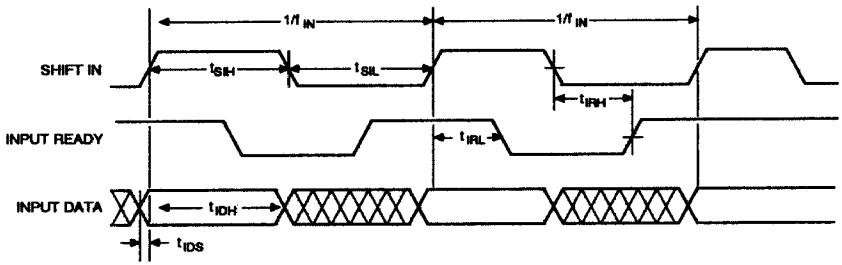
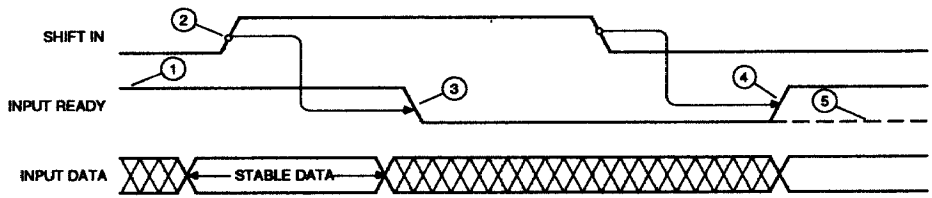


Figure 1. Input Timing



① Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.

② Input Data is loaded into the first available memory location.

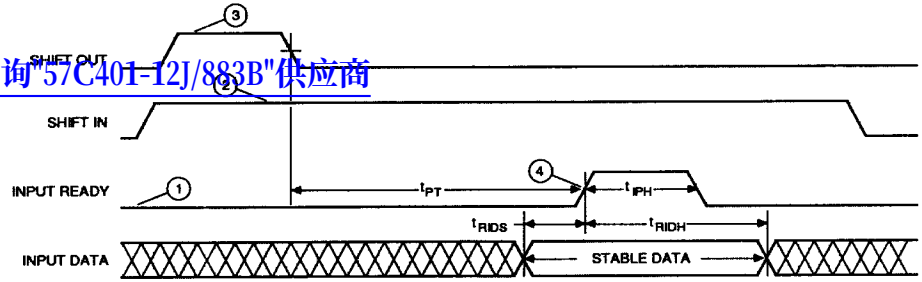
③ Input Ready goes LOW indicating this memory location is full.

④ Shift-In going LOW allows Input Ready to sense the status of the next memory location. The next memory location is empty as indicated by Input Ready HIGH.

⑤ If the FIFO is already full, then the Input Ready remains low.

Note: Shift-In pulses applied while Input Ready is LOW will be ignored.

Figure 2. The Mechanism of Shifting Data Into the FIFO



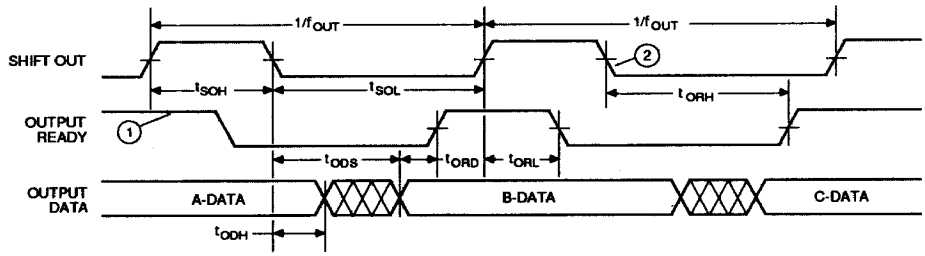
① FIFO is initially full.

② Shift In is held HIGH.

③ Shift Out pulse is applied. An empty location is detected by the internal pointers on the falling edge of SO.

④ As soon as Input Ready becomes HIGH the Input Data is loaded into this location.

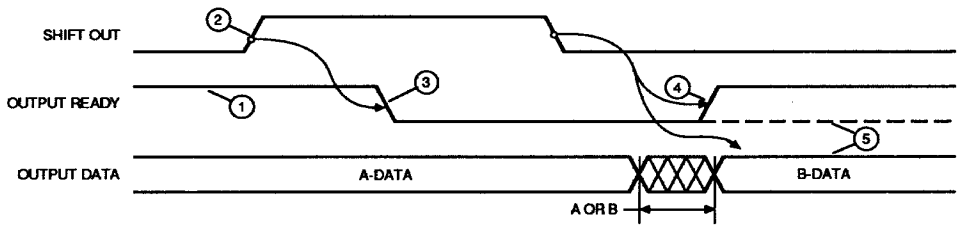
Figure 3. Data Is Shifted In Whenever Shift In and Input Ready Are Both HIGH



① The diagram assumes that the FIFO contains at least three words: A-Data (first input word), B-Data (second input word), and C-Data (third input word).

② Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e., OR and SO are both high together.

Figure 4. Ouput Timing



① Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.

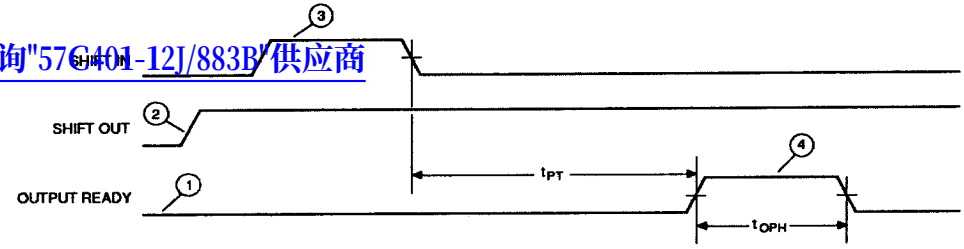
② Shift-Out goes HIGH causing (B-Data (second input word) to advance to the output register
Output data remains as valid A-Data while Shift-Out is HIGH.

③ Output Ready goes LOW.

④ Shift-Out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.

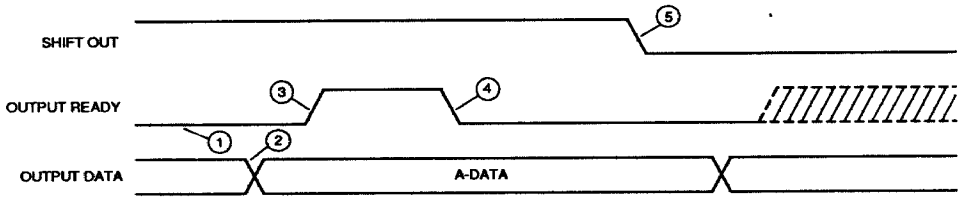
⑤ If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data remains the same (A-Data).

Figure 5. The Mechanism of Shifting Data Out of the FIFO



① FIFO is initially empty.
② Shift Out is held HIGH.
③ Shift-In pulse applied. A full location is detected by the internal pointers on the falling edge of Shift-In.
④ As soon as Output Ready becomes HIGH, the word is shifted out.

Figure 6. t_{PT} and t_{OPH} Specification



① The internal logic does not detect the presence of any data in the FIFO.
② New data (A) arrives at the outputs.
③ Output Ready goes HIGH indicating arrival of the new data.
④ Since Shift Out is held HIGH, Output Ready goes immediately LOW.
⑤ As soon as Shift Out goes LOW the Output Data is subject to change.
Output Ready will go HIGH or LOW depending on whether there are any additional upstream words in the FIFO.

Figure 7. Data Is Shifted Out Whenever Shift Out and Output Ready Are Both HIGH

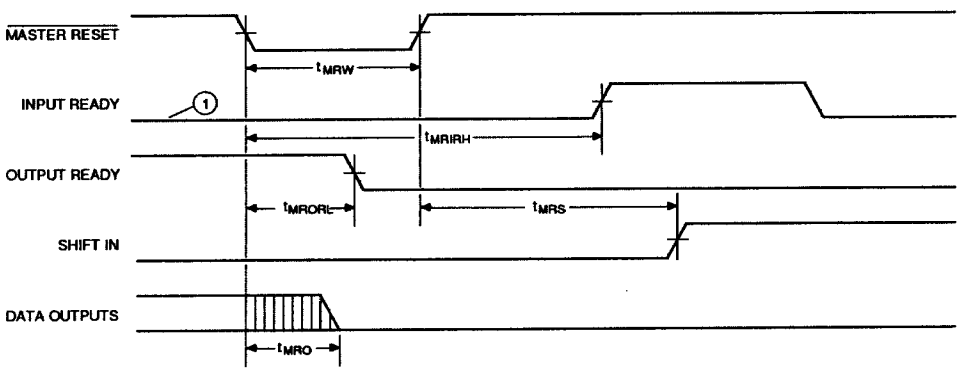
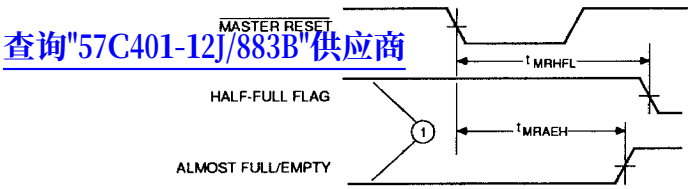
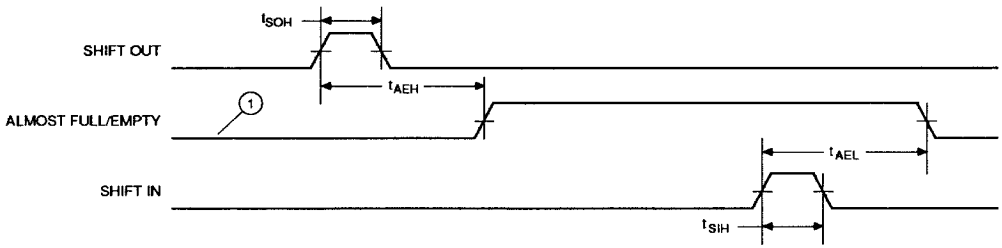


Figure 8. Master Reset Timing



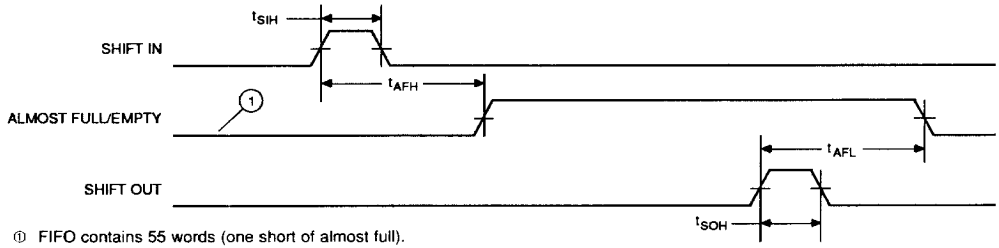
① FIFO initially has between 32 and 56 words.

Figure 9. t_{MRHFL} and t_{MRAEH} Specifications



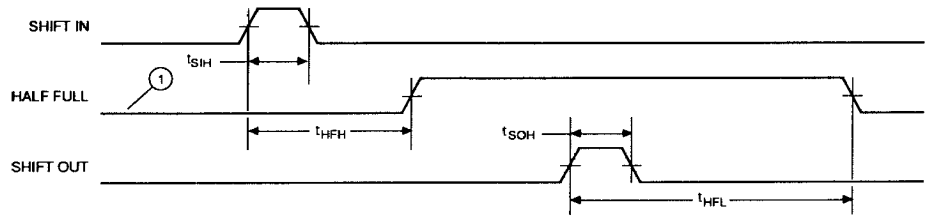
① FIFO contains 9 words (one more than almost empty).

Figure 10. t_{AEH} and t_{AEL} Specifications



① FIFO contains 55 words (one short of almost full).

Figure 11. t_{AFH} and t_{AFL} Specifications

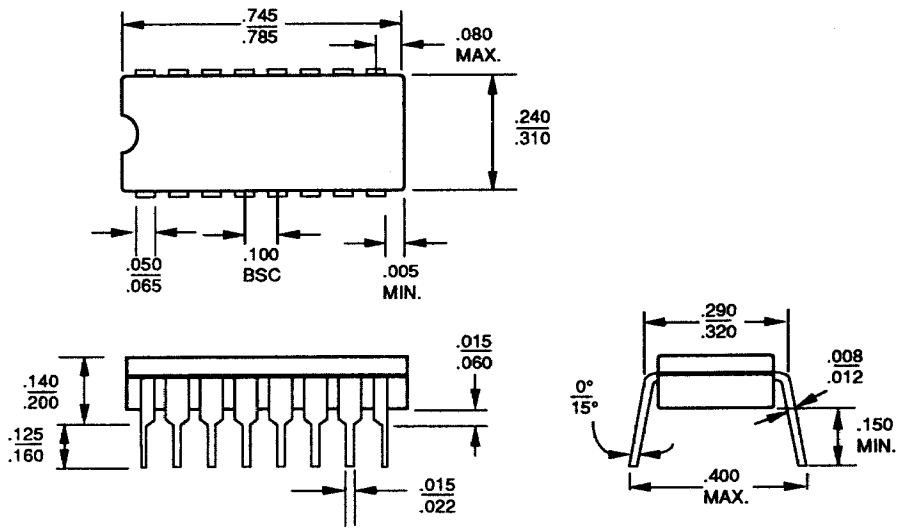


① FIFO contains 31 words (one short of almost full).

Figure 12. t_{HFL} and t_{HFH} Specifications

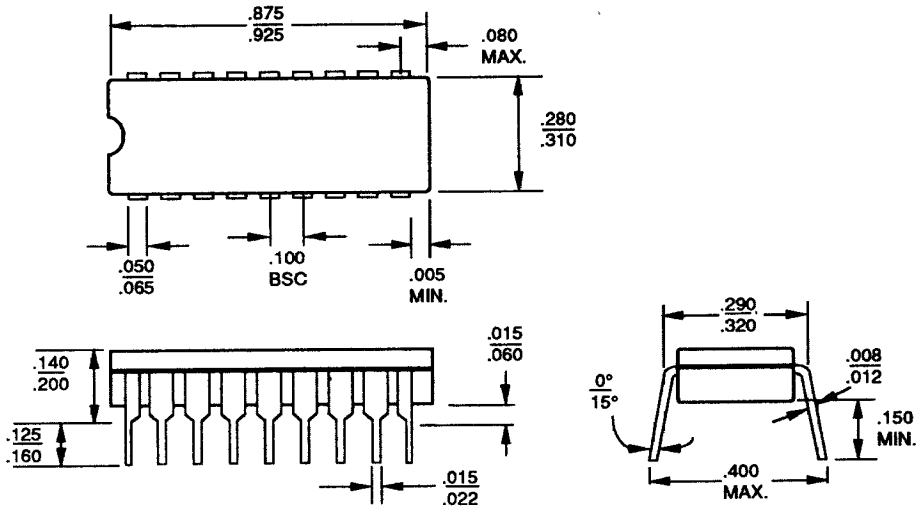
PHYSICAL DIMENSIONS*

CD 016



PID# 07319B

CD 018



07803C

* For reference only. All dimensions are measured in inches. BSC is an ANSI standard for Basic Space Centering.