

## General Description

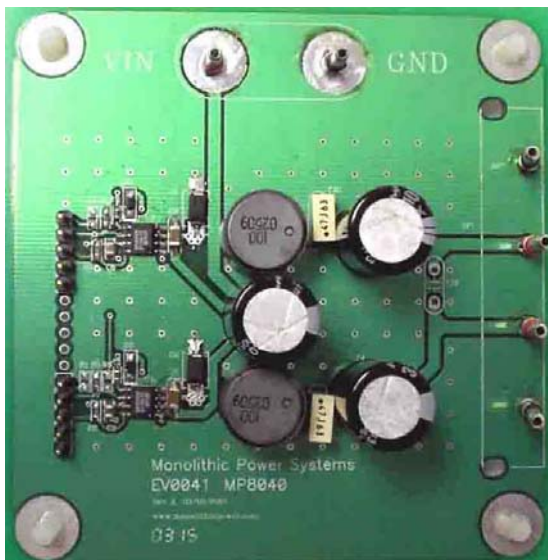
The EV0041 is an evaluation board designed to demonstrate the capabilities of MPS' MP8040. It can be configured as a stereo single ended amplifier (EV0041A) or a full bridge mono amplifier (EV0041B).

The MP8040 is a general purpose, high frequency half bridge power driver. The MP8040 integrates both top and bottom n-channel MOSFET power switches. The MP8040 is fully protected from both sourcing and sinking current by a preset cycle-by-cycle current limit. The MP8040 features a low-current shutdown-mode, input under-voltage protection, thermal shutdown, and fault flag signal output. The MP8040 interfaces with standard logic signals and is available in small 8-lead SOIC package.

## Ordering Information

Board Number	MPS IC Number
EV0041	<a href="#">MP8040DN</a>

## EV0041 Evaluation Board



(Actual Size: 3.5"X x 3.5"Y)

## Absolute Maximum Ratings

Supply Voltage $V_{IN}$	-0.3V to 26V
SW Pin Voltage $V_{SW}$	-0.3V to $V_{IN}$
SW to BS	-0.3V to 6V
Voltage at All Other Pins	-0.3V to 6V
RMS Output Current	6A Maximum

## Recommended Operating Conditions

Input Supply Voltage ( $V_{IN}$ )	7.5 V to 25V
Peak Output Current	9A Maximum
RMS Output Current	4.5A Maximum

## Features

- **+/- 9A Peak Current Output**
- **+/- 4.25A Continuous Current Output**
- Up to 1.2MHz Switching Frequency
- Protected Integrated Power 0.1  $\Omega$  Switches
  - Designed Switch Dead time of 30ns
  - All Switches Current Limited
  - Internal Under-voltage Protection
  - Internal Thermal Protection
- 1 $\mu$ A Standby Mode
- Fault Indicator Output

## Applications

- Full or Half Bridge DC-DC Switching Regulator
- Class D Audio Driver
- Motor Driver



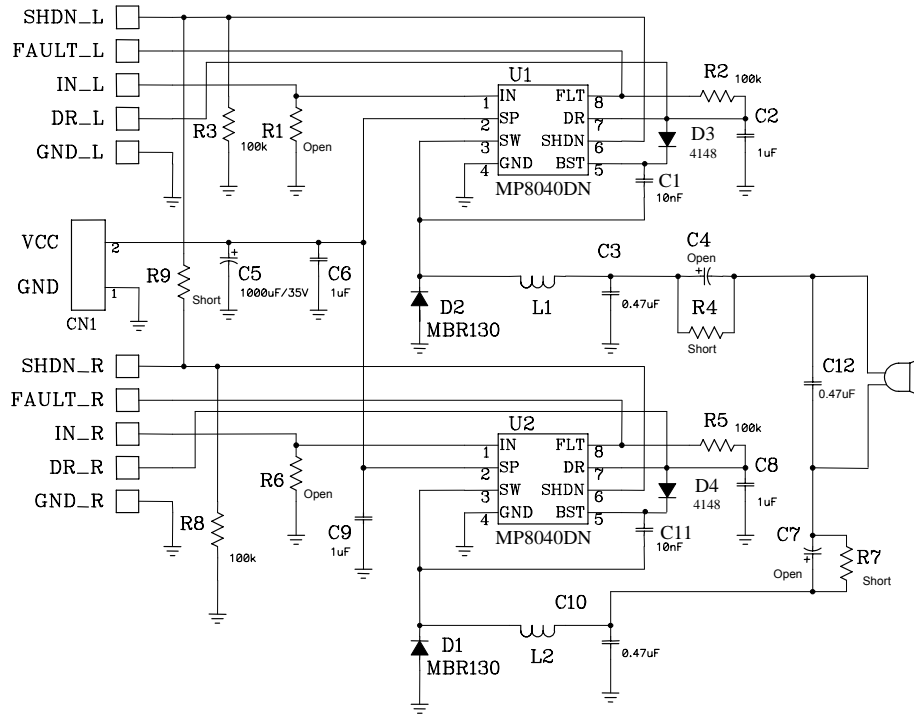
# MP8040

## EVALUATION BOARD

The schematic diagram illustrates the MP8040DN evaluation board, featuring two identical channels for SP1:A and SP1:B. Each channel is powered by a VCC and GND connection through a connector CN1. The input section for each channel includes pins for SHDN\_L, FAULT\_L, IN\_L, DR\_L, and GND\_L for the first channel, and SHDN\_R, FAULT\_R, IN\_R, DR\_R, and GND\_R for the second channel. The MP8040DN converter (U1 and U2) is configured with its input (IN) connected to the input pins, its output (OUT) connected to the output pins, and its fault (FLT) pin connected to the fault pins. The converter's status pins (SP, SW, GND, BST) are connected to ground. The output of each channel is connected to a speaker (SP1:A and SP1:B) through a series of components: a diode (D2 and D1, MBR130), an inductor (L1 and L2), a capacitor (C3 and C10, 0.47uF), a resistor (R4 and R7, 100k), and a capacitor (C4 and C7, 1000uF/35V). The output pins (SHDN\_R, FAULT\_R, IN\_R, DR\_R, GND\_R) are connected to ground through resistors (R6, R8, R9, R10, 100k) and capacitors (C5, C6, C8, C9, 1uF). The output pins (SHDN\_L, FAULT\_L, IN\_L, DR\_L, GND\_L) are connected to ground through resistors (R1, R2, R3, R4, 100k) and capacitors (C1, C2, C3, C4, 1uF). The output pins (SHDN\_R, FAULT\_R, IN\_R, DR\_R, GND\_R) are connected to ground through resistors (R6, R8, R9, R10, 100k) and capacitors (C5, C6, C8, C9, 1uF). The output pins (SHDN\_L, FAULT\_L, IN\_L, DR\_L, GND\_L) are connected to ground through resistors (R1, R2, R3, R4, 100k) and capacitors (C1, C2, C3, C4, 1uF).

Component	Description	Manufacturer Part Number	Package	Qty
U1, U2	PWM Power Driver	Monolithic Power Systems MP8040DN	SOIC8	2
C4, C5, C7	1000μF/35V	Panasonic P/N EEUF1C1V102B	5.0-R10.0	3
C3, C10	0.47μF	Panasonic P/N ECQV1H474JL	5.08	3
C12	No Stuff	N/A	5.08	0
C1, C11	10nF	NIC P/N NMC0603X7R103K10	0603	2
	Alternate	Taiyo Yuden P/N UMK107BJ103MA	0603	0
C2, C8	1μF	Taiyo Yuden P/N UMK107BJ103MA	0805	2
C6, C9	1μF	NIC P/N NMC12063X7R105K16	1206	2
	Alternate	Taiyo Yuden P/N GMK316BJ105ML	1206	
L1, L2	15μH, 6A	Toko P/N 13BHBP-A7502H	13BHBP	2
R1, R6	No Stuff	Taiyo Yuden P/N GMK316BJ105ML	0805	0
R2, R3, R5, R8	100KΩ	Toko P/N 13BHBP-A7502H	0805	4
R4, R7, R9	No Stuff	N/A	0805	0
D1, D2	1A, 30V, Schottky	On Semiconductor P/N MBR130	SMC	2
	Alternate	Diodes Inc., P/N B130B	SMC	0
D3, D4	300mA, 100V	Diodes Inc. P/N 1N4148WS	SOD323	2
			<b>Total</b>	<b>24</b>

**Figure 4: EV0041B Mono Full Bridge Schematic**



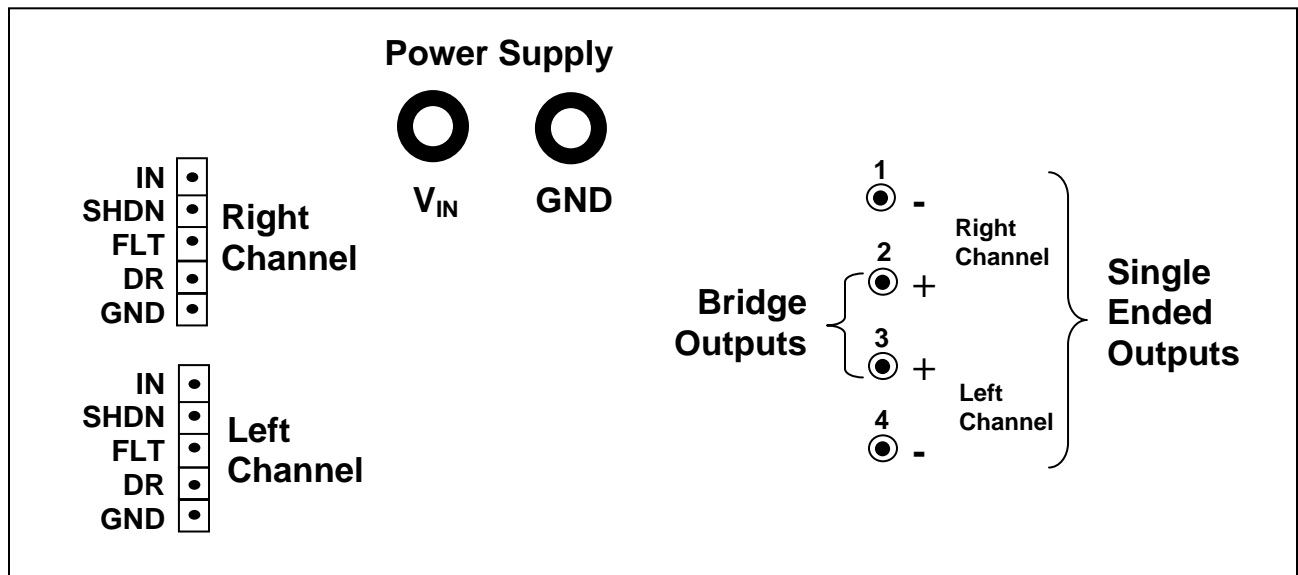
**Table 2: EV0041B Mono Full Bridge Bill of Materials**

Component	Description	Manufacturer Part Number	Package	Qty
U1, U2	PWM Power Driver	Monolithic Power Systems MP8040DN	SOIC8	2
C5	1000μF/35V	Panasonic P/N EEUFC1V102B	5.0-R10.0	3
C3, C10, C12	0.47μF	Panasonic P/N ECQV1H474JL	5.08	3
C4, C7	No Stuff	N/A	5.0-R10.0	0
C1, C11	10nF	NIC P/N NMC0603X7R103K10	0603	2
	Alternate	Taiyo Yuden P/N UMK107BJ103MA	0603	0
C2, C8	1μF	Taiyo Yuden P/N UMK107BJ103MA	0805	2
C6, C9	1μF	NIC P/N NMC12063X7R105K16	1206	2
	Alternate	Taiyo Yuden P/N GMK316BJ105ML	1206	0
L1, L2	15μH, 6A	Toko P/N 13BHBP-A7502H	13BHBP	2
R1, R6	No Stuff	Taiyo Yuden P/N GMK316BJ105ML	0805	0
R2, R3, R5, R8	100KΩ	Toko P/N 13BHBP-A7502H	0805	4
R4, R7, R9	0Ω	N/A	0805	0
D1, D2	1A, 30V, Schottky	On Semiconductor P/N MBR130	SMC	2
	Alternate	Diodes Inc., P/N B130B	SMC	0
D3, D4	300mA, 100V	Diodes Inc. P/N 1N4148WS	SOD323	2
			<b>Total</b>	<b>24</b>

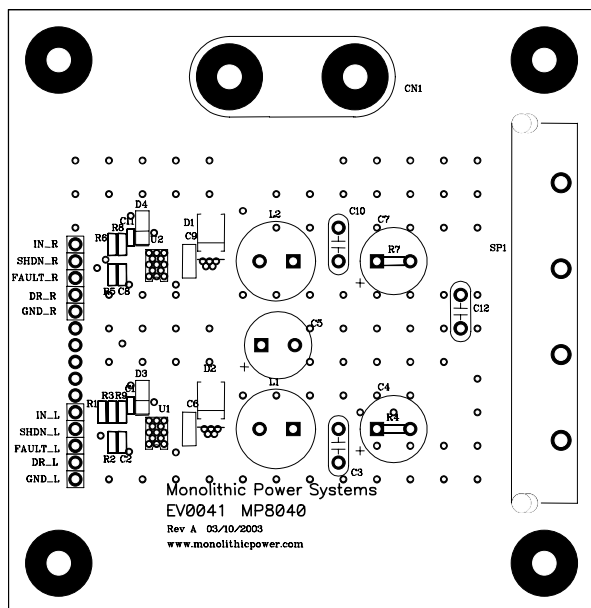
## Operation

1. The EV0041 comes configured as a stereo single ended audio amplifier (EV0041A).
2. To configure the board as a full bridge circuit (EV0041B), short R4, R7, R9, remove C4, C7 and stuff C12 with a 0.47 $\mu$ F capacitor.
3. Connect the audio inputs to the IN pins as shown in Figure 5.
4. Connect speakers to pins 1-4 as shown in Figure 5 for single ended configuration. Use pins 2 and 3 for bridged circuit.
5. Connect the power supply to the V<sub>IN</sub> terminals as shown in Figure 5.
6. SHDN enables/disables the MP8040. Drive SHDN low to turn on the MP8040, drive it high to turn it off. If not used connect SHDN to GND.
7. A low output at FLT indicates that the MP8040 has detected a fault and has shutdown.
8. The DR pin is an optional fixed 5V voltage output capable of driving a 1mA load for external circuitry.

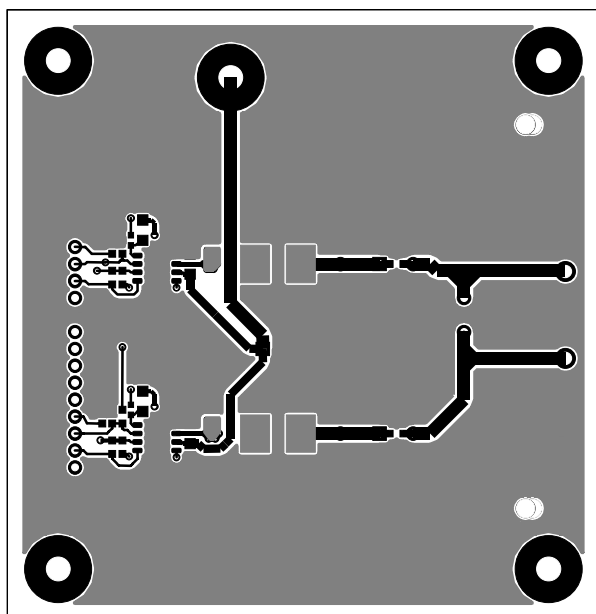
**Figure 5: Top Side Evaluation Board Diagram**



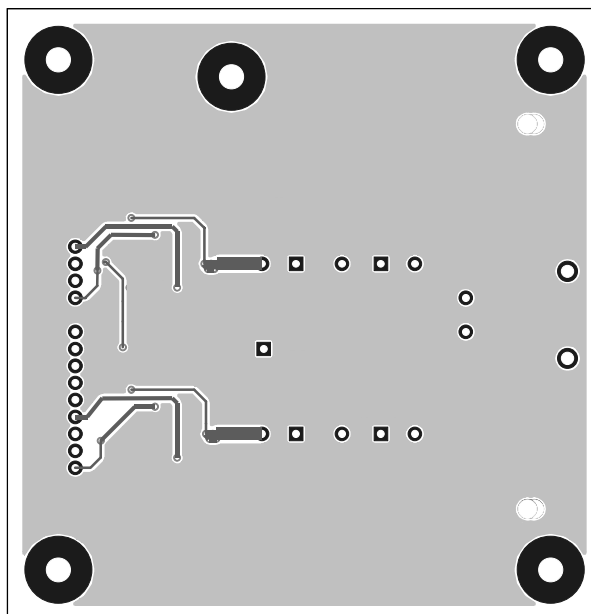
**Figure 6: Top Silk Layer**



**Figure 7: Top Layer**



**Figure 8: Bottom Layer**



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