

16-Bit D-type registered transceiver; 3-state

74ALVCH16543

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FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- 16-Bit transceiver with D-type latch
- Combines '16245 and '16373 type functions in one chip
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- All data inputs have bushold
- 3-state non-inverting outputs for bus oriented applications

DESCRIPTION

The 74ALVCH16543 is a dual octal registered transceiver. Each section contains two sets of D-type latches for temporary storage of the data flow in either direction. Separate latch enable (\overline{LE}_{AB} , \overline{LE}_{BA}) and output enable (\overline{OE}_{AB} , \overline{OE}_{BA}) inputs are provided for each register to permit independent control in either direction of the data flow.

The '16543' contains two sections each consisting of two sets of eight D-type latches with separate inputs and controls for each set. For data flow from A to B, for example, the A-to-B enable ($n\overline{E}_{AB}$, where n equals 1 or 2) input must be LOW in order to enter data from nA_0 - nA_7 , or take data from nB_0 - nB_7 , as indicated in the function table. With $n\overline{E}_{AB}$ LOW, a LOW signal on the A-to-B latch enable ($n\overline{LE}_{AB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $n\overline{LE}_{AB}$ signal stores the A data into the latches. With \overline{E}_{AB} and \overline{OE}_{AB} both LOW, the 3-state B output buffers are active and display the data present at the output of the A latches. Similarly, the \overline{E}_{BA} , \overline{LE}_{BA} and \overline{OE}_{BA} signals control the data flow from B-to-A.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25^\circ\text{C}$; $t_r = t_f = 2.5\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n ; LE to Q_n	$C_L = 50\text{ pF}$ $V_{CC} = 3.3\text{ V}$	3.0 3.2	ns
C_i	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	22	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is $V_i = \text{GND}$ to V_{CC} .

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVCH16543DL	56	SSOP56	plastic	SOT371-1
74ALVCH16543DGG	56	TSSOP56	plastic	SOT364-1

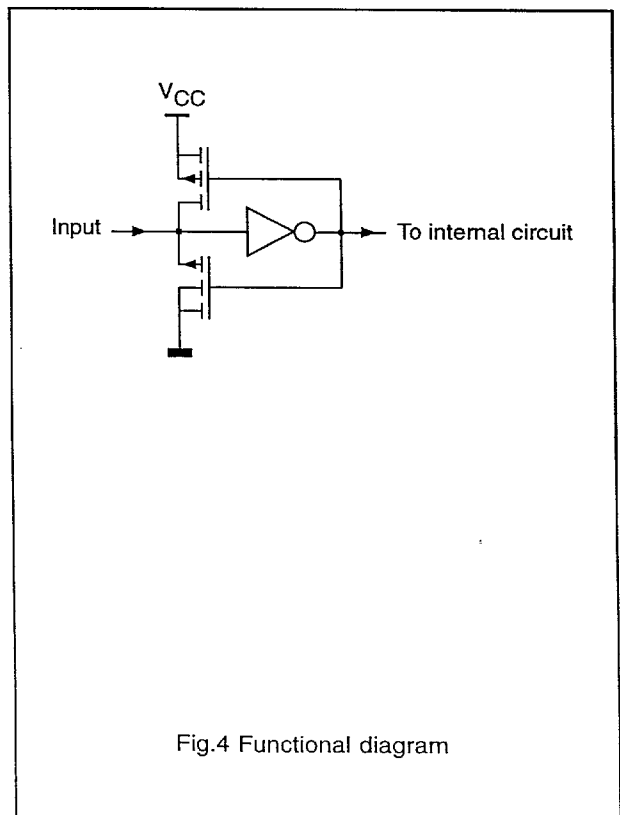
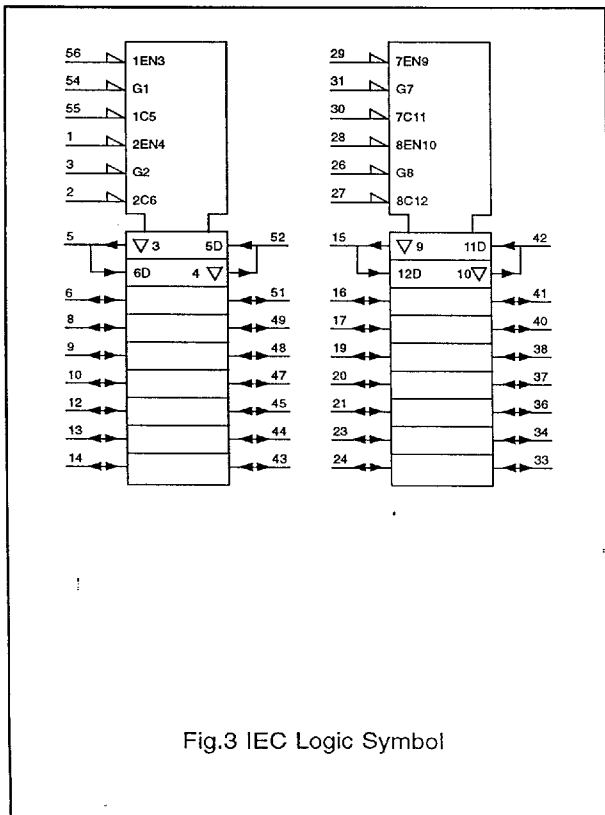
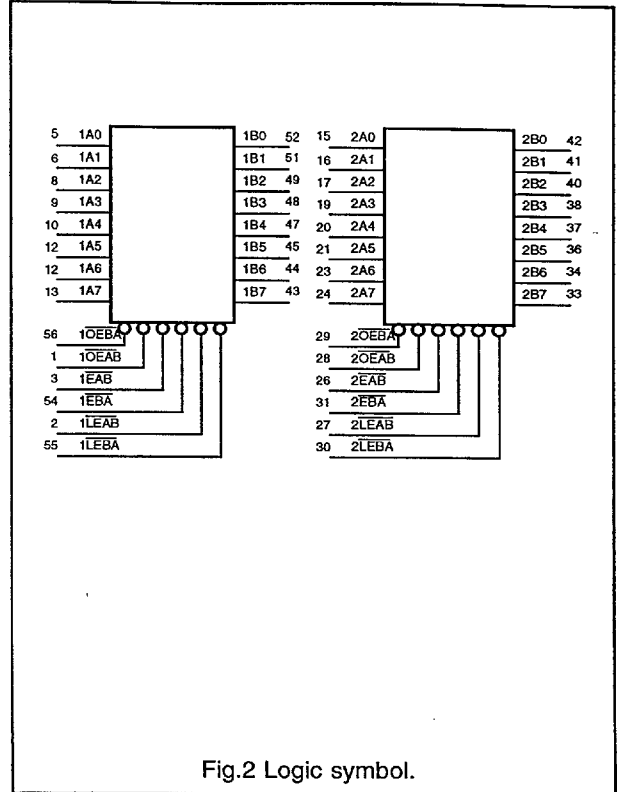
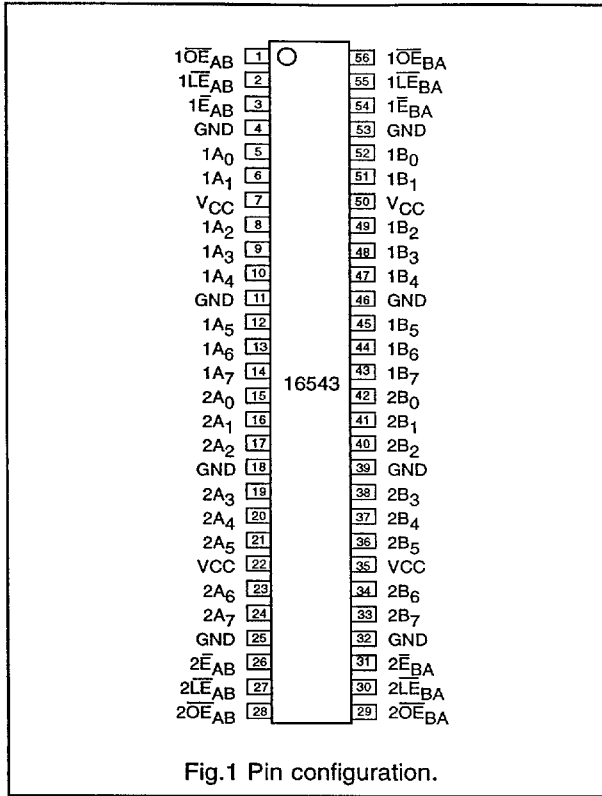
PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 28	$n\overline{OE}_{AB}$	Output enable A-to-B for register 1 or 2
2, 27	$n\overline{LE}_{AB}$	Latch enable A-to-B for register 1 or 2
3, 26	$n\overline{E}_{AB}$	A-to-B enable for register 1 or 2
5, 6, 8, 9, 10, 12, 13, 14	$1A_0$ to $1A_7$	'1A' data inputs/outputs
4, 11, 18, 25, 32, 39, 46, 53	GND	ground (0 V)
7, 22, 35, 50	V_{CC}	positive supply voltage
15, 16, 17, 19, 20, 21, 23, 24	$2B_0$ to $2B_7$	'2B' data inputs/outputs
29, 56	$n\overline{OE}_{BA}$	Output enable B-to-A for register 1 or 2
30, 55	$n\overline{LE}_{BA}$	Latch enable B-to-A for register 1 or 2
31, 54	$n\overline{E}_{BA}$	B-to-A enable for register 1 or 2
42, 41, 40, 38, 37, 36, 34, 33	$2B_0$ to $2B_7$	'2B' data inputs/outputs
52, 51, 49, 48, 47, 45, 44, 43	$1B_0$ to $1B_7$	'1B' data inputs/outputs

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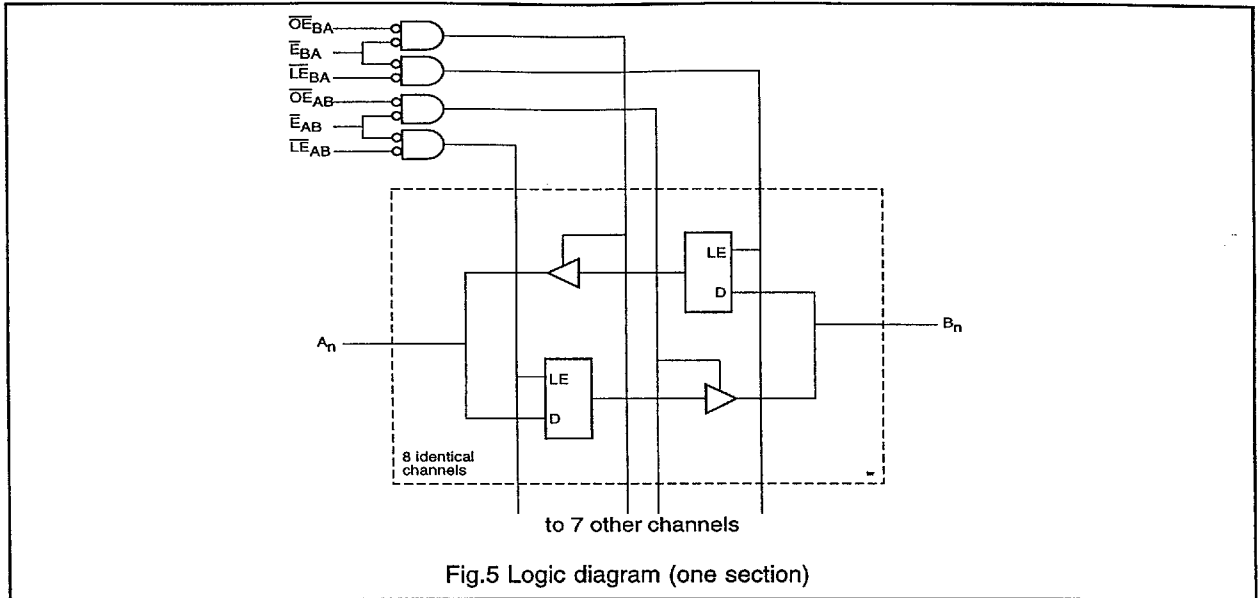
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FUNCTION TABLE

INPUTS			DATA	OUTPUTS	STATUS
\overline{OE}_{xx}	\overline{E}_{xx}	\overline{LE}_{xx}			
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disables
L	↑	L	h	Z	Disabled + Latch
L	↑	L	l	Z	
L	L	↑	h	H	Latch + Display
L	L	↑	l	L	
L	L	L	H	H	Transparent
L	L	L	L	L	
L	L	H	X	NC	Hold

XX = AB for A-to-B direction, BA for B-to-A direction

H = HIGH voltage level

L = LOW voltage level

h = High state must be present one setup time before the low-to-high transition of \overline{LE}_{AB} , \overline{LE}_{BA} , \overline{E}_{AB} or \overline{E}_{BA}

l = Low state must be present one setup time before the low-to-high transition of \overline{LE}_{AB} , \overline{LE}_{BA} , \overline{E}_{AB} or \overline{E}_{BA}

X = Don't care

↑ = LOW-to-HIGH level transition

NC = No change

Z = High impedance "off" state

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DC CHARACTERISTICS FOR 74ALVCH16543

For the DC characteristics see chapter "ALVCH family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74ALVCH16543

GND = 0 V; $t_r = t_f = 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T _{amb} (°C)			UNIT	TEST CONDITIONS	
		-40 to +85				V _{CC} (V)	WAVEFORMS
		MIN.		MAX.			
t _{PHL} /t _{PLH}	propagation delay A _n to B _n , B _n to A _n	-	-	18.0	ns	1.2	Fig.6
		-	-	4.8		2.7	
		-	3.0*	4.4		3.0 to 3.6	
t _{PHL} /t _{PLH}	propagation delay \overline{LE}_{BA} to A _n , \overline{LE}_{AB} to B _n	-	-	20.0	ns	1.2	Fig.6
		-	-	6.0		2.7	
		-	3.2*	5.4		3.0 to 3.6	
t _{PZH} /t _{PZL}	3-state output enable time \overline{OE}_{BA} to A _n , \overline{OE}_{AB} to B _n	-	-	22.0	ns	1.2	Fig.7
		-	-	6.1		2.7	
		-	-	5.5		3.0 to 3.6	
t _{PHZ} /t _{PLZ}	3-state output disable time \overline{OE}_{BA} to A _n , \overline{OE}_{AB} to B _n	-	-	22.0	ns	1.2	Fig.7
		-	-	6.1		2.7	
		-	-	5.5		3.0 to 3.6	
t _{PZH} /t _{PZL}	3-state output enable time \overline{E}_{BA} to A _n , \overline{E}_{AB} to B _n	-	-	22.0	ns	1.2	Fig.8
		-	-	6.1		2.7	
		-	-	5.5		3.0 to 3.6	
t _{PHZ} /t _{PLZ}	3-state output disable time \overline{E}_{BA} to A _n , \overline{E}_{AB} to B _n	-	-	22.0	ns	1.2	Fig.8
		-	-	6.1		2.7	
		-	-	5.5		3.0 to 3.6	

SYMBOL	PARAMETER	T _{amb} (°C)			UNIT	TEST CONDITIONS	
		-40 to +85				V _{CC} (V)	WAVEFORMS
		MIN.		MAX.			
t _w	LE pulse width LOW	2.8	-	-	ns	2.7	Fig.7
		2.5	-	-		3.0 to 3.6	
t _{su}	set-up time A _n /B _n to \overline{LE}_{XX} , A _n /B _n to \overline{E}_{XX}	2.2	-	-	ns	1.2	Fig.9
		0.7	-	-		2.7	
		0.6	-	-		3.0 to 3.6	
t _h	hold time A _n /B _n to \overline{LE}_{XX} , A _n /B _n to \overline{E}_{XX}	2.2	-	-	ns	1.2	Fig.9
		0.7	-	-		2.7	
		0.6	-	-		3.0 to 3.6	

Notes: All typical values are measured at T_{amb} = 25 °C.* Typical values are measured at V_{CC} = 3.3 V.

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AC WAVEFORMS

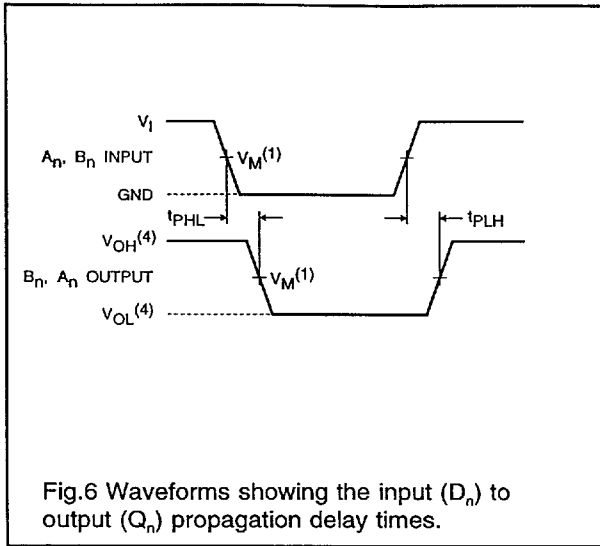


Fig.6 Waveforms showing the input (D_n) to output (Q_n) propagation delay times.

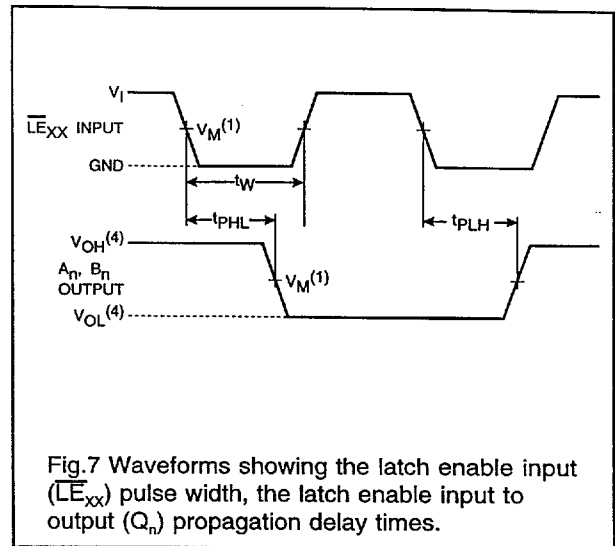


Fig.7 Waveforms showing the latch enable input (\overline{LE}_{xx}) pulse width, the latch enable input to output (Q_n) propagation delay times.

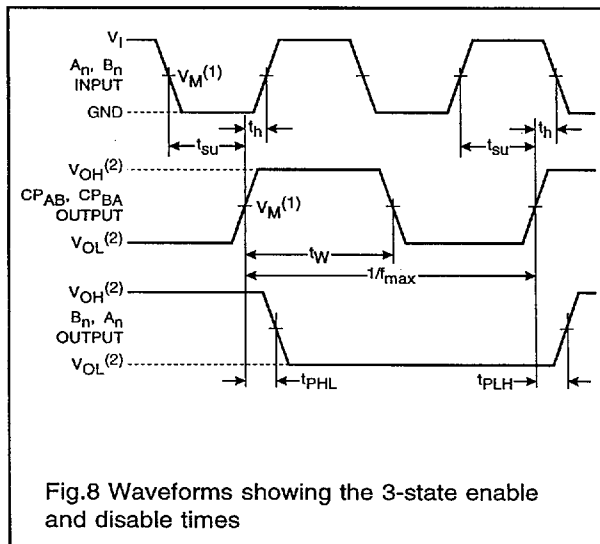


Fig.8 Waveforms showing the 3-state enable and disable times

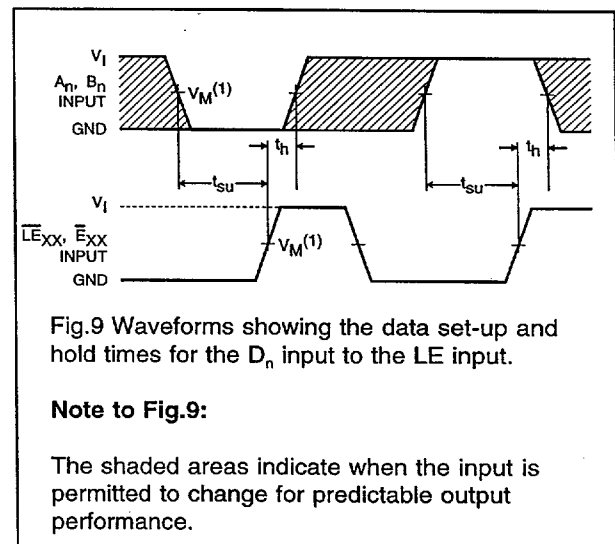


Fig.9 Waveforms showing the data set-up and hold times for the D_n input to the LE input.

Note to Fig.9:

The shaded areas indicate when the input is permitted to change for predictable output performance.

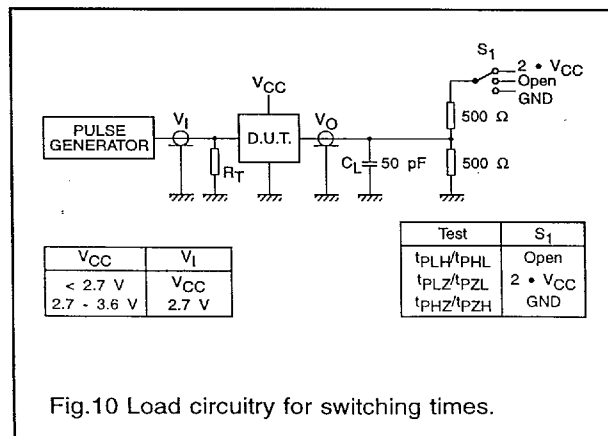


Fig.10 Load circuitry for switching times.

- Notes:
- (1) $V_M = 1.5 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$
 $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7 \text{ V}$
 - (2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
 - (3) $V_X = V_{OL} + 0.3 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$
 $V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7 \text{ V}$
 - (4) $V_Y = V_{OH} - 0.3 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$
 $V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7 \text{ V}$