BURR-BROWN®

SHC804

High Speed SAMPLE/HOLD AMPLIFIER

FEATURES

- 350ns max ACQUISITION TIME
- ±0.01% THROUGHPUT NONLINEARITY
- 150ns max SAMPLE-TO-HOLD SETTLING TIME
- 24-PIN HERMETICALLY-SEALED METAL PACKAGE

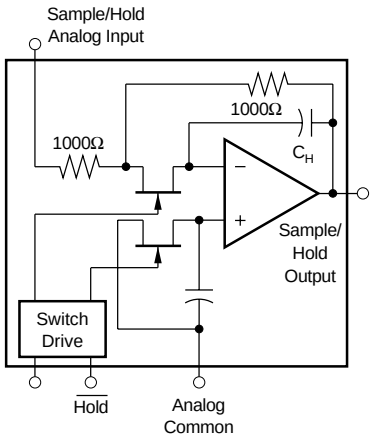
DESCRIPTION

The SHC804 is a high speed sample/hold amplifier designed for use in fast 12-bit data acquisition systems and signal processing systems.

The SHC804 acquires a 10V signal change in less than 350ns to ±1/2LSB at 12 bits. Throughput nonlinearity error is guaranteed to be within ±1/2LSB for 12-bit systems. Stability over temperature is excellent, with only ±5ppm/°C of gain drift and ±4ppm of FSR/°C of charge offset drift over the –25 to +85°C temperature range.

The ±25ps maximum aperture uncertainty of the SHC804 permits sampling (to ±0.01% of Full Scale Range) of signals with rates of change of up to 100V/µs. This component is capable of accurately digitizing fast changing signals at sample rates as high as 500k samples per second.

The digital inputs (HOLD and $\overline{\text{HOLD}}$) are TTL-compatible. Power supply requirements are ±15V and +5V and the specification temperature range is –25°C to +85°C. The SHC804 is packaged in a 24-pin dual-in-line hermetic metal package. SHC804 is pin-compatible with other sample/holds on the market with similar performance characteristics.



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PDS-512E
Printed in U.S.A. March, 1998

SPECIFICATIONS

At +25°C, rated power supplies and a 1kΩ output load, unless otherwise specified.

PARAMETER	SHC804BM MIN	SHC804BM TYP	SHC804BM MAX	SHC804CM MIN	SHC804CM TYP	SHC804CM MAX	UNITS
SAMPLE/HOLD INPUTS (without Input Buffer)							
ANALOG							
Voltage Range	±10.25	±11		*	*		V
R_{IN}		1.00			*		kΩ
DIGITAL (HOLD, $\overline{HOLD}$)							
V_{IH}	+2.0			*			V
V_{IL}			+0.8			*	V
I_{IH}, V_{IN} = +2.7V			+60			*	µA
I_{IL}, V_{IN} = +0.4V			–1.2			*	mA
SAMPLE/HOLD TRANSFER CHARACTERISTICS (without Input Buffer)							
ACCURACY							
Sample Mode							
Gain		–1			*		V/V
Gain Error			±0.1			*	%
Temperature Coefficient		±3	±10		±1	±5	ppm/°C
Linearity Error		±0.001	±0.005		*	*	% of FSR(1)
Zero Offset		±1	±5		±0.5	±3	mV
Temperature Coefficient		±1	±2.5		±0.5	±1.5	ppm of FSR/°C
Hold Mode							
Charge Offset		±2	±10		±1	±5	mV
Temperature Coefficient		±3	±10		±2	±4	ppm of FSR/°C
Droop Rate: at +25°C		±0.5	±5		*	*	µV/µs
+85°C			±0.5			±0.1	mV/µs
Throughput Nonlinearity			±0.01			*	% of FSR
Power Supply Sensitivity(2): ±V_{CC}			±0.002			*	% of FSR/%V_{CC}
V_{DD}			±0.003			*	% of FSR/%V_{DD}
DYNAMIC CHARACTERISTICS							
Acquisition Time (with 10V Step)							
to within: ±0.1% (±10mV)		220			*		ns
±0.01% (±1mV)		250	350		*	*	ns
Sample-to-Hold Settling Time							
to within ±0.01% (±1mV)		100	150		*	*	ns
Sample-to-Hold Transient Amplitude		60	150		*	*	mV_{PEAK}
Aperture Delay TIme(3)		15	25		*	*	ns
Aperture Uncertainty		±10	±25		*	*	ps
Sample Mode: Output Slew Rate		160			*		V/µs
Full Power Bandwidth		1			*		MHz
Small Signal Bandwidth		16			*		MHz
Hold Mode Feedthrough Rejection							
(10V Square Wave Input)	±0.03	±0.005			*		%
SAMPLE/HOLD OUTPUT							
Voltage Range	±10.25	±11		*	*		V
Output Current	±50			*			mA
Short Circuit Protection		Indefinite to Common			*		
Output Impedance (at DC)		0.01	0.1		*	*	Ω
POWER SUPPLY REQUIREMENTS							
Rated Voltage: ±V_{CC}	±13.5	±15	±16.5	*	*	*	V
V_{DD}	+4.75	+5.00	+5.25	*	*	*	V
Quiescent Current (No Load)							
SHC804: +V_{CC}		30	35		*	*	mA
–V_{CC}		15	20		*	*	mA
V_{DD}		5	10		*	*	mA
SHC803: +V_{CC}		33	40		*	*	mA
–V_{CC}		18	25		*	*	mA
V_{DD}		5	10		*	*	mA
Power Dissipation: SHC804		700	875		*	*	mW
TEMPERATURE RANGE							
Specification	–25		+85	*		*	°C
Storage	–55		+125	*		*	°C

* Specification same as SHC804BM.

NOTES: (1) FSR means Full Scale Range and is 20V for SHC804. (2) Sensitivity of offset plus charge offset. (3) With respect to HOLD. For $\overline{HOLD}$ add 5ns typical. (4) With buffer connected to the sample/hold amplifier.

ABSOLUTE MAXIMUM RATINGS[1]

Input Overvoltage	±15V
$+V_{CC}$ to V_{CC} COMMON	0 to +18V
$-V_{CC}$ to V_{CC} COMMON	0 to –18V
Voltage on Digital Inputs (pins 11 and 12)	–0.5V to +7V
Power Dissipation	1500mW
V_{DD} to DCOM	–0.5V
Analog Output	Indefinite Short to V_{CC} COM

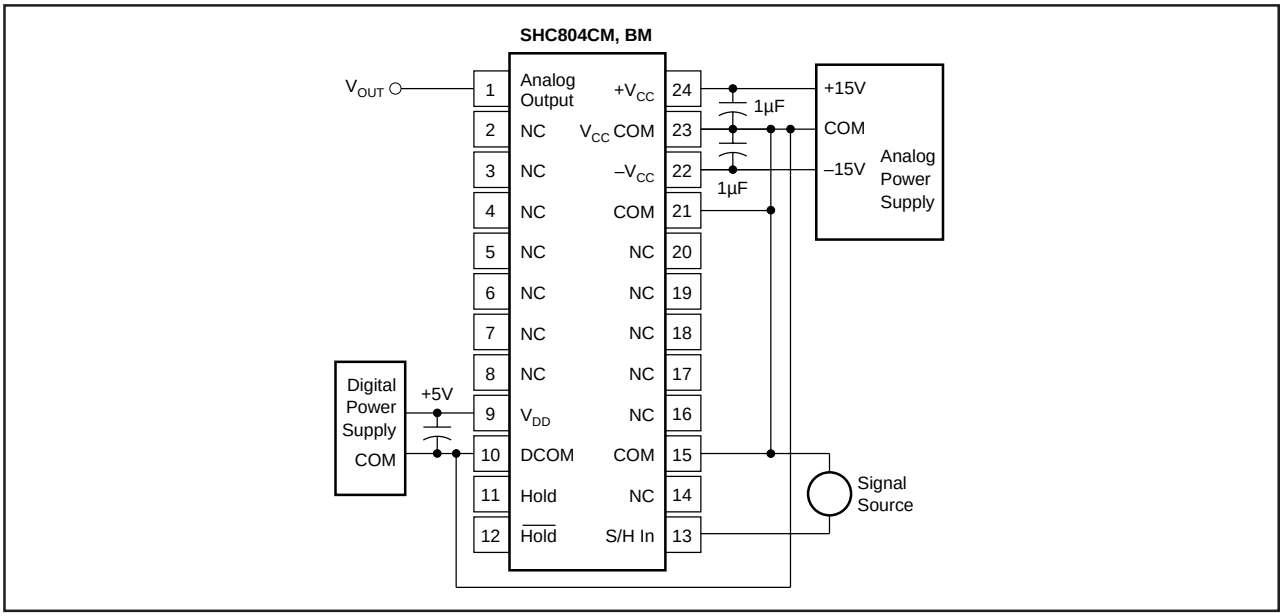
NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER[1]
SHC804BM	24-Pin	037
SHC804CM	24-Pin	037

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

CONNECTION DIAGRAMS



PIN ASSIGNMENTS

PIN	NAME	DESCRIPTION
1	Sample/Hold Output	Analog voltage output
2	NC	Not connected
3	NC	Not connected
4	NC	Not connected
5	NC	Not connected
6	NC	Not connected
7	NC	Not connected
8	NC	Not connected
9	V_{DD}	Logic supply
10	DCOM	Logic supply common
11	HOLD	Logic "1" = HOLD
12	$\overline{\text{HOLD}}$	Logic "0" = HOLD
13	S/H In	SHC804 input
14	NC	Not connected
15	COM	Signal common
16	NC	Not connected
17	NC	Not connected
18	NC	Not connected
19	NC	Not connected
20	NC	Not connected
21	COM	Signal common
22	$-V_{CC}$	–15V supply
23	V_{CC} COM	Analog to power common, connected to case
24	$+V_{CC}$	+15V supply

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCUSSION OF SPECIFICATIONS

Throughput Nonlinearity is defined as total Hold mode, nonadjustable, input to output error caused by charge offset, gain nonlinearity, droop, feedthrough, and thermal transients. It is the inaccuracy due to these errors which cannot be corrected by Offset and Gain adjustments.

Gain Error is the difference between the input and output voltage magnitude (in the Sample mode) due to the amplifier gain errors.

Droop Rate is the voltage decay at the output when in the Hold mode due to storage capacitor and FET switch leakage current and the input bias current of the output amplifier.

Feedthrough is the amount of output voltage change caused by an input voltage change when the sample/hold is in the Hold mode.

Aperture Delay Time is the time required to switch from Sample to Hold. The time is measured from the 50% point of the Hold mode control transition to the time at which the output stops tracking the input.

Aperture Uncertainty Time is the nonrepeatability of aperture delay time.

Acquisition Time is the time required for the sample/hold output to settle to within a given error band of its final value when the sample/hold is switched from Hold to Sample.

Charge Offset (Pedestal) is the output voltage change that results from charge coupled into the Hold capacitor through the gate capacitance of the switching field effect transistor. This charge appears as an offset at the output.

Sample-to-Hold Switching Transient is the switching transient which appears on the output when the sample/hold is switched from Sample to Hold. Both the magnitude and the settling time of the transient are specified.

OPERATION

In the Sample (track) mode the circuit acts as a unity-gain inverting amplifier. In the Hold mode, the capacitor, C_H, holds the value of the output at the time the unit was switched to the Hold mode. Additional circuits compensate for switching transients and provide switch leakage current cancellation. The amplifier provides high current drive and low output impedance to external loads.

GAIN, OFFSET, CHARGE OFFSET

SHC804 has been internally-trimmed to eliminate the need for external trim potentiometers for Gain, Offset (in Sample mode) and Charge Offset (Pedestal). System Gain and Offset errors can be adjusted elsewhere in the system, at an input amplifier preceding the sample/hold, or at an analog-to-digital converter following the sample/hold.

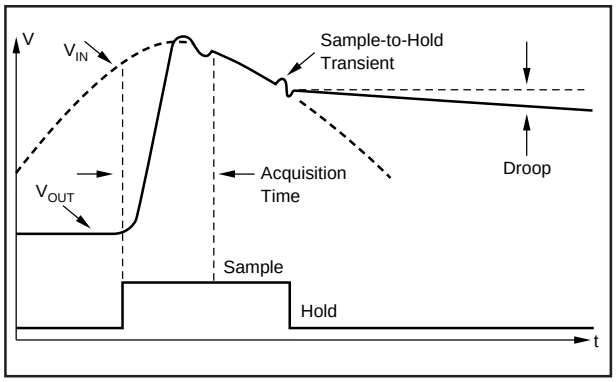


FIGURE 1. Definition of Acquisition Time, Droop and Sample-to-Hold Transient.

INSTALLATION

GROUNDING AND BYPASSING

SHC804 has four COMMON pins (pins 10, 15, 21 and 23) and all must be tied together and connected to the system analog common (V_{CC} COM) as close to the package as possible. It is preferable to have a large ground plane surrounding the sample/hold and have all four common pins soldered directly to it. Note that the metal case is internally connected to pin 23; therefore, care must be taken to avoid a ground loop if the case is allowed to contact the ground plane.

Most digital return currents pass through pin 10. Noise from the switch-drive circuit may couple directly into the main op amp summing junction, a very noise-sensitive node. Care must be taken to insure that no voltage differences occur between pin 10 and the other common pins. This is the reason pin 10 must be connected directly to the ground plane.

For the same reason, the logic supply should be kept as free of noise as possible. $\pm V_{CC}$ supply lines (pins 24 and 22) are internally bypassed to common with 0.01µF capacitors. It is recommended that the user install additional external 0.1µF to 1µF tantalum bypass capacitors at each supply pin.

SAMPLE/HOLD CONTROL

A TTL logic “0” at pin 11 (or a logic “1” at pin 12) switches the SHC804 into the Sample (track) mode. In this mode, the device acts as a unity-gain inverting amplifier, the output following the inverse of the input. A logic “1” at pin 11 (or a logic “0” at pin 12) will switch the SHC804 into the Hold mode. The output voltages will be held constant at the value present when the Hold command is given.

If pin 11 is used, pin 12 must be connected to the DCOM (pin 10). If pin 12 is used, pin 11 must be tied to V_{DD}. Using the HOLD and $\overline{\text{HOLD}}$ inputs as logic function may adversely affect the charge offset (pedestal). A clean digital signal (no overshoot) at the HOLD of $\overline{\text{HOLD}}$ inputs will also reduce charge offset errors. Pins 11 and 12 present less than one standard TTL load (two LSTTL loads) to the digital drive circuit.

OUTPUT LOADING

Care must be taken when loading the output of the SHC804 to avoid possible oscillations, current limiting and performance variations over temperature.

The maximum capacitive load to avoid oscillations is about 300pF. Recommended resistive load is 500Ω or more, although values as low as 250Ω may be used. Acquisition and sample-to-hold settling times are relatively unaffected by resistive loads down to 250Ω in parallel with capacitive loads up to 100pF. Higher capacitances will affect acquisition and settling times.

ANALOG SIGNAL SOURCE CONSIDERATIONS

The output impedance of the signal source driving the SHC804 will affect the accuracy of the sample and hold operation both statically (at DC) and dynamically. The output impedance of the signal source should be low and remain low over a wide bandwidth. A small capacitor at the driving source may help to improve the charge offset errors that are affected by dynamic source impedance.