

CY14B101K

1 Mbit (128K x 8) nvSRAM With Real Time Clock

Features

- Data integrity of Cypress nvSRAM combined with full featured Real Time Clock (RTC)
- Watchdog timer
- Clock alarm with programmable interrupts
- Capacitor or battery backup for RTC
- 25 ns, 35 ns, and 45 ns access times
- Hands off automatic STORE on power down with only a small capacitor
- STORE to QuantumTrap[™] initiated by software, device pin, or on power down
- RECALL to SRAM initiated by software or on power up
- Infinite READ, WRITE, and RECALL cycles
- High reliability
 Endurance to 200,000 cycles
 Data retention: 20 years at 55°C
- 10 mA typical I_{CC} at 200 ns cycle time
- Single 3V operation +20%, -10%
- Commercial and industrial temperature
- SSOP package (ROHS compliant)

Functional Description

The Cypress CY14B101K combines a 1 Mbit nonvolatile static RAM with a full featured real time clock in a monolithic integrated circuit. The embedded nonvolatile elements incorporate QuantumTrap™ technology producing the world's most reliable nonvolatile memory. The SRAM is read and written an infinite number of times, while independent, nonvolatile data resides in the nonvolatile elements.

The Real Time Clock function provides an accurate clock with leap year tracking and a programmable high accuracy oscillator. The alarm function is programmable for one time alarm or periodic seconds, minutes, hours, or days. There is also a programmable watchdog timer for process control.





198 Champion Court

San Jose, CA 95134-1709 • 408-943-2600 Revised Nov 06, 2007



Pinouts

Figure 1. Pin Diagram - 48 SSOP



Pin Definitions

Pin Name	Ю Туре	Description					
$A_0 - A_{16}$	Input	ddress inputs used to select one of the 131,072 bytes of the nvSRAM.					
DQ0 – DQ7	Input Output	Bidirectional Data IO Lines. Used as input or output lines depending on operation					
NC	No Connect	No Connects. This pin is not connected to the die					
WE	Input	rite Enable Input, Active LOW . When selected LO <u>W</u> , enables data on the IO pins to be written the address location latched by the falling edge of CE.					
CE	Input	Chip Enable Input, Active LOW. When LOW, selects the chip. When HIGH, deselects the chip.					
ŌE	Input	Itput Enable, Active LOW. The active low \overline{OE} input enables the data output buffers during READ cles. Deasserting \overline{OE} high causes the IO pins to tri-state.					
X ₁	Output	Crystal Connection, drives crystal on start up.					
X ₂	Input	Crystal Connection for 32.768 kHz crystal.					
V _{RTCcap}	Power Supply	Capacitor Supplied Backup RTC Supply Voltage. (Left unconnected if V _{RTCbat} is used)					
V _{RTCbat}	Power Supply	Battery Supplied Backup RTC Supply Voltage. (Left unconnected if V _{RTCcap} is used)					
INT	Output	Interrupt Output. Program to respond to the clock alarm, the watchdog timer, and the power monitor. Programmable to either active HIGH (push or pull) or LOW (open drain).					
V _{SS}	Ground	Ground for the Device. Must be connected to ground of the system.					
V _{CC}	Power Supply	Power Supply Inputs to the Device.					
HSB	Input Output	Hardware Store Busy . When LOW this output indicates a Hardware Store is in progress. When pulled LOW external to the chip it initiates a nonvolatile STORE operation. A weak internal pull up resistor keeps this pin HIGH if not connected (connection optional).					
V _{CAP}	Power Supply	AutoStore TM Capacitor. Supplies power to nvSRAM during power loss to store data from SRAM to nonvolatile elements.					



Device Operation

The CY14B101K nvSRAM is made up of two functional components paired in the same physical cell, a SRAM memory cell, and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data transfers from the SRAM to the nonvolatile cell (the STORE operation) or from the nonvolatile cell to SRAM (the RECALL operation). This unique architecture enables all cells to store and recall in parallel. During the STORE and RECALL operations, SRAM READ and WRITE operations are inhibited. The CY14B101K supports infinite reads and writes similar to a typical SRAM. In addition, it provides infinite RECALL operations, STORE and up to 200,000 STORE operations.

SRAM READ

The CY14B101K performs a READ cycle whenever \overline{CE} and \overline{OE} are LOW, when WE and HSB are HIGH. The address specified on pins A₀₋₁₆ determines which of the 131,072 data bytes are accessed. When the READ is initiated by an address transition, the outputs are valid after a delay of t_{AA} (READ cycle 1). If the READ is initiated by CE or OE, the outputs are valid at t_{ACE} or at t_{DOE}, whichever is later (READ cycle 2). The data outputs repeatedly respond to address changes within the t_{AA} access time without the need for transitions on any control input pins. It remains valid until another address change or until CE or OE is brought HIGH, or WE or HSB is brought LOW.

SRAM WRITE

<u>A WRITE</u> cycle is performed whenever \overrightarrow{CE} and \overrightarrow{WE} are LOW and HSB is HIGH. The address inputs must be stable before entering the WRITE cycle and must remain stable until either \overrightarrow{CE} or \overrightarrow{WE} go HIGH at the end of the cycle. The data on the common IO pins DQ_{0-7} is written into the memory if the data is valid t_{SD} before the end of a WE controlled WRITE or before the end of an \overrightarrow{CE} controlled WRITE. Keep \overrightarrow{OE} HIGH during the entire WRITE cycle to avoid data bus contention on common IO lines. If \overrightarrow{OE} is left LOW, internal circuitry turns off the output buffers t_{HZWE} after WE goes LOW.

AutoStore Operation

The CY14B101K stores data to nvSRAM using one of three storage operations:

- 1. Hardware Store activated by HSB
- 2. Software Store activated by an address sequence
- 3. AutoStore on device power down

AutoStore operation is a unique feature of QuantumTrap technology and is enabled by default on the CY14B101K.

During normal operations, the device draws current from V_{CC} to charge a capacitor connected to the V_{CAP} pin. This stored charge is used by the chip to perform a single STORE operation. If the voltage on the V_{CC} pin drops below V_{SWITCH}, the part automatically disconnects the V_{CAP} pin from V_{CC}. A STORE operation is initiated with power provided by the V_{CAP} capacitor.

Figure 2 shows the proper connection of the storage capacitor (V_{CAP}) for automatic store operation. Refer to the section "DC Electrical Characteristics" on page 14 for the size of V_{CAP}. The voltage on the V_{CAP} pin is driven to 5V by a charge pump internal

Figure 2. AutoStore Mode



to the chip. A pull up is placed on $\overline{\text{WE}}$ to hold it inactive during power up.

To reduce unnecessary nonvolatile stores, AutoStore and Hardware Store operations are ignored unless at least one WRITE operation takes place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a WRITE operation took place. Monitor the HSB signal by the system to detect if an AutoStore cycle is in progress.

Hardware STORE (HSB) Operation

The CY14B101K provides the HSB pin for controlling and acknowledging the STORE operations. Use the HSB pin to request a hardware STORE cycle. When the HSB pin is driven LOW, the CY14B101K conditionally initiates a STORE operation after t_{DELAY}. An actual STORE cycle only begins if a WRITE to the SRAM has taken place since the last STORE or RECALL cycle. The HSB pin also acts as an open drain driver that is internally driven LOW to indicate a busy condition while the STORE (initiated by any means) is in progress.

<u>SRAM</u> READ and WRITE operations that are in progress when HSB is driven LOW by any means are given <u>time</u> to complete before the STORE operation is initiated. After HSB goes LOW, the CY14B101K continues SRAM operations for t_{DELAY}. During t_{DELAY}, multiple SRAM <u>RE</u>AD operations take place. If a WRITE is in progress when HSB is pulled LOW, it is allowed a time, t_{DELAY}, to complete. However, any SRAM W<u>RITE</u> cycles requested after HSB goes LOW are inhibited until HSB returns HIGH.

During any STORE operation, regardless of how it is initiated, the CY14B101K continues to drive the HSB pin LOW, releasing it only when the STORE is complete. After completing the <u>STORE</u> operation, the CY14B101K remains disabled until the HSB pin returns HIGH. Leave the HSB unconnected if it is not used.



Hardware RECALL (Power Up)

During power up or after any low power condition ($V_{CC} < V_{SWITCH}$), an internal RECALL request is latched. When V_{CC} once again exceeds the sense voltage of V_{SWITCH} , a RECALL cycle automatically initiates and takes $t_{HRECALL}$ to complete.

Software STORE

Using a software address sequence, transfer the data from the SRAM to the nonvolatile memory. The CY14B1<u>01K</u> software STORE cycle is initiated by executing sequential CE controlled READ cycles from six specific address locations in exact order. During the STORE cycle, an erase of the previous nonvolatile data is first performed followed by a program of the nonvolatile elements. Once a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for STORE initiation, it is important that no other READ or WRITE accesses intervene in the sequence. If there are intervening READ OR WRITE accesses, the sequence is aborted and no STORE or RECALL takes place.

To initiate the software STORE cycle, the following READ sequence are performed:

- 1. Read Address 0x4E38 Valid READ
- 2. Read Address 0xB1C7 Valid READ
- 3. Read Address 0x83E0 Valid READ
- 4. Read Address 0x7C1F Valid READ
- 5. Read Address 0x703F Valid READ
- 6. Read Address 0x8FC0 Initiate STORE cycle

<u>The</u> software sequence is clocked with \overline{CE} controlled READs or \overline{OE} controlled READs. Once the sixth address in the sequence is entered, the STORE cycle commences and the chip is disabled. It is important that READ cycles and not WRITE cycles are used in the sequence. It is not necessary that OE is LOW for the sequence to be valid. After the t_{STORE} cycle time is fulfilled, the SRAM is activated again for READ and WRITE operation.

Software RECALL

Transfer the data from the nonvolatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of READ operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of CE controlled READ operations are performed:

- 1. Read Address 0x4E38 Valid READ
- 2. Read Address 0xB1C7 Valid READ
- 3. Read Address 0x83E0 Valid READ
- 4. Read Address 0x7C1F Valid READ
- 5. Read Address 0x703F Valid READ
- 6. Read Address 0x4C63 Initiate RECALL Cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared and then the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time, the SRAM is once again ready for READ and WRITE operations. The RECALL operation does not alter the data in the nonvolatile elements.

Preventing AutoStore

Disable the AutoStore function by initiating an AutoStore Disable sequence. A sequence of READ operations is performed in a manner similar to the software STORE initiation. To initiate the AutoStore Disable sequence, the following sequence of CE controlled READ operations are performed:

- 1. Read Address 0x4E38 Valid READ
- 2. Read Address 0xB1C7 Valid READ
- 3. Read Address 0x83E0 Valid READ
- 4. Read Address 0x7C1F Valid READ
- 5. Read Address 0x703F Valid READ
- 6. Read Address 0x8B45 AutoStore Disable

Re-enable the AutoStore by initiating an AutoStore Enable sequence. A sequence of READ operations is performed in a manner similar to the software RECALL initiation. To initiate the AutoStore Enable sequence, the following sequence of CE controlled READ operations are performed:

- 1. Read Address 0x4E38 Valid READ
- 2. Read Address 0xB1C7 Valid READ
- 3. Read Address 0x83E0 Valid READ
- 4. Read Address 0x7C1F Valid READ
- 5. Read Address 0x703F Valid READ
- 6. Read Address 0x4B46 AutoStore Enable

If the AutoStore function is disabled or re-enabled, a manual STORE operation (Hardware or Software) is issued to save the AutoStore state through subsequent power down cycles. The part comes from the factory with AutoStore enabled.

Data Protection

The CY14B101K protects data from corruption during low voltage conditions by inhibiting all externally initiated STORE and WRITE operations. The low voltage condition is detected when V_{CC} is less than V_{SWITCH} . If the CY14B101K is in a WRITE mode (both \overline{CE} and \overline{WE} LOW) at power up, after a RECALL or after a STORE, the WRITE is inhibited until a negative transition on \overline{CE} or \overline{WE} is detected. This protects against inadvertent writes during power up or brownout conditions.

Noise Considerations

The CY14B101K is a high speed memory and so must have a high frequency bypass capacitor of approximately 0.1 μF connected between V_{CC} and V_{SS}, using leads and traces that are as short as possible. As with all high speed CMOS ICs, careful routing of power, ground, and signals reduce circuit noise.



Table 1. Mode Selection

CE	WE	OE	A15 – A0	Mode	ю	Power
Н	Х	Х	Х	Not Selected	Output High Z	Standby
L	Н	L	Х	READ SRAM	Output Data	Active
L	L	Х	Х	WRITE SRAM	Input Data	Active
L	Н	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8B45	READ SRAM READ SRAM READ SRAM READ SRAM READ SRAM AutoStore Disable	Output Data Output Data Output Data Output Data Output Data Output Data	Active ^[1, 2, 3]
L	Н	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4B46	READ SRAM READ SRAM READ SRAM READ SRAM Read SRAM AutoStore Enable	Output Data Output Data Output Data Output Data Output Data Output Data	Active ^[1, 2, 3]
L	Н	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile Store	Output Data Output Data Output Data Output Data Output Data Output High Z	Active I _{CC2} ^[1, 2, 3]
L	Н	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile Recall	Output Data Output Data Output Data Output Data Output Data Output High Z	Active ^[1, 2, 3]

Notes

 The six consecutive address locations are in the order listed. WE is HIGH during all six cycles to enable a nonvolatile cycle.
 While there are 17 address lines on the CY14B101K, only the lower 16 lines are used to control software modes.
 O state depends on the state of OE. The IO table shown is based on OE Low.



Low Average Active Power

CMOS technology provides the CY14B101K the benefit of drawing significantly less current when it is cycled at times longer than 50 ns.

Figure 3. Current vs. Cycle Time



Figure 3 shows the relationship between I_{CC} and READ/WRITE Cycle Time. The worst case current consumption is shown for commercial temperature range, $V_{CC} = 3.6V$, and chip enable at maximum frequency. Only standby current is drawn when the chip is disabled.

The overall average current drawn by the CY14B101K depends on the following items:

- The duty cycle of chip enable
- The overall cycle rate for accesses
- The ratio of READs to WRITEs
- The operating temperature
- The V_{CC} level
- IO loading

Real Time Clock Operation

nvTIME Operation

The CY14B101K offers internal registers that contain clock, alarm, watchdog, interrupt, and control functions. Internal double buffering of the clock and the clock or timer information registers prevents accessing transitional internal clock data during a READ or WRITE operation. Double buffering also circumvents disrupting normal timing counts or clock accuracy of the internal clock while accessing clock data. Clock and Alarm Registers store data in BCD format.

Clock Operations

The clock registers maintain time up to 9,999 years in one second increments. The user sets the time to any calendar time and the clock automatically keeps track of days of the week, month, leap years, and century transitions. There are eight registers dedicated to the clock functions that are used to set time with a WRITE cycle and to READ time during a READ cycle. These registers contain the Time of Day in BCD format. Bits defined as '0' are currently not used and are reserved for future use by Cypress.

Reading the Clock

While the double buffered RTC register structure reduces the chance of reading incorrect data from the clock, halt internal updates to the CY14B101K clock registers before reading clock data to prevent the reading of data in transition. Stopping the internal register updates does not affect clock accuracy. The update process is stopped by writing a '1' to the READ bit 'R' (in the flags register at 0x1FFF0) and does not restart until a '0' is written to the READ bit. The RTC registers then READ when the internal clock continues to run. Within 20 ms after a '0' is written to the READ bit, all CY14B101K registers are simultaneously updated.

Setting the Clock

Setting the WRITE bit 'W' (in the flags register at 0x1FFF0) to a '1' halts updates to the CY14B101K registers. The correct day, date, and time are then written into the registers in 24 hour BCD format. The time written is referred to as the 'Base Time'. This value is stored in nonvolatile registers and used in calculation of the current time. Resetting the WRITE bit to '0' transfers those values to the actual clock counters, after which the clock resumes normal operation.

Backup Power

The RTC in the CY14B101K is intended for permanently powered operations. Either the V_{RTCcap} or V_{RTCbat} pin is connected depending on whether a capacitor or battery is chosen for the application. When the primary power, V_{CC}, fails and drops below V_{SWITCH}, the device switches to the backup power supply.

The clock oscillator uses very little current to maximize the backup time available from the backup source. Regardless of clock operation with the primary source removed, the data stored in nvSRAM is secure, as it is stored in the nonvolatile elements when power was lost.

During backup operation, the CY14B101K consumes a maximum of 300 nA at 2V. According to the application, the user chooses the capacitor or battery values.

Backup time values, based on maximum current specifications, are shown in the following table. Nominal times are approximately three times longer.

Capacitor Value	Backup Time
0.1F	72 hours
0.47F	14 days
1.0F	30 days



Using a capacitor has the obvious advantage of recharging the backup source each time the system is powered up. If a battery is used, use a 3V lithium and the CY14B101K only source current from the battery when the primary power is removed. However, the battery does not recharge at any time by the CY14B101K. The battery capacity is chosen for total anticipated cumulative downtime required over the life of the system.

Stopping and Starting the Oscillator

The OSCEN bit in the calibration register at 0x1FFF8 controls the starting and stopping of the oscillator. This bit is nonvolatile and is shipped to customers in the "enabled" (set to '0<u>') state</u>. To preserve battery life when the system is in storage, OSCEN is set to a '1'. This <u>turns off</u> the oscillator circuit extending the battery life. If the OSCEN bit goes from disabled to enabled, it takes approximately 5 seconds (10 seconds max) for the oscillator to start.

The CY14B101K has the ability to detect oscillator failure. This is recorded in the OSCF (Oscillator Failed bit) of the Flags register at address 0x1FFF0. When the device is powered on (V_{CC} goes above V_{SWITCH}) the OSCEN bit is checked for "enabled" status. If the OSCEN bit is enabled and the oscillator is not active, the OSCF bit is set. The user must check for this condition and then WRITE a '0' to clear the flag. In addition to setting the OSCF flag bit, the time registers are reset to the "Base Time" (see the section "Setting the Clock" on page 6): the value that is last written to the time keeping registers. The Control or Calibration register and the OSCEN bit are not affected by the oscillator failed condition.

If the voltage on the backup supply (either V_{RTCcap} or V_{RTCbat}) falls below their minimum level, the oscillator may fail. This may lead to the oscillator failed condition that is detected when system power is restored.

The value of OSCF is reset to '0' when the time registers are written for the first time. This initializes the state of this bit that is set when the system is first powered on.

Calibrating the Clock

The RTC is driven by a quartz controlled oscillator with a nominal frequency of 32.768 kHz. Clock accuracy depends on the quality of the crystal usually specified to 35 ppm limits at 25°C. This error equates to +1.53 minutes in accordance with the month. The CY14B101K employs a calibration circuit that improves the accuracy to +1/–2 ppm at 25°C. The calibration circuit adds or subtracts counts from the oscillator divider circuit.

The number of pulses that are suppressed (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five calibration bits found in calibration register at 0x1FFF8. Adding counts speeds the clock up and subtracting counts slows the clock down. The calibration bits occupy the five lower order bits in the Control register 8. Set these bits to represent any value between 0 and 31 in binary form. Bit D5 is a sign bit, where a '1' indicates positive calibration and a '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once in accordance with minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles.

If a binary '1' is loaded into the register, only the first two minutes of the 64 minute cycle are modified. If a binary 6 is loaded, the

To determine how to set the calibration one may set the CAL bit in the flags register at 0x1FFF0 to '1' that causes the INT pin to toggle at a nominal 512 Hz. Any deviation measured from the 512 Hz indicates the degree and direction of the required correction. For example, a reading of 512.010124 Hz indicates a +20 ppm error, requiring to load a -10 (001010) into the Calibration register. Note that setting or changing the calibration register does not affect the frequency test output frequency.

Alarm

The alarm function compares user programmed values to the corresponding time-of-day values. When a match occurs, the alarm event occurs. The alarm drives an internal flag, AF, and may drive the INT pin if required.

There are four alarm match fields. They are date, hours, minutes, and seconds. Each of these fields also has a match bit that is used to determine if the field is used in the alarm match logic. Setting the match bit to '0' indicates that the corresponding field is used in the match process.

Depending on the match bits, the alarm occurs as specifically as one particular second on one day of the month or as frequently as once in accordance with second continuously. The MSb of each alarm register is a match bit. Selecting none of the match bits (all 1s) indicates that no match is required. The alarm occurs every second. Setting the match select bit for seconds to '0' causes the logic to match the seconds alarm value to the current time of day. Since a match occurs for only one value in accordance with minute, the alarm occurs once in accordance with minute. Likewise, setting the seconds and minutes match bits causes an exact match of these values. Thus, an alarm occurs once in accordance with hour. Setting seconds, minutes, and hours causes a match once in accordance with day. Lastly, selecting all match values causes an exact time and date match. Selecting other bit combinations does not produce meaningful results. However, the alarm circuit must follow the functions described.

There are two ways a user can detect an alarm event. They are by reading the AF flag or monitoring the INT pin. The AF flag in the Flags register at 0x1FFF0 indicates that a date and time match has occurred. The AF bit is set to '1' when a match occurs. Reading the Flags or Control register clears the Alarm flag bit (and all others). A hardware interrupt pin is also used to detect an alarm event.

Watchdog Timer

The Watchdog Timer is a free running down counter that uses the 32 Hz clock (31.25 ms) derived from the crystal oscillator. The oscillator is running for the watchdog to function. It begins counting down from the value loaded in the Watchdog Timer register.

The counter consists of a loadable register and a free running counter. On power up, the watchdog timeout value in register 0x1FFF7 is loaded into the counter load register. Counting begins on power up and restarts from the loadable value any time the watchdog strobe (WDS) bit is set to '1'. The counter is



compared to the terminal value of '0'. If the counter reaches this value, it causes an internal flag and an optional interrupt output. You can prevent the timeout interrupt by setting WDS bit to '1' before the counter reaching '0'. This reloads the counter with the watchdog timeout value and restarts. As long as the user sets the WDS bit before the counter reaches the terminal value, the interrupt and flag never occur.

Write new time<u>out values</u> by setting the watchdog WRITE bit to '0'. When the WDW is '0' (from the previous operation), new writes to the watchdog timeout value bits D5–D0 enable to modify the timeout value. When WDW is a '1', writes to bits D5 – D0 are ignored. The WDW function enables a user to set the WDS bit without concern that the watchdog timer value is modified. A logical diagram of the watchdog timer is shown in Figure 4. Note that setting the watchdog timeout value to '0' is otherwise meaningless and disables the watchdog function.

The output of the watchdog timer is the flag bit WDF that is set if the watchdog is allowed to timeout. The flag is set upon a watchdog timeout and cleared when the Flags/Control register is Read by the user. If the watchdog timeout occurs, the user can also enable an optional interrupt source to drive the INT pin.





Power Monitor

The CY14B101K provides a power management scheme with power fail interrupt capability. It also controls the internal switch to backup power for the clock and protects the memory from low V_{CC} access. The power monitor is based on an internal band gap reference circuit that compares the V_{CC} voltage to various thresholds.

As described in the "AutoStore Operation" on page 3, when V_{SWITCH} is reached as V_{CC} decays from power loss, a data store operation is initiated from SRAM to the nonvolatile elements, securing the last SRAM data state. Power is also switched from V_{CC} to the backup supply (battery or capacitor) to operate the RTC oscillator.

When operating from the backup source, no data is read or written and the clock functions are not available to the user. The clock continues to operate in the background. Updated clock data is available to the user after VCC is restored to the device and the RECALL delay (see the section "AutoStore/Power Up RECALL" on page 16).

Interrupts

The CY14B101K provides three potential interrupt sources. They include the watchdog timer, the power monitor, and the clock or calendar alarm. Individually enable each and assign to drive the INT pin. In addition, each has an associated flag bit that the host processor uses to determine the cause of the interrupt. Some of the sources have additional control bits that determine functional behavior. In addition, the pin driver has three bits that specify its behavior when an interrupt occurs.

The three interrupts each have a source and an enable. Both the source and the enable are active (true HIGH) to generate an interrupt output. Only one source is necessary to drive the pin. The user identifies the source by reading the Flags/Control register, that contains the flags associated with each source. All flags are cleared to '0' when the register is READ. The flags are cleared only after a complete read cycle (WE HIGH). The power monitor has two programmable settings that is explained in the section "Power Monitor" on page 8.

Once an interrupt source is active, the pin driver determines the behavior of the output. It has two programmable settings as shown in the following section. Pin driver control bits are located in the Interrupts register.

According to the programming selections, the pin is driven in the backup mode for an alarm interrupt. In addition, the pin is an active LOW (open drain) or an active HIGH (push pull) driver. If programmed for operation during backup mode, it is only active LOW. Lastly, the pin provides a one shot function so that the active condition is a pulse or a level condition. In one shot mode, the pulse width is internally fixed at approximately 200 ms. This mode is intended to reset a host microcontroller. In level mode, the pin goes to its active polarity until the Flags/Control register is read by the user. This mode is used as an interrupt to a host microcontroller. The Interrupt register is initialized to 00h. The control bits are summarized as follows:

Watchdog Interrupt Enable – WIE. When set to '1', the watchdog timer drives the INT pin and an internal flag when a watchdog timeout occurs. When WIE is set to '0', the watchdog timer affects only the internal flag.

Alarm Interrupt Enable – AIE. When set to '1', the alarm match drives the INT pin and an internal flag. When set to '0', the alarm match only affects the internal flag.

Power Fail Interrupt Enable – PFE. When set to '1', the power fail monitor drives the pin and an internal flag. When set to '0', the power fail monitor affects only the internal flag.

High/Low – **H/L**. When set to a '1', the INT pin is active HIGH and the driver mode is push pull. The INT pin drives high only when $V_{CC} > V_{SWITCH}$. When set to a '0', the INT pin is active LOW and the drive mode is open drain. Active LOW (open drain) is operational even in battery backup mode.

Pulse/Level – P/L. When set to a '1' and an interrupt occurs, the INT pin is driven for approximately 200 ms. When P/L is set to a '0', the INT pin is driven high or low (determined by H/L) until the Flags/Control register is READ.



When an enabled interrupt source activates the INT pin, an external host can READ the Flags or Control registers to determine the cause. Remember that all flags are cleared when the register is READ. If the INT pin is programmed for Level mode, then the condition clears and the INT pin returns to its inactive state. If the pin is programmed for Pulse mode, then reading the flag also clears the flag and the pin. The pulse does not complete its specified duration if the Flags or Control registers are READ. If the INT pin is used as a host reset, then the Flags or Control registers must not be READ during a reset.

During a power on reset with no battery, the Interrupt register is automatically loaded with the value 24h. This enables power fail interrupt with an active LOW pulse.

Flags Register – The Flags register has three flag bits: WDF, AF, and PF. These flag bits are initialized to 00h. These flags are set by the watchdog timeout, alarm match, or power fail monitor, respectively. The processor either polls this register or enables to inform interrupts when a flag is set. The flags are automatically reset once the register is READ.

Figure 5. RTC Recommended Component Configuration



Recommended Values Y1 = 32.768 KHz RF = 10 M Ω

C1 = 0 C2 = 56 pF





H/L - High/Low



Table 3. RTC Register Map

Pogistor	BCD Format Data								Function/Pange
Register	D7	D6	D5	D4	D3	D2	D1	D0	Function/Kange
0x1FFFF		10s	Years			Y	ears		Years: 00 – 99
0x1FFFE	0	0	0	10s Months	Months				Months: 01 – 12
0x1FFFD	0	0	10s Day	of Month		Day C	Of Month		Day of Month: 01 – 31
0x1FFFC	0	0	0	0	0		Day of w	eek	Day of week: 01 – 07
0x1FFFB	0	0	10s H	lours		H	ours	Hours: 00 – 23	
0x1FFFA	0	1	0s Minute	s	Minutes				Minutes: 00 – 59
0x1FFF9		1	0s Secono	ds		Se	Seconds: 00 – 59		
0x1FFF8	OSCEN	0	Cal Sign			Calibrati	Calibration Values ^[4]		
0x1FFF7	WDS	WDW			V	VDT			Watchdog ^[4]
0x1FFF6	WIE	AIE	PFE	0	H/L	P/L	0	0	Interrupts ^[4]
0x1FFF5	M	0	10s Alar	rm Date		Alar	m Day		Alarm, Day of Month: 01 – 31
0x1FFF4	M	0	10s Aları	m Hours		Alarn	n Hours		Alarm, Hours: 00 – 23
0x1FFF3	M	10 /	Alarm Min	utes	Alarm Minutes				Alarm, Minutes: 00 – 59
0x1FFF2	M	10 /	Alarm Min	utes		Alarm,	Alarm, Seconds: 00 – 59		
0x1FFF1		10s Ce	enturies			Cer	nturies		Centuries: 00 – 99
0x1FFF0	WDF	AF	PF	OSCF	0	CAL	W	R	Flags ^[4]

Table 4. Register Map Detail

	Time Keeping – Years										
	D7	D6	D5	D4	D3	D2	D1	D0			
0x1FFFF		10s	Years			Ye	ears				
	Contains the the value for	Contains the lower two BCD digits of the year. Lower nibble contains the value for years and upper nibble contains the value for 10s of years. Each nibble operates from 0 to 9. The range for the register is $0 - 99$.									
	Time Keeping – Months										
	D7	D6	D5	D4	D3	D2	D1	D0			
0x1FFFE	0x1FFFE 0 0 10s Month Months					onths					
	Contains the BCD digits of the month. Lower nibble contains the lower digit and operates from 0 to 9 and upper nibble (one bit) contains the upper digit and operates from 0 to 1. The range for the register is $1 - 12$.										
		Time Keeping – Date									
	D7	D6	D5	D4	D3	D2	D1	D0			
0x1FFFD	0	0	10s Day	of Month	Day of Month						
	Contains the BCD digits for the date of the month. Lower nibble contains the lower digit and operates from 0 to 9 and upper nibble contains the upper digit and operates from 0 to 3. The range for the register is $1 - 31$. Leap years are automatically adjusted for.										
				Time Keep	ing – Day						
	D7	D6	D5	D4	D3	D2	D1	D0			
0x1FFFC	0	0	0	0	0		Day of Weel	K			
	Lower nibble 1 to 7 then re	contains a val eturns to 1. The	ue that correlate e user must ass	es to day of the ign meaning to	week. Day of the day value	the week is a e, as the day is	ring counter the s not integrate	hat counts from d with the date.			

Note

4. This register contains a binary, not BCD, value.



Table 4. Register Map Detail (continued)

	Time Keeping – Hours									
	D7	D6	D5	D4	D3	D2	D1	D0		
0x1FFFB	12/24 0 10s Hours Hours									
	Contains the BCD value of hours in 24 hour format. Lower nibble contains the lower digit and operates from 0 to 9 and upper nibble (two bits) contains the upper digit and operates from 0 to 2. The range for the register is $0 - 23$.									
	Time Keeping – Minutes									
	D7	D6	D5	D4	D3	D2	D1	D0		
0x1FFFA	0		10s Minutes			Mir	nutes			
	Contains the BCD value of minutes. Lower nibble contains the lower digit and operates from 0 to 9 and u contains the upper minutes digit and operates from 0 to 5. The range for the register is $0 - 59$.							nd upper nibble		
				Time Keepin	g – Seconds					
	D7	D6	D5	D4	D3	D2	D1	D0		
0x1FFF9	0		10s Seconds			Sec	conds			
	Contains the contains the	BCD value of s upper digit and	seconds. Lower d operates from	nibble contains 0 to 5. The rar	the lower dig	it and operates jister is 0 – 59.	s from 0 to 9 ai	nd upper nibble		
				Calibratio	n/Control					
0X1FFF8	D7	D6	D5	D4	D3	D2	D1	D0		
	OSCEN 0 Calibration Calibration Sign									
OSCEN	Oscillator En saves batter	able. When se y/capacitor pov	t to 1, the oscill ver during stora	ator is halted. \ ge. On a no ba	When set to 0, attery power u	, the oscillator p, this bit is se	runs. Disablin t to 0.	g the oscillator		
Calibration Sign	Determines i	f the calibration	n adjustment is	applied as an a	addition to or a	as a subtractio	n from the tim	ne base.		
Calibration	These five bi	its control the c	alibration of the	e clock.						
				WatchDo	og Timer					
0x1FFF7	D7	D6	D5	D4	D3	D2	D1	D0		
	WDS	WDW			WI	DT				
WDS	Watchdog Strobe. Setting this bit to 1 reloads and restarts the watchdog timer. Setting the bit to 0 has no affect. The bit is cleared automatically once the watchdog timer is reset. The WDS bit is WRITE only. Reading it always returns a 0.									
WDW	Watchdog Write Enable. Setting this bit to 1 masks the watchdog timeout value (WDT5–WDT0) so it is not written. This enables the user to strobe the watchdog without disturbing the timeout value. Setting this bit to 0 allows bits 5 – 0 to be written on the next WRITE to the watchdog register. The new value is loaded on the next internal watchdog clock after the WRITE cycle is complete. This function is explained in more detail in the "Watchdog Timer" on page 7.									
WDT	Watchdog Ti a multiplier o maximum tin bits are writte	meout Selectio f the 32 Hz cou neout is 2 seco en only if the W	n. The watchdo Int (31.25 ms). nds (setting of 3 /DW bit is clear	g timer interval The minimum r 3 Fh). Setting tl ed to 0 on a pr	is selected by ange or timeo ne watchdog t evious cycle.	the 6-bit value ut value is 31.2 imer register to	e in this registe 25 ms (a settir 5 0 disables th	er. It represents ng of 1) and the ne timer. These		



Table 4. Register Map Detail (continued)

	Interrupt Status/Control									
0x1FFF6	D7	D6	D5	D4	D3	D2	D1	D0		
	WIE	AIE	PFIE	0	H/L	P/L	0	0		
WIE	Watchdog Interrupt Enable. When set to 1 and a watchdog timeout occurs, the watchdog timer drives the INT pin and the WDF flag. When set to 0, the watchdog timeout affects only the WDF flag.									
AIE	Alarm Interru match only a	Alarm Interrupt Enable. When set to 1, the alarm match drives the INT pin and the AF flag. When set to 0, the alarm match only affects the AF flag.								
PFIE	Power Fail E monitor affect	Power Fail Enable. When set to 1, the alarm match drives the INT pin and the AF flag. When set to 0, the power fail monitor affects only the PF flag.								
0	Reserved for	future use.								
H/L	High/Low. W	hen set to a 1,	the INT pin is o	driven active hig	h. When set t	to 0, the INT p	in is open dra	in, active LOW.		
P/L	Pulse/Level. 200 ms. Whe	When set to a 1 In set to a 0, the	l , the INT pin is INT pin is drive	driven active (de n to an active lev	etermined by H vel (as set by H	H/L) by an inter H/L) until the Fl	rupt source fo ags/Control re	r approximately egister is READ.		
				Alarm	– Day					
	D7	D6	D5	D4	D3	D2	D1	D0		
0,11113	M	0	10s Ala	rm Date		Alarr	m Date			
	Contains the alarm value for the date of the month and the mask bit to select or deselect the date value.									
M	Match. Setting this bit to 0 causes the date value to use the alarm match. Setting this bit to 1 causes the match circuit to ignore the date value.									
				Alarm –	Hours					
0x1FFF4	D7	D6	D5	D4	D3	D2	D1	D0		
UXIIII 4	M 0 10s Alarm Hours Alarm Hours									
	Contains the alarm value for the hours and the mask bit to select or deselect the hours value.									
M	Match. Settir circuit to igno	ng this bit to 0 o ore the hour va	causes the hou lue.	rs value to use	the alarm mat	ch. Setting thi	s bit to 1 caus	ses the match		
	Alarm – Minutes									
0x1FFF3	D7	D6	D5	D4	D3	D2	D1	D0		
0,11113	M 0 10s Alarm Minutes Alarm Minutes									
	Contains the	alarm value fo	or the minutes a	ind the mask bit	to select or c	leselect the m	inutes value.			
М	Match. Settir circuit to igno	ng this bit to 0 core the minute	auses the minuvalue.	utes value to us	e the alarm m	atch. Setting t	his bit to 1 ca	uses the match		
				Alarm – S	Seconds					
0x1FFF2	D7	D6	D5	D4	D3	D2	D1	D0		
•	М	0	10s Alarm	n Seconds		Alarm	Seconds			
	Contains the	alarm value fo	or the seconds a	and the mask bi	t to select or o	deselect the se	econd value.			
M	Match. Settir circuit to igno	ng this bit to 0 o bre the second	causes the seco value.	ond value to use	e the alarm m	atch. Setting the	his bit to 1 cat	uses the match		
				Time Keeping	– Centuries					
0x1FFF1	D7	D6	D5	D4	D3	D2	D1	D0		
	0	0	10s Ce	enturies		Cer	nturies			



Table 4. Register Map Detail (continued)

	Flags							
0x1FFF0	D7	D6	D5	D4	D3	D2	D1	D0
	WDF	AF	PF	OSCF	0	CAL	W	R
WDF	Watchdog Timer Flag. This READ only bit is set to 1 when the watchdog timer is allowed to reach 0 without being reset by the user. It is cleared to 0 when the Flags/Control register is READ.							
AF	Alarm Flag. This READ only bit is set to 1 when the time and date match the values stored in the alarm registers with the match bits = 0. It is cleared when the Flags/Control register is READ.							
PF	Power Fail Flag. This READ only bit is set to 1 when power falls below the power fail threshold V _{SWITCH} . It is cleared to 0 when the Flags/Control register is READ.							
OSCF	Oscillator Fail Flag. Set to 1 on power up only if the oscillator is not running in the first 5 ms of power on operation. This indicates that time counts are no longer valid. The user must reset this bit to 0 to clear this condition. The chip does not clear this flag. This bit survives power cycles.							
CAL	Calibration Mode. When set to 1, a 512 Hz square wave is output on the INT pin. When set to 0, the INT pin resumes normal operation. This bit defaults to 0 (disabled) on power up.							
W	Write Time. Setting the W bit to 1 freeze updates of the timekeeping registers. The user can then WRITE them with updated values. Setting the W bit to 0 causes the transfer of contents of the time registers to the timekeeping counters. The W bit enables writes to RTC, Alarm, Calibration, Interrupt, and Flag registers. ^[5]							
R	READ Time. register. The from 0 to 1 c	Setting the R I user can then auses the time	bit to 1 copies a READ without keeping captu	static image of concerns over o re, so the bit mu	the time keep changing valu ist be returne	bing registers a es causing sy d to 0 before r	and places the stem errors. T reading again.	em in a holding The R bit going



Maximum Ratings

Exceeding maximum ratings may impair the useful life of device. These user guidelines are not tested.

Storage Temperature65°C to +150°C
Ambient Temperature with Power Applied55°C to +125°C
Supply Voltage on V_{CC} Relative to GND0.5V to 4.1V
Voltage Applied to Outputs in High Z State0.5V to V _{CC} + 0.5V
Input Voltage0.5V to Vcc + 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential–2.0V to V _{CC} + 2.0V

Package Power Dissipation Capability ($T_A = 25^{\circ}C$)	1.0W
Surface Mount Pb Soldering Temperature (3 Seconds)	+260°C
Output Short Circuit Current [6]	15 mA
Static Discharge Voltage (MIL-STD-883, Method 3015)	> 2001V
Latch Up Current	> 200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	2.7V to 3.6V
Industrial	–40°C to +85°C	2.7V to 3.6V

DC Electrical Characteristics

Over the Operating Range (VCC = 2.7V to 3.6V) ^[7, 8, 9]

Parameter	Description	Test Conditions		Min	Max	Unit
I _{CC1}	Average V _{CC} Current	$t_{RC} = 25 \text{ ns}$ $t_{RC} = 35 \text{ ns}$ $t_{RC} = 45 \text{ ns}$	Commercial		65 55 50	mA mA mA
		Dependent on output loading and cycle rate. Values obtained without output loads. $I_{OUT} = 0$ mA.	Industrial		55 (t _{RC} = 45 ns)	mA mA mA
I _{CC2}	Average V _{CC} Current during STORE	All Inputs Do Not Care, V _{CC} = Max Average current for duration t _{STORE}			6	mA
I _{CC3}	Average V _{CC} Current at t _{AVAV} = 200 ns, 3V, 25°C Typical	WE > (V _{CC} – 0.2). All other inputs cyclir Dependent on output loading and cycle Values obtained without output loads.		10	mA	
I _{CC4}	Average V _{CAP} Current during AutoStore Cycle	All Inputs Do Not Care, V _{CC} = Max Average current for duration t _{STORE}			3	mA
I _{SB}	V _{CC} Standby Current	$\overline{\text{WE}}$ > (V _{CC} – 0.2). All others V _{IN} < 0.2V > (V _{CC} –0.2V). Standby current level after cycle is complete. Inputs are static. f = 0 MHz	or r nonvolatile		3	mA
I _{IX}	Input Leakage Current	$V_{CC} = Max, V_{SS} \le V_{IN} \le V_{CC}$		-1	+1	μA
I _{OZ}	Off State Output Leakage Current	$V_{CC} = Max, V_{SS} \le V_{IN} \le V_{CC}, \overline{CE} \text{ or } \overline{OE}$	> V _{IH}	-1	+1	μA
V _{IH}	Input HIGH Voltage ^[10]			2.0	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage			$V_{SS} - 0.5$	0.8	V
V _{OH}	Output HIGH Voltage	$I_{OUT} = -2 \text{ mA}$		2.4		V
V _{OL}	Output LOW Voltage	I _{OUT} = 4 mA		0.4	V	
V _{CAP}	Storage Capacitor	Between V_{CAP} pin and V_{SS} , 5V rated		17	120	μF

Notes

6. Outputs shorted for no more than one second. No more than one output is shorted at a time.

7. Typical conditions for the active current shown at the beginning of the data sheet are average values at 25°C (room temperature) and V_{CC} = 3V. Not 100% tested.

8. The HSB pin has $I_{OUT} = -10 \ \mu$ A for V_{OH} of 2.4 V, this parameter is characterized but not tested.

9. The INT pin is open drain and does not source or sink current when interrupt register bit D3 is low.

10. V_{IH} changes by 100 mV when V_{CC} > 3.5V.



Capacitance

These parameters are guaranteed but not tested.

Parameter	Description	Test Conditions	Max	Unit
C _{IN}	Input Capacitance	$T_{A} = 25^{\circ}C, f = 1 \text{ MHz},$	7	pF
C _{OUT}	Output Capacitance	$V_{CC} = 0$ to 3.0 V	7	pF

Thermal Resistance

These parameters are guaranteed but not tested.

Parameter	Description	Test Conditions	48-SSOP	Unit
Θ_{JA}	Thermal Resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in	TBD	°C/W
Θ^{JC}	Thermal Resistance (junction to case)	accordance with EIA/JESD51.	TBD	°C/W

AC Test Loads



AC Test Conditions

Input Pulse Levels	0 V to 3 V
Input Rise and Fall Times (10% - 90%)	<u><</u> 5 ns
Input and Output Timing Reference Levels	1.5 V



AC Switching Characteristics

Parameter			25 ns	25 ns Part		35 ns Part		45 ns Part	
Cypress Parameter	Alt. Parameter	Description	Min	Max	Min	Max	Min	Max	
SRAM REA	D Cycle								
t _{ACE}	t _{ACS}	Chip Enable Access Time		25		35		45	ns
t _{RC} ^[12]	t _{RC}	Read Cycle Time	25		35		45		ns
t _{AA} ^[13]	t _{AA}	Address Access Time		25		35		45	ns
t _{DOE}	t _{OE}	Output Enable to Data Valid		12		15		20	ns
t _{OHA} ^[13]	t _{OH}	Output Hold After Address Change	3		3		3		ns
t _{LZCE} ^[14]	t _{LZ}	Chip Enable to Output Active	3		3		3		ns
t _{HZCE} ^[14]	t _{HZ}	Chip Disable to Output Inactive		10		13		15	ns
t _{LZOE} [14]	t _{OLZ}	Output Enable to Output Active	0		0		0		ns
t _{HZOE} ^[14]	t _{OHZ}	Output Disable to Output Inactive		10		13		15	ns
t _{PU} ^[11]	t _{PA}	Chip Enable to Power Active	0		0		0		ns
t _{PD} ^[11]	t _{PS}	Chip Disable to Power Standby		25		35		45	ns
SRAM WRIT	TE Cycle		•			•			
t _{WC}	t _{WC}	Write Cycle Time	25		35		45		ns
t _{PWE}	t _{WP}	Write Pulse Width	20		25		30		ns
t _{SCE}	t _{CW}	Chip Enable To End of Write	20		25		30		ns
t _{SD}	t _{DW}	Data Setup to End of Write	10		12		15		ns
t _{HD}	t _{DH}	Data Hold After End of Write	0		0		0		ns
t _{AW}	t _{AW}	Address Setup to End of Write	20		25		30		ns
t _{SA}	t _{AS}	Address Setup to Start of Write	0		0		0		ns
t _{HA}	t _{WR}	Address Hold After End of Write	0 0		0		ns		
t _{HZWE} [14, 15]	t _{WZ}	Write Enable to Output Disable		10		13		15	ns
t _{LZWE} ^[14]	t _{OW}	Output Active after End of Write	3		3		3		ns

AutoStore/Power Up RECALL

Paramotor	Description	CY14	Unit	
Farameter	Description	Min	Max	Onit
t _{HRECALL} ^[16]	Power Up RECALL Duration		20	ms
t _{STORE} [17, 18]	STORE Cycle Duration		12.5	ms
V _{SWITCH}	Low Voltage Trigger Level		2.65	V
t _{VCCRISE}	VCC Rise Time	150		μs

Notes

- These parameters are guaranteed but not tested.
 WE must be HIGH during SRAM READ cycles.
 Device is continuously selected with CE and OE both low.
- 14. Measured ±200 mV from steady state output voltage.

- 15. If \overline{WE} is low when \overline{CE} goes low, the outputs remain in the high impedance state. 16. t_{HRECALL} starts from the time V_{CC} rises above V_{SWITCH}. 17. If an SRAM WRITE has not taken place since the last nonvolatile cycle, no STORE takes place.
- 18. Industrial grade devices require 15 ms max.



Software Controlled STORE/RECALL Cycles

In the following table, the software sequence is clocked with \overline{CE} controlled or \overline{OE} controlled READs. The six consecutive addresses must be READ in the order listed in the "Mode Selection" on page 5. WE must be HIGH during all six consecutive cycles. A 600 Ω resistor must be connected to HSB to use the software command.

Parameter	Description	25 ns Part		35 ns Part		45 ns Part		Unit
Farameter	Description	Min	Max	Min	Max	Min	Max	Onit
t _{RC}	STORE/RECALL Initiation Cycle Time	25		35		45		ns
t _{AS}	Address Setup Time	0		0		0		ns
t _{CW}	Clock Pulse Width	20		25		30		ns
t _{GHAX}	Address Hold Time	1		1		1		ns
t _{RECALL}	RECALL Duration		100		100		100	μs
t _{SS} ^[22, 23]	Soft Sequence Processing Time		70		70		70	μs

Hardware STORE Cycle

Parameter	Description	CY14B1	01K	Unit	
Farameter	Description	Min	Max	om	
t _{DELAY} ^[24]	Time Allowed to Complete SRAM Cycle	1	70	μs	
t _{HLHX}	Hardware STORE Pulse Width	15		ns	

RTC Characteristics

Parameters	Description	Test Conditions		Min	Max	Units
I _{BAK} ^[25]	RTC Backup Current		Commercial		300	nA
			Industrial		350	nA
V _{RTCbat} ^[26]	RTC Battery Pin Voltage		Commercial	1.8	3.3	V
			Industrial	1.8	3.3	V
V _{RTCcap} ^[27]	RTC Capacitor Pin Voltage		Commercial	1.2	2.7	V
			Industrial	1.2	2.7	V
tOCS	RTC Oscillator Time to Start	at Min Temperature from Power Up or Enable	Commercial		10	sec
		at 25°C Temperature from Power Up or Enable	Commercial		5	sec
		at Min Temperature from Power Up or Enable	Industrial		10	sec
		at 25°C Temperature from Power Up or Enable	Industrial		5	sec

Notes

- 19. The software sequence is clocked with \overline{CE} controlled or \overline{OE} controlled READs.
- 20. The six consecutive addresses must be READ in the order listed in the "Mode Selection" on page 5. WE must be HIGH during all six consecutive cycles.
- 21. A 600 $\!\Omega$ resistor must be connected to $\overline{\text{HSB}}$ to use the software command.

22. This is the amount of time it takes to take action on a soft sequence command. Vcc power must remain HIGH to effectively register the command.

23. Commands such as STORE and RECALL lock out IO until operation is complete which further increases this time. See the specific command.

24. READ and WRITE cycles in progress before $\overline{\text{HSB}}$ are given this amount of time to complete.

25. From either V_{RTCcap} or V_{RTCbat}.

26. Typical = 3.0V during normal operation.

27. Typical = 2.4V during normal operation.



Switching Waveforms

Figure 7 shows the SRAM Read Cycle 1(address controlled).^[12, 13, 28]



Figure 7. SRAM Read Cycle 1

Figure 8 shows the SRAM Read Cycle 2 (CE and OE controlled).^[12, 28]







Figure 9 shows the SRAM Write Cycle 1 (WE controlled). ^[28, 29]



Figure 9. SRAM WRITE Cycle 1

Figure 10 shows the SRAM Write Cycle 2 (CE controlled). [28, 29]

Figure 10. SRAM WRITE Cycle 2



Note

^{29.} \overline{CE} or \overline{WE} must be > V_{IH} during address transitions.

Figure 11. AutoStore/Power Up RECALL

In the following figure, The six consecutive addresses must be READ in the order listed in the "Mode Selection" on page 5. WE must be HIGH during all six consecutive cycles.

In the following figure, The six consecutive addresses must be READ in the order listed in the "Mode Selection" on page 5. WE must be HIGH during all six consecutive cycles.

Figure 13. OE Controlled Software STORE/RECALL Cycle

In the following figure, this is the amount of time it takes to take action on a soft sequence command. Vcc power must remain HIGH to effectively register the command. Commands such as STORE and RECALL lock out IO until operation is complete which further increases this time. See the specific command.

Part Numbering Nomenclature

Ordering Information

All mentioned parts are Pb-free. Shaded areas contain advance information. Contact your local Cypress sales representative for availability of these parts.

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
25	CY14B101K-SP25XCT	51-85061	48-pin SSOP	Commercial
	CY14B101K-SP25XC	51-85061	48-pin SSOP	
25	CY14B101K-SP25XIT	51-85061	48-pin SSOP	Industrial
	CY14B101K-SP25XI	51-85061	48-pin SSOP	
35	CY14B101K-SP35XCT	51-85061	48-pin SSOP	Commercial
	CY14B101K-SP35XC	51-85061	48-pin SSOP	
35	CY14B101K-SP35XIT	51-85061	48-pin SSOP	Industrial
	CY14B101K-SP35XI	51-85061	48-pin SSOP	
45	CY14B101K-SP45XCT	51-85061	48-pin SSOP	Commercial
	CY14B101K-SP45XC	51-85061	48-pin SSOP	
45	CY14B101K-SP45XIT	51-85061	48-pin SSOP	Industrial
	CY14B101K-SP45XI	51-85061	48-pin SSOP	

Package Diagram

Document History Page

Document Title: CY14B101K 1 Mbit (128K x 8) nvSRAM With Real Time Clock Document Number: 001-06401					
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change	
**	425138	See ECN	TUP	New data sheet	
*A	437321	See ECN	TUP	Show data sheet on External Web	
*В	471966	See ECN	TUP	$\begin{array}{l} \label{eq:component} \begin{tabular}{lllllllllllllllllllllllllllllllllll$	
*C	503272	See ECN	PCI	Changed from Advance to Preliminary Changed the term "Unlimited" to "Infinite" Changed Endurance from 500K Cycles to 200K Cycles Added temperature spec. to Data Retention - 20 years at 55×C Removed Icc ₁ values from the DC table for 25 ns and 35 ns Industrial Grade Changed Icc ₂ value from 3 mA to 6 mA in the DC Table Added a footnote on V_{IH} Added footnote 18 related to using the software command Changed $V_{SWITCH(min)}$ from 2.55V to 2.45V Updated Part Nomenclature Table and Ordering Information Table	
*D	597002	See ECN	TUP	Removed V _{SWITCH(min)} specification from the AutoStore/Power Up RECALL Table Changed t _{GLAX} specification from 20 ns to 1 ns Added t _{DELAY(max)} specification of 70 ms in the Hardware STORE Cycle Table Removed t _{HLBL} specification Changed t _{SS} specification form 70 ms (min) to 70 ms (max) Changed V _{CAP(max)} from 57 mF to 120 mF	
*E	688776	See ECN	VKN	Added footnote 7 related to HSB Added footnote 8 related to INT pin Changed t _{GLAX} to t _{GHAX} Removed ABE bit from interrupt register	
*F	1349963	See ECN	UHA/SFV	Changed from Preliminary to Final Added Note 5 regarding the W bit in the Flag register Updated Ordering Information Table	
*G	1739984	See ECN	vsutmp8/AESA	Added Pinout diagram and Pin definition Table	

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