Dual, 200mA, Low-I_Q Low-Dropout Regulator for Portable Devices

FEATURES

- **Very Low Dropout:**
  - **150mV at I_{OUT} = 200mA and V_{OUT} = 2.8V**
  - **75mV at I_{OUT} = 100mA and V_{OUT} = 2.8V**
  - **40mV at I_{OUT} = 50mA and V_{OUT} = 2.8V**
- **2% Accuracy Over Temperature**
- **Low I_Q of 35μA per Regulator**
- **Multiple Fixed Output Voltage Combinations Possible from 1.2V to 4.8V**
- **High PSRR: 70dB at 1kHz**
- **Stable with Effective Capacitance of 0.1μF(1)**
- **Over-Current and Thermal Protection**
- **Dedicated V_{REF} for Each Output Minimizes Crosstalk**
- **Available in 1.5mm × 1.5mm SON-6 Package**

(1) See the *Input and Output Capacitor Requirements* in the *Application Information* section

APPLICATIONS

- **Wireless Handsets, Smart Phones, PDAs**
- **MP3 Players and Other Handheld Products**

DESCRIPTION

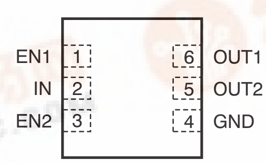
The TLV710 and TLV711 series of dual, low-dropout (LDO) linear regulators are low quiescent current devices with excellent line and load transient performance. These LDOs are designed for power-sensitive applications. These devices provide a typical accuracy of 2% over temperature.

The TLV711 series provides an active pulldown circuit to quickly discharge the outputs.

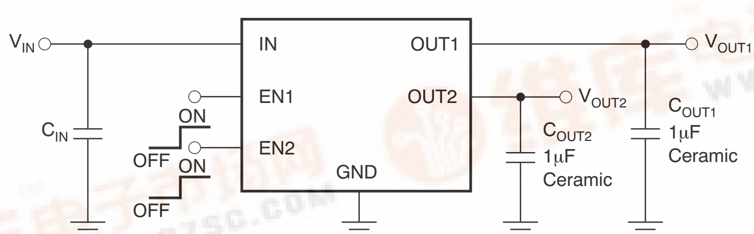
In addition, the TLV711-D series of devices have pull-down resistors at the EN pins. This design helps in disabling the device when the signal-driving EN pins are in a weak, indeterminate state (for example, the GPIO of a processor that might be three-stated during startup). The pull-down resistor pulls the voltage to the EN pins down to 0V, thus disabling the device.

The TLV710 and TLV711 series are available in a 1.5mm x 1.5mm SON-6 package, and are ideal for handheld applications.

TLV710
TLV711
1.5mm x 1.5mm SON-6
(TOP VIEW)



Typical Application Circuit



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION[1]

PRODUCT	V_{OUT} [2]
TLV710**xxyy**qwwwz TLV711**xxyy**qwwwz	**XX** is nominal output voltage of channel 1 (for example 18 = 1.8V). **YY** is nominal output voltage of channel 2 (for example 28 = 2.8V). **Q** is optional. Use "U" for devices with EN pin pull-up resistor, and "D" for devices with EN pin pull-down resistor. **WWW** is package designator. **Z** is package quantity. Use "R" for reel (3000 pieces), and "T" for tape (250 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Output voltages from 1.2V to 4.8V in 50mV increments are available through the use of innovative factory OTP programming; minimum order quantities may apply. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS[1]

At T_J = –40°C to +125°C (unless otherwise noted).

		VALUE		UNIT
		MIN	MAX	
Voltage[2]	IN	–0.3	+6.0	V
	EN	–0.3	V_{IN} + 0.3	V
	OUT	–0.3	+6.0	V
Current	OUT	Internally limited		A
Output short-circuit duration		Indefinite		s
Temperature	Operating junction, T_J	–55	+150	°C
	Storage, T_{stg}	–55	+150	°C
Electrostatic Discharge Rating	Human body model (HBM) QSS 009-105 (JESD22-A114A)		2	kV
	Charged device model (CDM) QSS 009-147 (JESD22-C101B.01)		500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages with respect to ground.

THERMAL INFORMATION[1]

THERMAL METRIC[2]		TLV710, TLV711	UNITS
		DSE	
		6 PINS	
ψ_{JT}	Junction-to-top characterization parameter	6	°C/W

(1) See the *Power Dissipation* section for more details.
(2) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

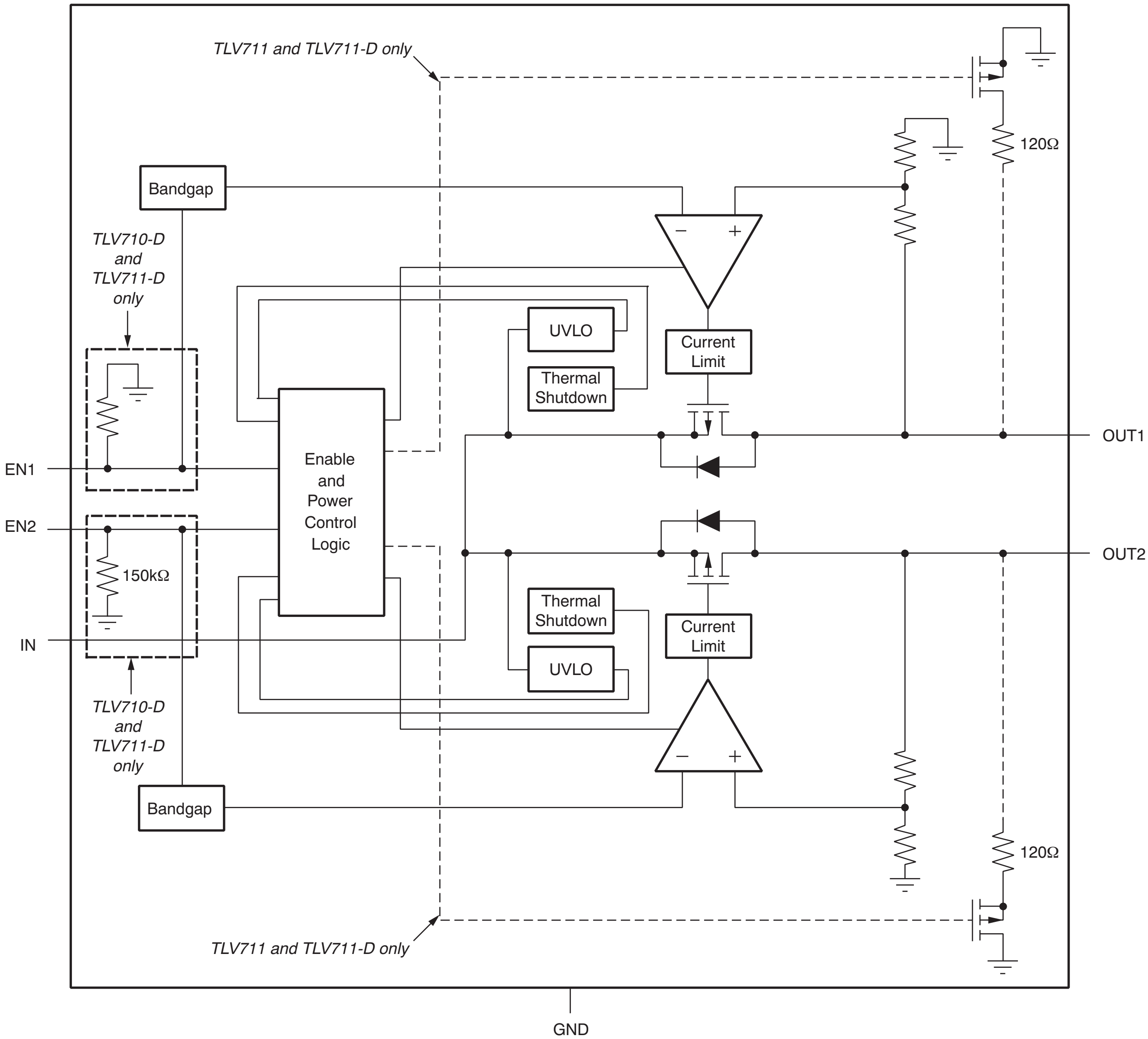
ELECTRICAL CHARACTERISTICS

At T_J = +25°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.0V (whichever is greater), I_{OUT} = 10mA, V_{EN1} = V_{EN2} = 0.9V, and C_{OUT1} = C_{OUT2} = 1μF, unless otherwise noted.

PARAMETER		TEST CONDITIONS		TLV710, TLV711 MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range			2.0		5.5	V
V_O	Output voltage range			1.2		4.8	V
V_{OUT}	DC output accuracy	–40°C ≤ T_J ≤ +125°C		–2		+2	%
$\Delta V_O/\Delta V_{IN}$	Line regulation	$V_{OUT(NOM)}$ + 0.5V ≤ V_{IN} ≤ 5.5V			1	5	mV
$\Delta V_O/\Delta I_{OUT}$	Load regulation	0mA ≤ I_{OUT} ≤ 200mA			5	15	mV
V_{DO}	Dropout voltage	V_{IN} = 0.98V × $V_{OUT(NOM)}$, I_{OUT} = 200mA, 2V ≤ V_{OUT} < 2.4V			200	285	mV
		V_{IN} = 0.98V × $V_{OUT(NOM)}$, I_{OUT} = 200mA, 2.4V ≤ V_{OUT} < 2.8V			175	250	mV
		V_{IN} = 0.98V × $V_{OUT(NOM)}$, I_{OUT} = 200mA, 2.8V ≤ V_{OUT} < 3.3V			150	215	mV
		V_{IN} = 0.98V × $V_{OUT(NOM)}$, I_{OUT} = 200mA, 3.3V ≤ V_{OUT} ≤ 4.8V			140	200	mV
I_{CL}	Output current limit	V_{OUT} = 0.9V × $V_{OUT(NOM)}$		220	350	550	mA
I_Q	Quiescent current	V_{EN1} = high, V_{EN2} = low, I_{OUT1} = 0mA			35		μA
		V_{EN1} = low, V_{EN2} = high, I_{OUT2} = 0mA			35		μA
		V_{EN1} = high, V_{EN2} = high, I_{OUT} = 0mA			70	110	μA
I_{GND}	Ground pin current	I_{OUT1} = I_{OUT2} = 200mA			360		μA
$I_{SHUTDOWN}$	Shutdown current	$V_{EN1,2}$ ≤ 0.4V, 2.0V ≤ V_{IN} ≤ 4.5V			2.5	4	μA
PSRR	Power-supply rejection ratio	V_{OUT} = 1.8V	f = 10Hz		80		dB
			f = 100Hz		75		dB
			f = 1kHz		70		dB
			f = 10kHz		70		dB
			f = 100kHz		50		dB
V_N	Output noise voltage	BW = 100Hz to 100kHz, V_{OUT} = 1.8V			48		μV_{RMS}
t_{STR}	Startup time (1)	C_{OUT} = 1.0μF, I_{OUT} = 200mA			100		μs
V_{HI}	Enable high (enabled)			0.9		V_{IN}	V
V_{LO}	Enable low (shutdown)			0		0.4	V
I_{EN}	Enable pin current, enabled	TLV710, TLV711			0.04		μA
		TLV710-D, TLV711-D			6		μA
UVLO	Undervoltage lockout	V_{IN} rising			1.9		V
T_J	Operating junction temperature			–40		+125	°C
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing			+165		°C
		Reset, temperature decreasing			+145		°C

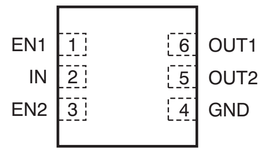
(1) Startup time = time from EN assertion to 0.98 x $V_{OUT(NOM)}$.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

DSE PACKAGE
1.5mm x 1.5mm SON-6
(TOP VIEW)



PIN DESCRIPTIONS

NAME	PIN NO.	DESCRIPTION
EN1	1	Enable pin for regulator 1. Driving EN1 over 0.9V turns on regulator 1. Driving EN below 0.4V puts regulator 1 into shutdown mode.
IN	2	Input pin. A small capacitor is needed from this pin to ground to assure stability. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.
EN2	3	Enable pin for regulator 2. Driving EN2 over 0.9V turns on regulator 2. Driving EN2 below 0.4V puts regulator2 into shutdown mode.
GND	4	Ground pin.
OUT2	5	Regulated output voltage pin. A small 1μF ceramic capacitor is needed from this pin to ground to assure stability. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.
OUT1	6	Regulated output voltage pin. A small 1μF ceramic capacitor is needed from this pin to ground to assure stability. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.

查询"TLV7101828"供应商

TYPICAL CHARACTERISTICS

Over operating temperature range of T_J = –40°C to +125°C, V_{EN1} = V_{EN2} = V_{IN}, C_{IN} = 1μF, C_{OUT1} = 1μF, and C_{OUT2} = 1μF, unless otherwise noted. Typical values are at T_J = +25°C.

LINE REGULATION: V_{OUT1} (TLV7101828)

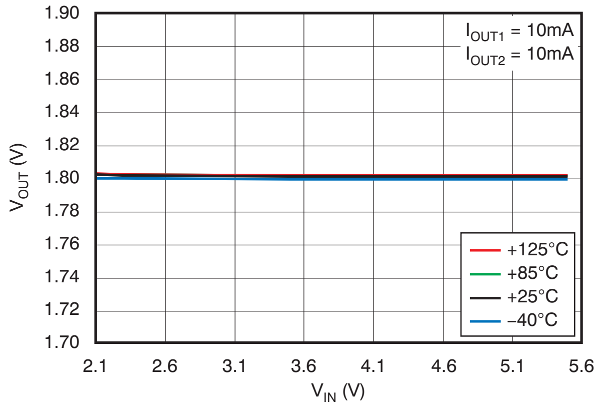


Figure 1.

LINE REGULATION: V_{OUT2} (TLV7101828)

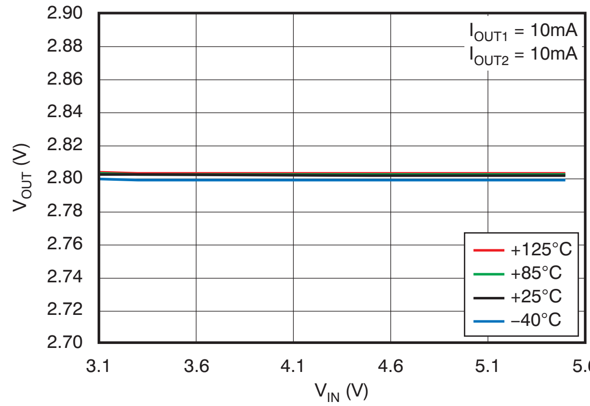


Figure 2.

LINE REGULATION: V_{OUT1} (TLV7101828)

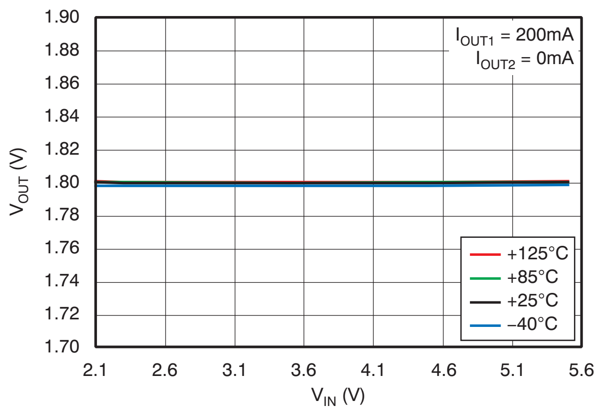


Figure 3.

LINE REGULATION: V_{OUT2} (TLV7101828)

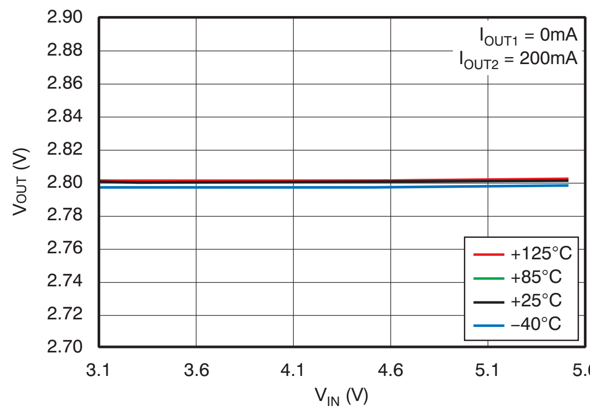


Figure 4.

LINE REGULATION: V_{OUT1} (TLV7103333)

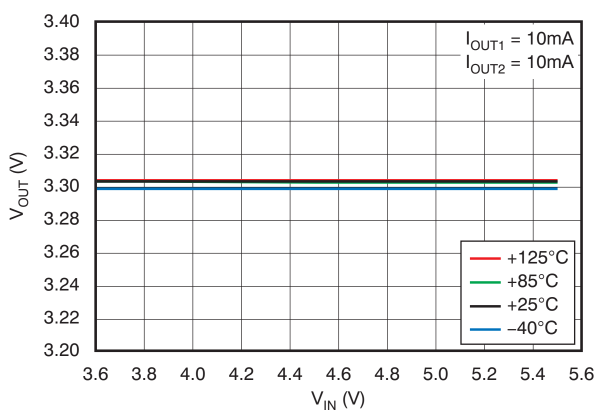


Figure 5.

LINE REGULATION: V_{OUT2} (TLV7103333)

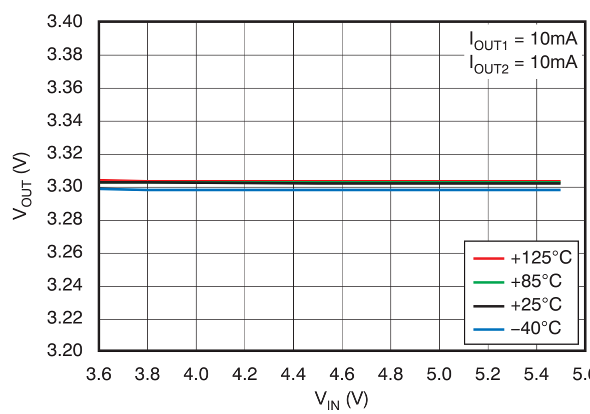


Figure 6.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of T_J = –40°C to +125°C, V_{EN1} = V_{EN2} = V_{IN}, C_{IN} = 1µF, C_{OUT1} = 1µF, and C_{OUT2} = 1µF, unless otherwise noted. Typical values are at T_J = +25°C.

LINE REGULATION: V_{OUT1} (TLV7103333)

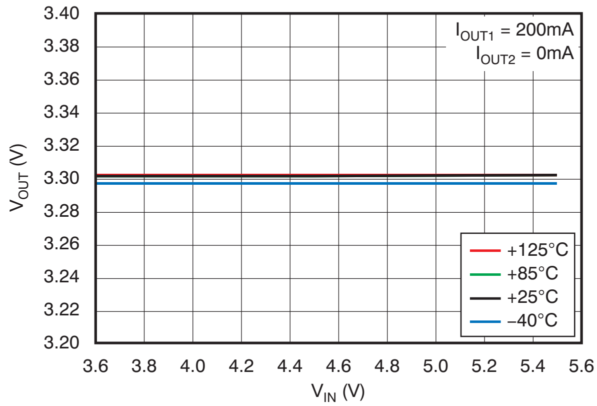


Figure 7.

LINE REGULATION: V_{OUT2} (TLV7103333)

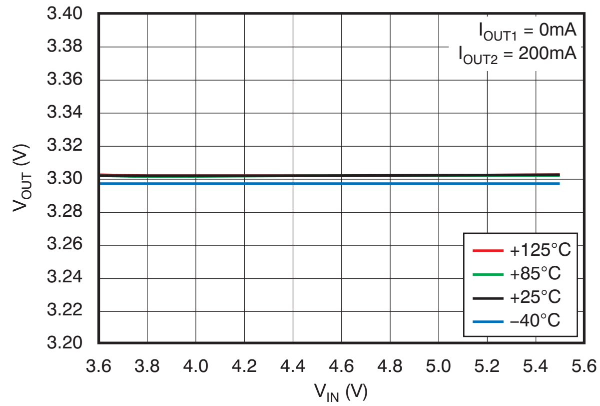


Figure 8.

LINE REGULATION: V_{OUT1} (TLV7111525)

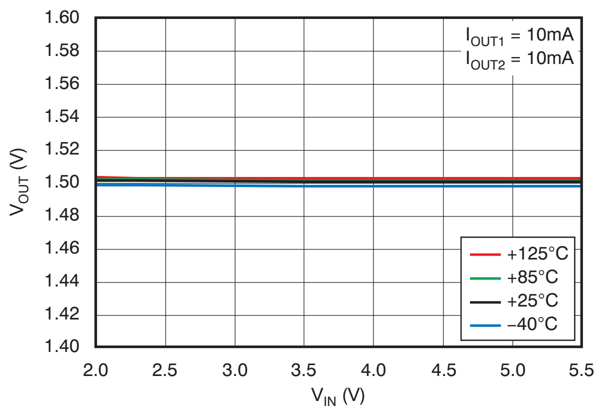


Figure 9.

LINE REGULATION: V_{OUT2} (TLV7111525)

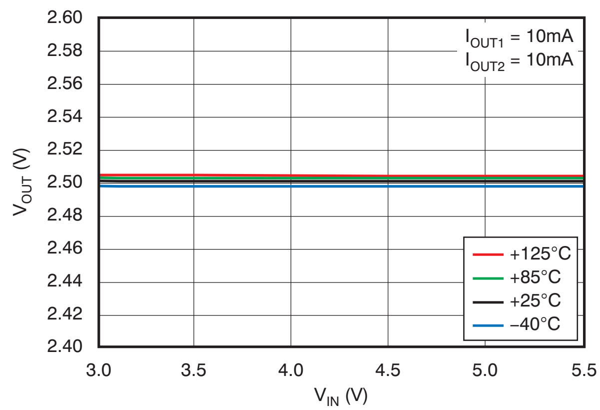


Figure 10.

LINE REGULATION: V_{OUT1} (TLV7111525)

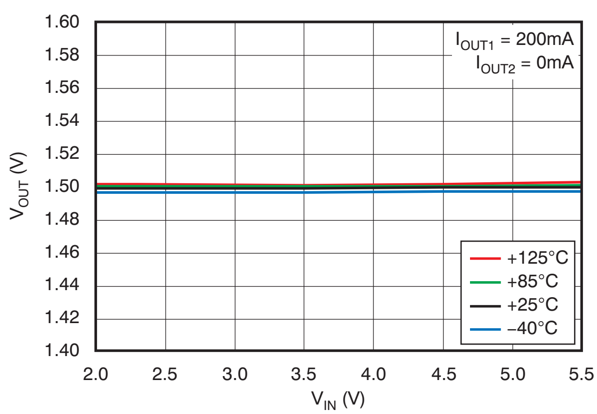


Figure 11.

LINE REGULATION: V_{OUT2} (TLV7111525)

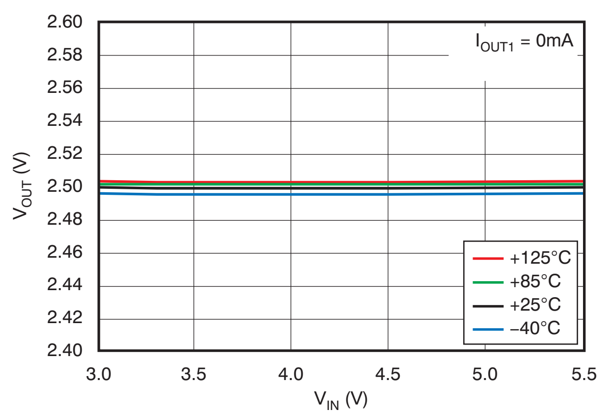


Figure 12.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of T_J = –40°C to +125°C, V_{EN1} = V_{EN2} = V_{IN}, C_{IN} = 1μF, C_{OUT1} = 1μF, and C_{OUT2} = 1μF, unless otherwise noted. Typical values are at T_J = +25°C.

LOAD REGULATION: V_{OUT1} (TLV7101828)

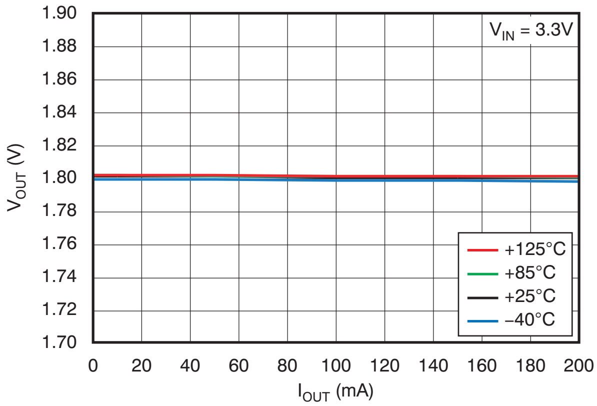


Figure 13.

LOAD REGULATION: V_{OUT2} (TLV7101828)

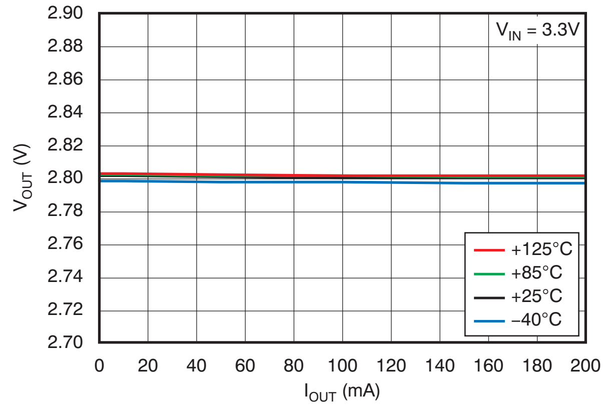


Figure 14.

LOAD REGULATION: V_{OUT1} (TLV7103333)

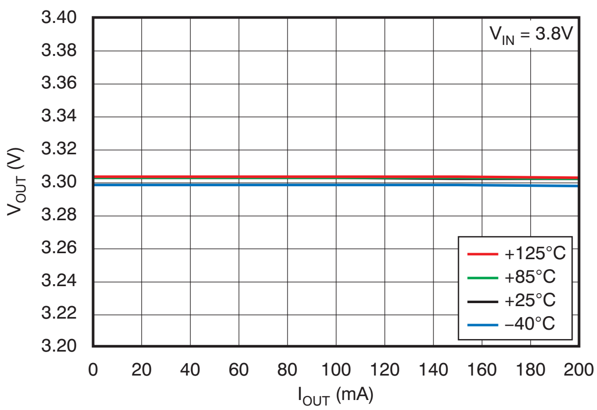


Figure 15.

LOAD REGULATION: V_{OUT2} (TLV7103333)

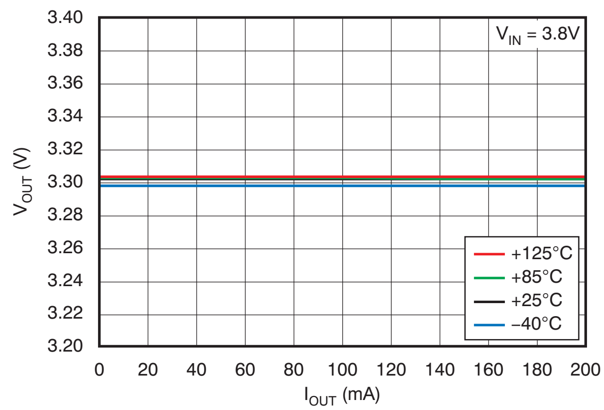


Figure 16.

LOAD REGULATION: V_{OUT1} (TLV7111525)

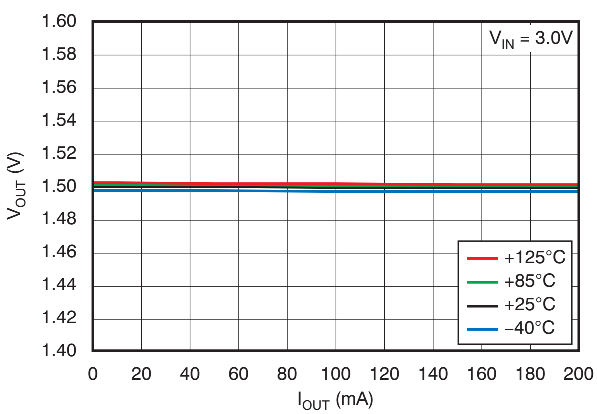


Figure 17.

LOAD REGULATION: V_{OUT2} (TLV7111525)

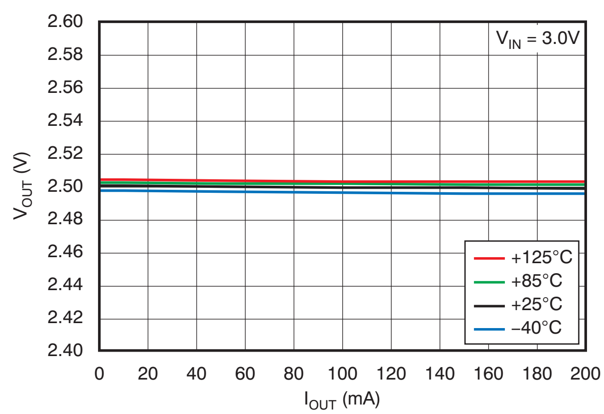


Figure 18.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of T_J = –40°C to +125°C, V_{EN1} = V_{EN2} = V_{IN}, C_{IN} = 1μF, C_{OUT1} = 1μF, and C_{OUT2} = 1μF, unless otherwise noted. Typical values are at T_J = +25°C.

DROPOUT VOLTAGE vs INPUT VOLTAGE

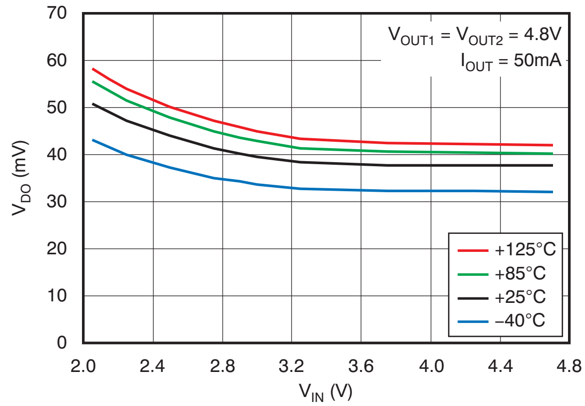


Figure 19.

DROPOUT VOLTAGE vs INPUT VOLTAGE

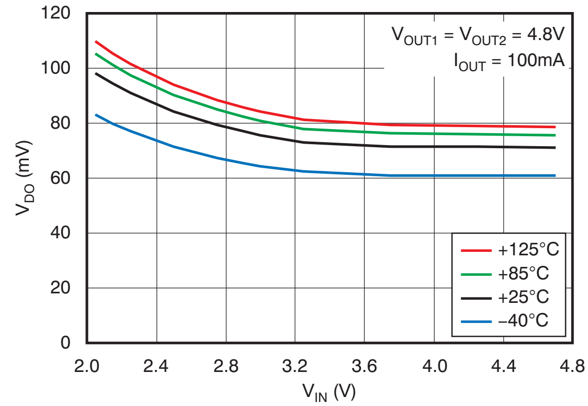


Figure 20.

DROPOUT VOLTAGE vs INPUT VOLTAGE

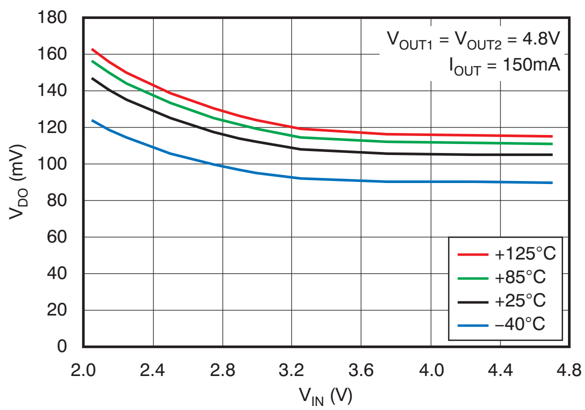


Figure 21.

DROPOUT VOLTAGE vs INPUT VOLTAGE

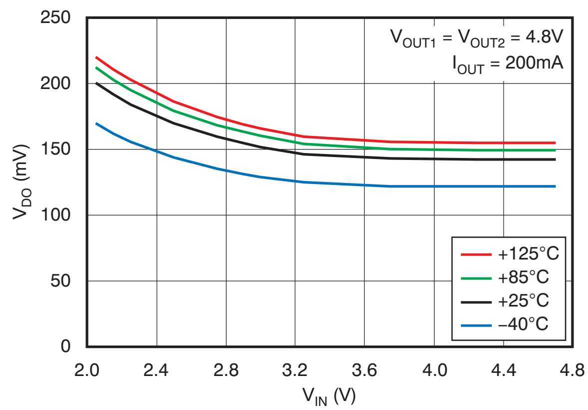


Figure 22.

DROPOUT VOLTAGE vs OUTPUT CURRENT: V_{OUT2} (TLV7101828)

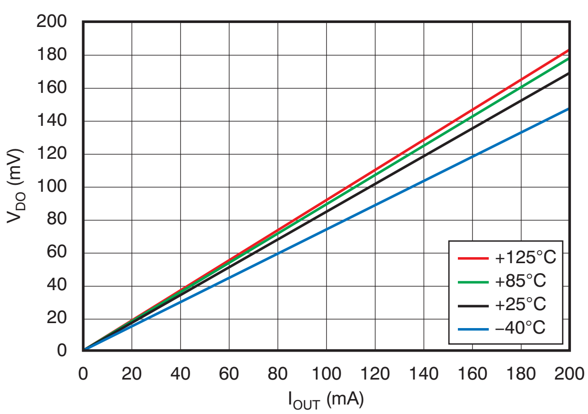


Figure 23.

DROPOUT VOLTAGE vs OUTPUT CURRENT: V_{OUT1}/V_{OUT2} (TLV7103333)

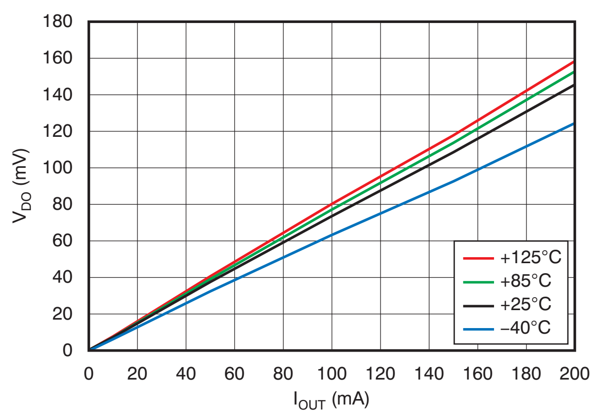


Figure 24.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of T_J = –40°C to +125°C, $V_{EN1} = V_{EN2} = V_{IN}$, C_{IN} = 1μF, C_{OUT1} = 1μF, and C_{OUT2} = 1μF, unless otherwise noted. Typical values are at T_J = +25°C.

DROPOUT VOLTAGE vs OUTPUT CURRENT: V_{OUT2} (TLV7111525)

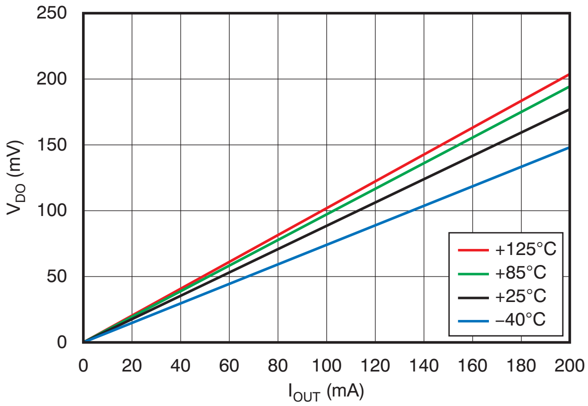


Figure 25.

OUTPUT VOLTAGE vs TEMPERATURE: V_{OUT1} (TLV7101828)

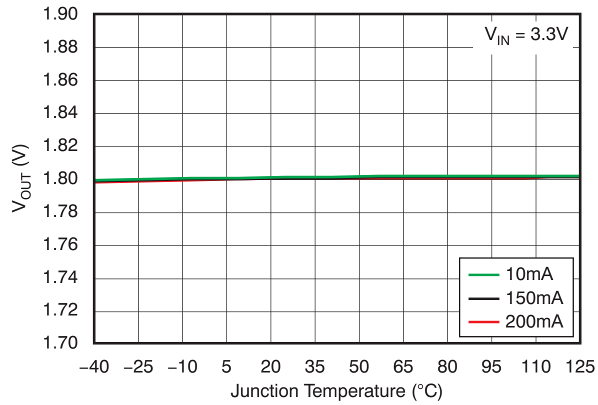


Figure 26.

OUTPUT VOLTAGE vs TEMPERATURE: V_{OUT2} (TLV7101828)

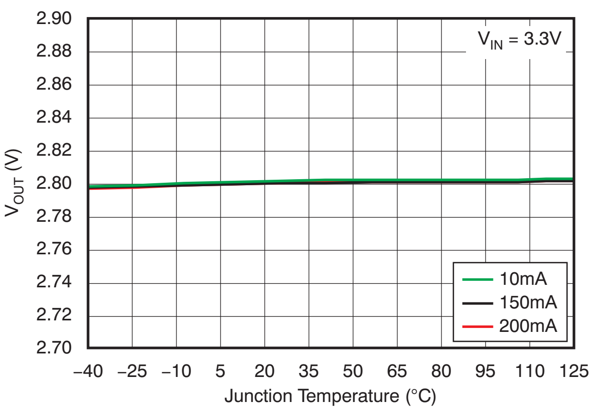


Figure 27.

OUTPUT VOLTAGE vs TEMPERATURE: V_{OUT1} (TLV7103333)

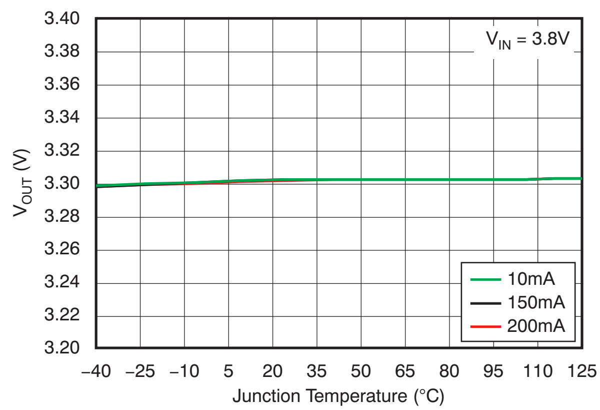


Figure 28.

OUTPUT VOLTAGE vs TEMPERATURE: V_{OUT2} (TLV7103333)

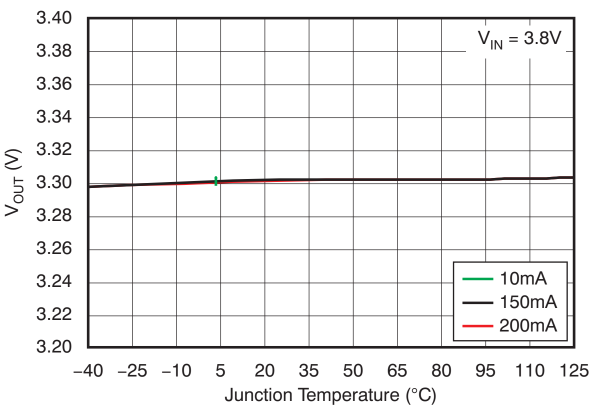


Figure 29.

OUTPUT VOLTAGE vs TEMPERATURE: V_{OUT1} (TLV7111525)

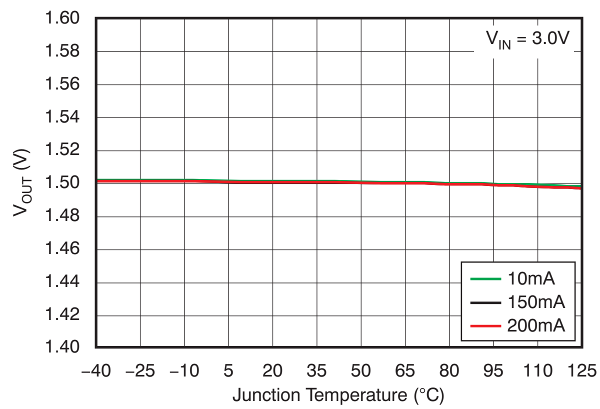


Figure 30.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of T_J = –40°C to +125°C, V_{EN1} = V_{EN2} = V_{IN}, C_{IN} = 1µF, C_{OUT1} = 1µF, and C_{OUT2} = 1µF, unless otherwise noted. Typical values are at T_J = +25°C.

OUTPUT VOLTAGE vs TEMPERATURE: V_{OUT2} (TLV7111525)

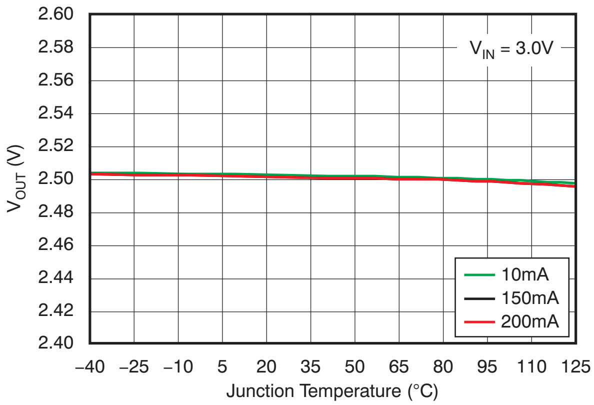


Figure 31.

GROUND PIN CURRENT vs INPUT VOLTAGE: I_{Q1} (TLV7101828)

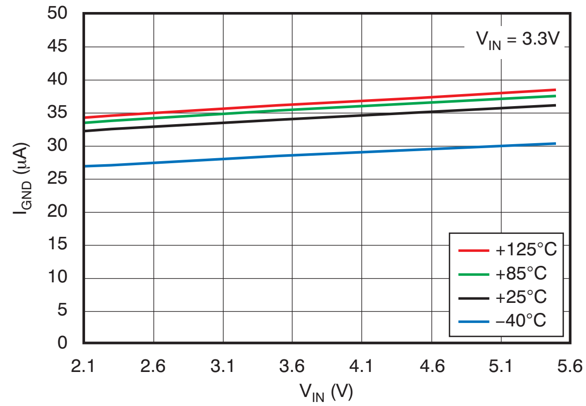


Figure 32.

GROUND PIN CURRENT vs INPUT VOLTAGE: I_{Q2} (TLV7101828)

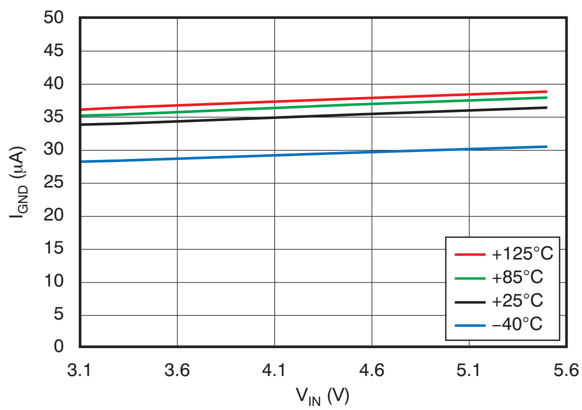


Figure 33.

GROUND PIN CURRENT vs INPUT VOLTAGE: I_{Q1} (TLV7103333)

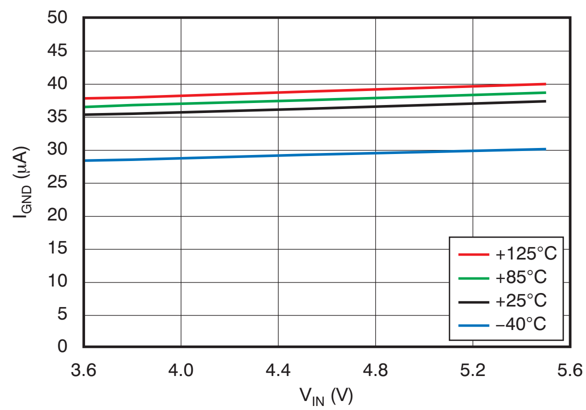


Figure 34.

GROUND PIN CURRENT vs INPUT VOLTAGE: I_{Q2} (TLV7103333)

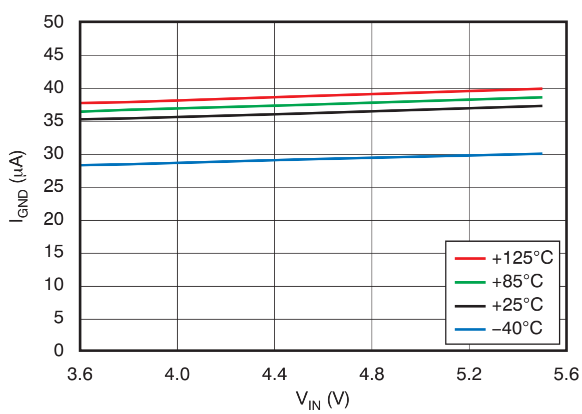


Figure 35.

GROUND PIN CURRENT vs INPUT VOLTAGE: I_{Q1} (TLV7111525)

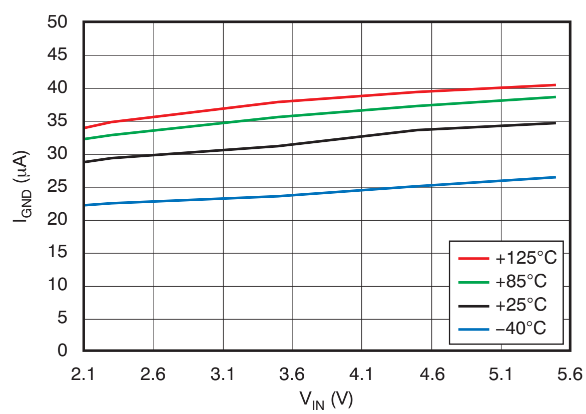


Figure 36.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of T_J = –40°C to +125°C, $V_{EN1} = V_{EN2} = V_{IN}$, C_{IN} = 1µF, C_{OUT1} = 1µF, and C_{OUT2} = 1µF, unless otherwise noted. Typical values are at T_J = +25°C.

GROUND PIN CURRENT vs INPUT VOLTAGE: I_{Q2} (TLV7111525)

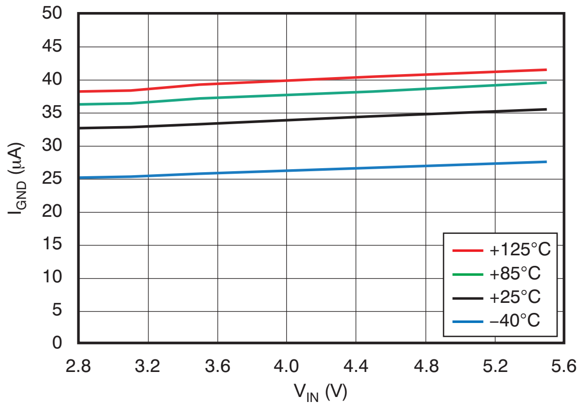


Figure 37.

GROUND PIN CURRENT vs LOAD: I_{Q1} (TLV7101828)

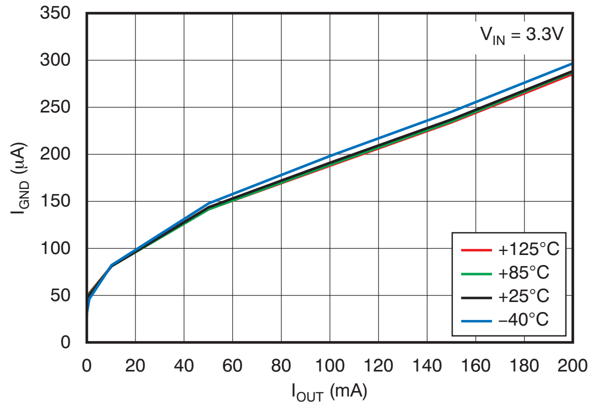


Figure 38.

GROUND PIN CURRENT vs LOAD: I_{Q2} (TLV7103333)

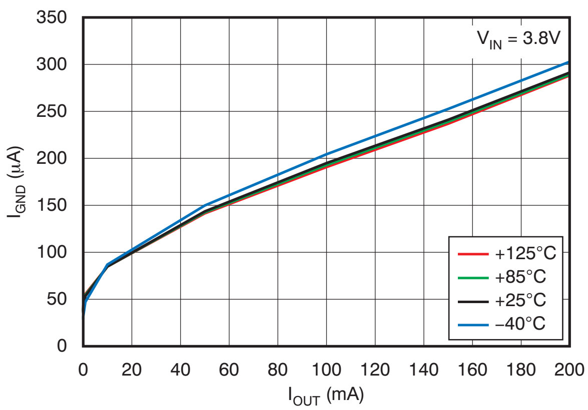


Figure 39.

GROUND PIN CURRENT vs LOAD: I_{Q1} (TLV7111525)

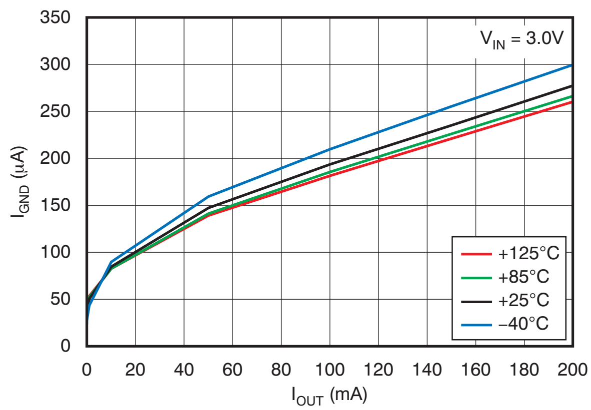


Figure 40.

SHUTDOWN CURRENT vs INPUT VOLTAGE (TLV7101828)

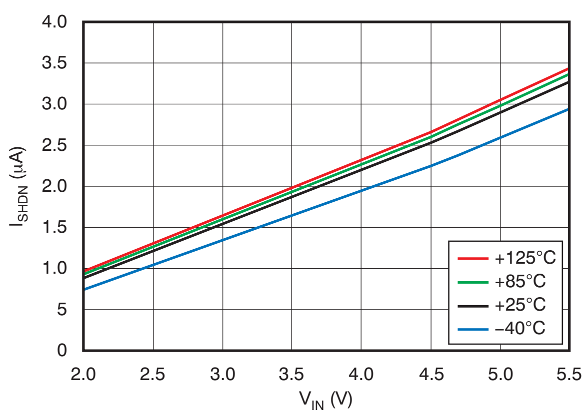


Figure 41.

SHUTDOWN CURRENT vs INPUT VOLTAGE (TLV7103333)

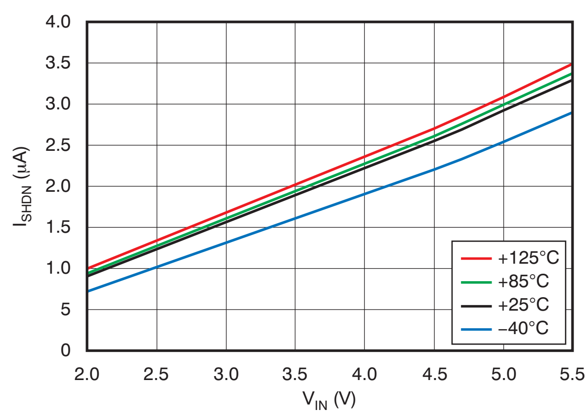


Figure 42.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of T_J = –40°C to +125°C, V_{EN1} = V_{EN2} = V_{IN}, C_{IN} = 1μF, C_{OUT1} = 1μF, and C_{OUT2} = 1μF, unless otherwise noted. Typical values are at T_J = +25°C.

SHUTDOWN CURRENT vs INPUT VOLTAGE (TLV7111525)

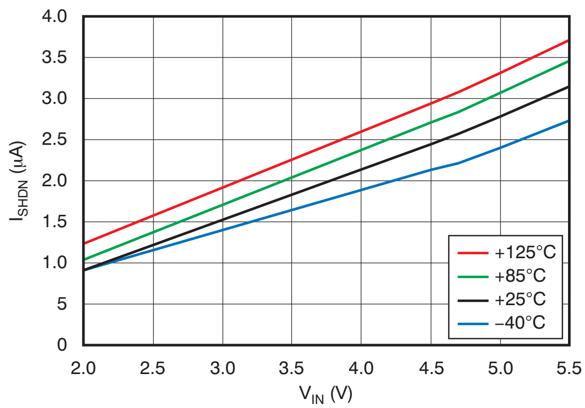


Figure 43.

CURRENT LIMIT vs INPUT VOLTAGE: I_{CL1} (TLV7101828)

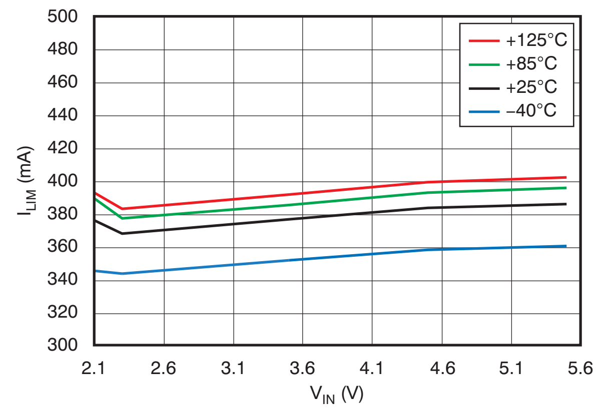


Figure 44.

CURRENT LIMIT vs INPUT VOLTAGE: I_{CL2} (TLV7101828)

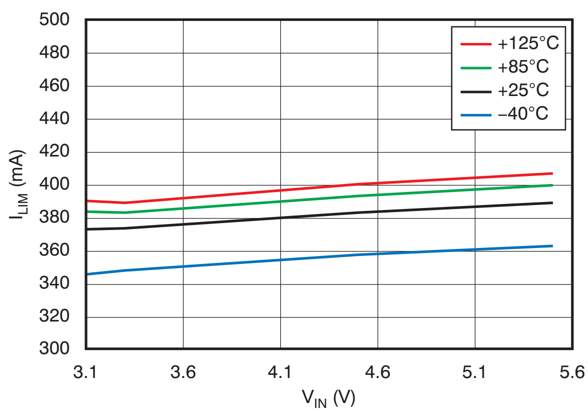


Figure 45.

CURRENT LIMIT vs INPUT VOLTAGE: I_{CL1} (TLV7103333)

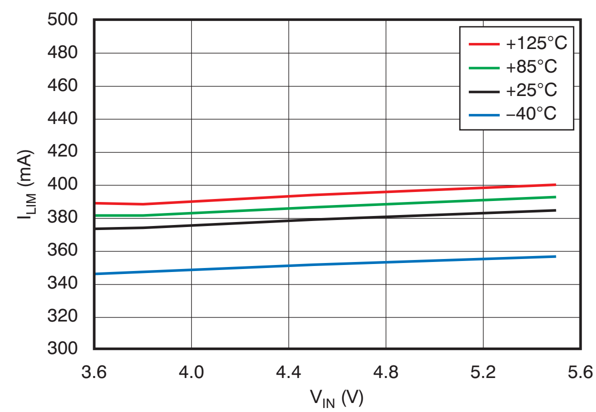


Figure 46.

CURRENT LIMIT vs INPUT VOLTAGE: I_{CL2} (TLV7103333)

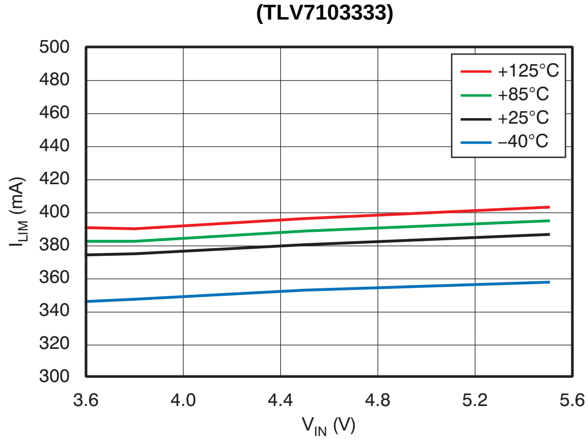


Figure 47.

CURRENT LIMIT vs INPUT VOLTAGE: I_{CL1} (TLV7111525)

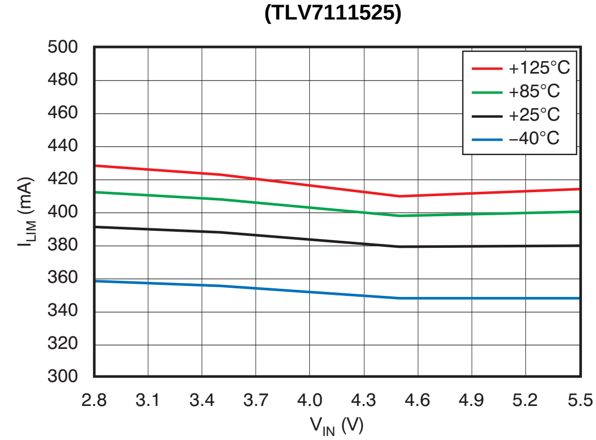


Figure 48.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of T_J = –40°C to +125°C, V_{EN1} = V_{EN2} = V_{IN}, C_{IN} = 1μF, C_{OUT1} = 1μF, and C_{OUT2} = 1μF, unless otherwise noted. Typical values are at T_J = +25°C.

CURRENT LIMIT vs INPUT VOLTAGE: I_{CL2}
(TLV7111525)

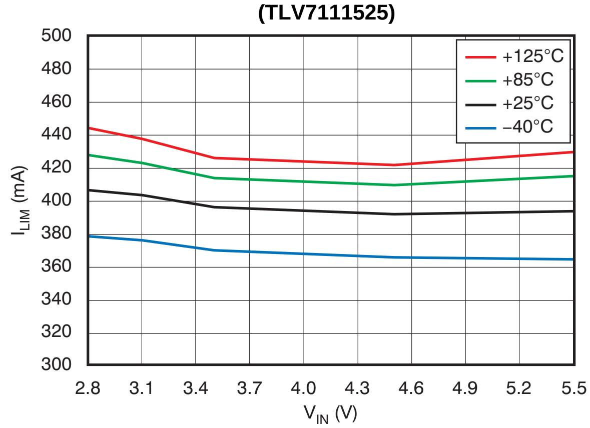


Figure 49.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY
(TLV7101828)

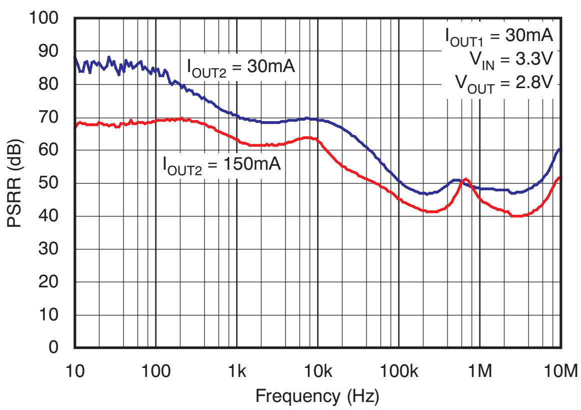


Figure 50.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY
(TLV7103333)

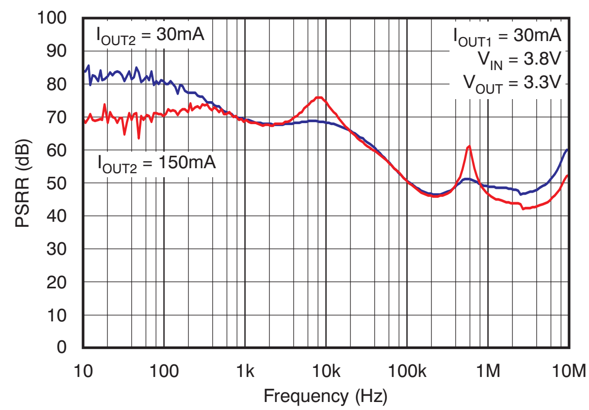


Figure 51.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY
(TLV7111525)

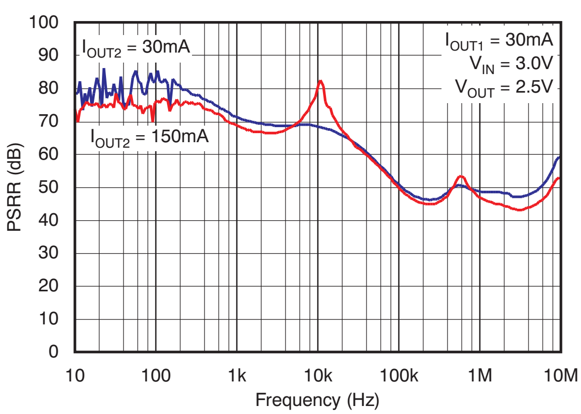


Figure 52.

OUTPUT SPECTRAL NOISE DENSITY
vs FREQUENCY (TLV7101828)

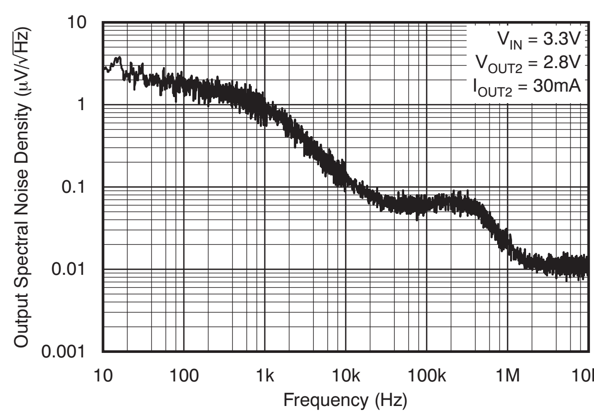


Figure 53.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of T_J = –40°C to +125°C, $V_{EN1} = V_{EN2} = V_{IN}$, C_{IN} = 1µF, C_{OUT1} = 1µF, and C_{OUT2} = 1µF, unless otherwise noted. Typical values are at T_J = +25°C.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY (TLV7103333)

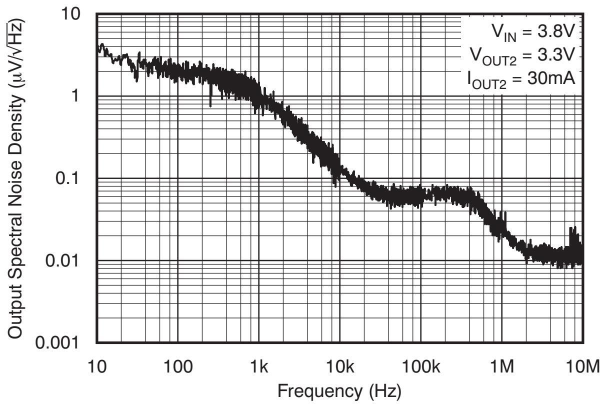


Figure 54.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY (TLV7111525)

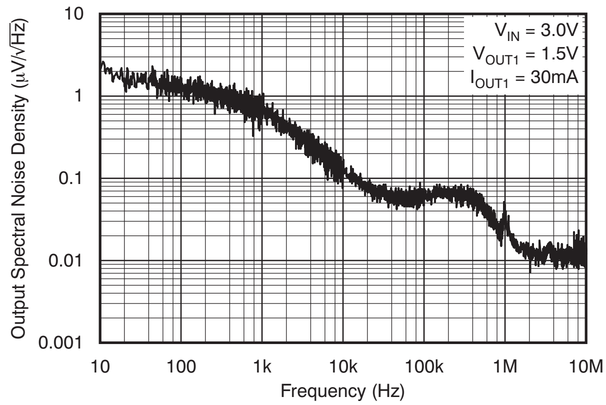


Figure 55.

LINE TRANSIENT RESPONSE V_{OUT1} = 1.2V, V_{OUT2} = 1.2V

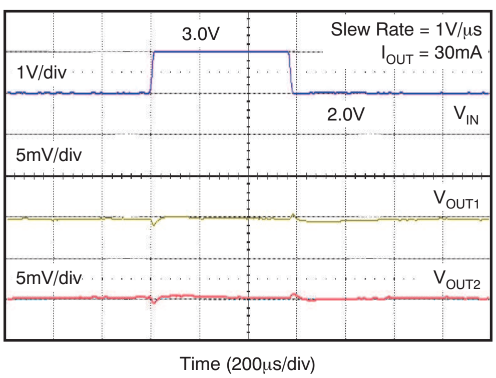


Figure 56.

LINE TRANSIENT RESPONSE V_{OUT1} = 1.2V, V_{OUT2} = 1.2V

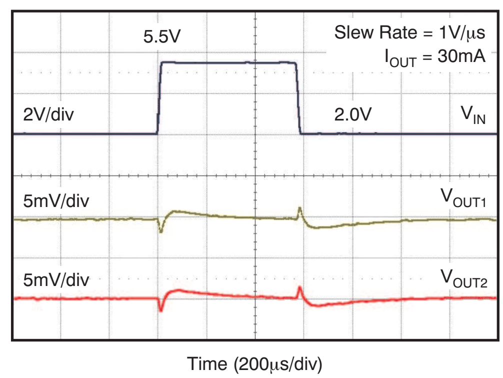


Figure 57.

LINE TRANSIENT RESPONSE V_{OUT1} = 1.8V, V_{OUT2} = 2.8V

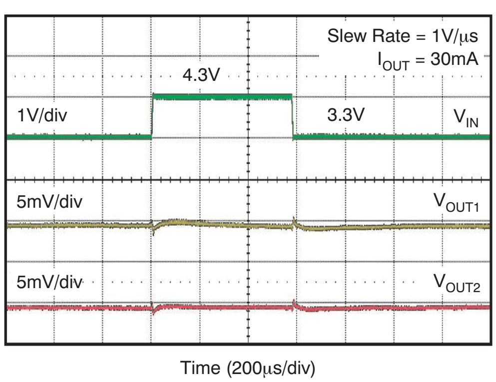


Figure 58.

LINE TRANSIENT RESPONSE V_{OUT1} = 1.8V, V_{OUT2} = 2.8V

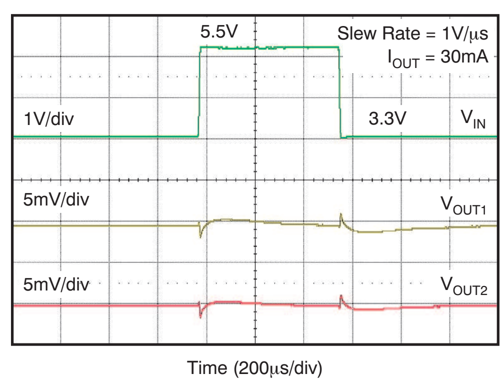
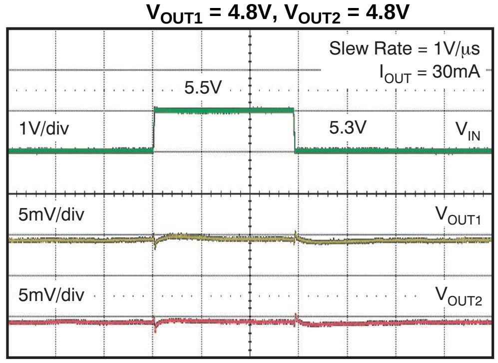


Figure 59.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of T_J = –40°C to +125°C, V_{EN1} = V_{EN2} = V_{IN}, C_{IN} = 1μF, C_{OUT1} = 1μF, and C_{OUT2} = 1μF, unless otherwise noted. Typical values are at T_J = +25°C.

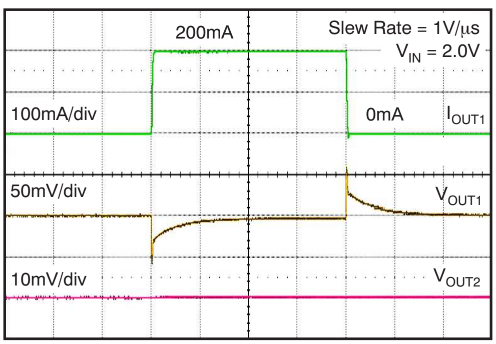
LINE TRANSIENT RESPONSE
V_{OUT1} = 4.8V, V_{OUT2} = 4.8V



Time (200μs/div)

Figure 60.

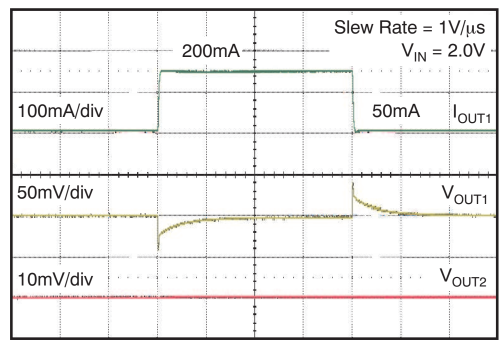
LOAD TRANSIENT RESPONSE AND CROSSTALK
V_{OUT1} = 1.2V, V_{OUT2} = 1.2V



Time (50μs/div)

Figure 61.

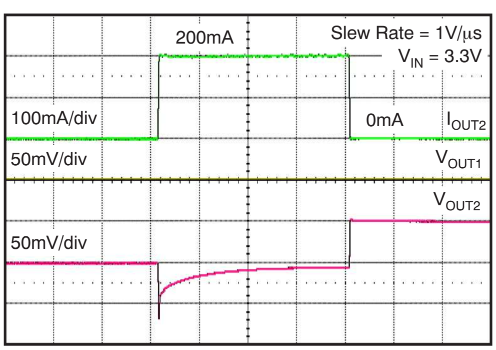
LOAD TRANSIENT RESPONSE AND CROSSTALK
V_{OUT1} = 1.2V, V_{OUT2} = 1.2V



Time (50μs/div)

Figure 62.

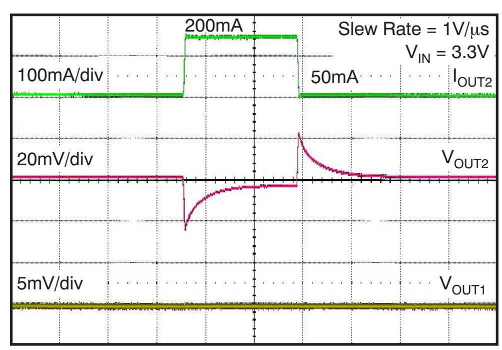
LOAD TRANSIENT RESPONSE AND CROSSTALK
V_{OUT1} = 1.8V, V_{OUT2} = 2.8V



Time (50μs/div)

Figure 63.

LOAD TRANSIENT RESPONSE AND CROSSTALK
V_{OUT1} = 1.8V, V_{OUT2} = 2.8V



Time (50μs/div)

Figure 64.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of T_J = –40°C to +125°C, $V_{EN1} = V_{EN2} = V_{IN}$, C_{IN} = 1μF, C_{OUT1} = 1μF, and C_{OUT2} = 1μF, unless otherwise noted. Typical values are at T_J = +25°C.

LOAD TRANSIENT RESPONSE AND CROSSTALK
V_{OUT1} = 4.8V, V_{OUT2} = 4.8V

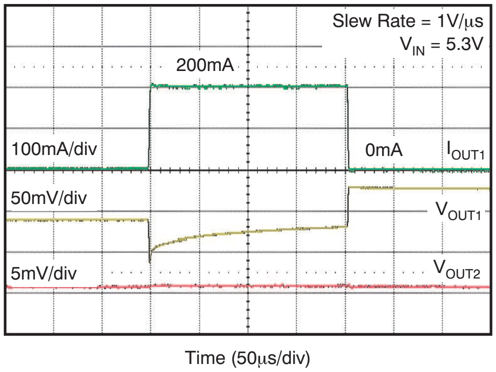


Figure 65.

LOAD TRANSIENT RESPONSE AND CROSSTALK
V_{OUT1} = 4.8V, V_{OUT2} = 4.8V

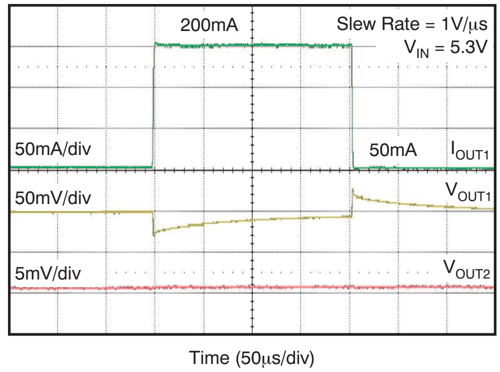


Figure 66.

V_{IN} RAMP UP, RAMP DOWN RESPONSE
V_{OUT1} = 1.2V, V_{OUT2} = 1.2V

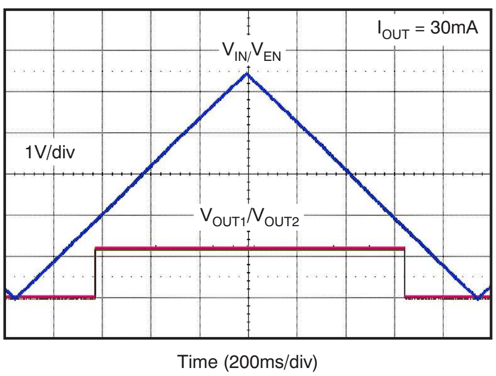


Figure 67.

V_{IN} RAMP UP, RAMP DOWN RESPONSE
V_{OUT1} = 1.8V, V_{OUT2} = 2.8V

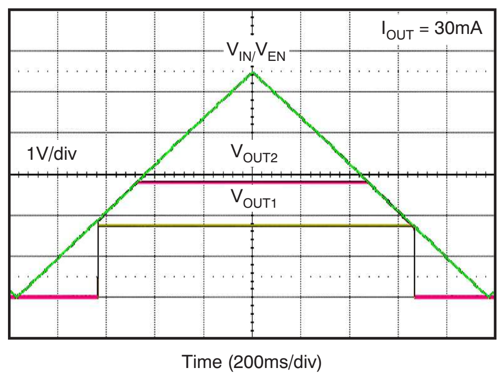


Figure 68.

V_{IN} RAMP UP, RAMP DOWN RESPONSE
V_{OUT1} = 4.8V, V_{OUT2} = 4.8V

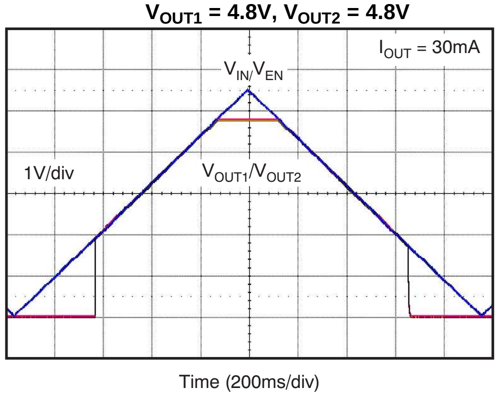


Figure 69.

APPLICATION INFORMATION

The TLV710 and TLV711 series of devices belong to a new family of next generation, value LDO regulators. These devices consume low quiescent current and deliver excellent line and load transient performance. These features, combined with low noise, very good PSRR with little (V_{IN} to V_{OUT}) headroom, make these devices ideal for RF portable applications. This family of LDO regulators offers current limit and thermal protection, and is specified from –40°C to +125°C.

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

1.0μF X5R- and X7R-type ceramic capacitors are recommended because they have minimal variation in value and equivalent series resistance (ESR) over temperature.

However, the TLV710 and TLV711 are designed to be stable with an effective capacitance of 0.1μF or larger at the output. Thus, the device would also be stable with capacitors of other dielectrics, as long as the effective capacitance under operating bias voltage and temperature is greater than 0.1μF. This effective capacitance refers to the capacitance that the device sees under operating bias voltage and temperature conditions (that is, the capacitance after taking bias voltage and temperature derating into consideration.)

In addition to allowing the use of cost-effective dielectrics, these devices also enable using smaller footprint capacitors that have a higher derating in size-constrained applications.

Note that using a 0.1μF rating capacitor at the output of the LDO regulator does not ensure stability because the effective capacitance under operating conditions would be less than 0.1μF. The maximum ESR should be less than 200mΩ.

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1μF to 1.0μF low ESR capacitor across the IN and GND pins of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast-rise-time load transients are anticipated, or if the device is not located near the power source. If source impedance is more than 2Ω, a 0.1μF input capacitor may be necessary to ensure stability.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

Input and output capacitors should be placed as close to the device pins as possible. To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should be connected directly to the GND pin of the device. High ESR capacitors may degrade PSRR.

INTERNAL CURRENT LIMIT

The TLV710 and TLV711 internal current limits help protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. In such a case, the output voltage is not regulated, and is $V_{OUT} = I_{LIMIT} \times R_{LOAD}$.

The PMOS pass transistor dissipates ($V_{IN} - V_{OUT}$) × I_{LIMIT} until thermal shutdown is triggered and the device is turned off. As the device cools down, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown. See the *Thermal Information* section for more details. The PMOS pass element in the TLV710 and TLV711 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of rated output current is recommended.

SHUTDOWN

The enable pin (EN) is active high. The device is enabled when EN pin goes above 0.9V. This relatively lower value of voltage needed to turn the LDO regulator on can be used to enable the device with the GPIO of recent processors whose GPIO voltage is lower than traditional microcontrollers.

The device is turned off when the EN pin is held at less than 0.4V. When shutdown capability is not required, the EN pin can connected to the IN pin.

The TLV711 has internal pull-down circuitry that discharges output with a time constant of:

$$\tau = \frac{120 \cdot R_L}{120 + R_L} \cdot C_{OUT}$$

Where:

R_L = load resistance

C_{OUT} = output capacitor (1)

DROPOUT VOLTAGE

The TLV710 and TLV711 use a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with the output current because the PMOS device behaves as a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout.

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response.

The TLV710 and TLV711 each have a dedicated V_{REF}. Consequently, crosstalk from one channel to the other as a result of transients is close to 0V.

UNDERVOLTAGE LOCKOUT (UVLO)

The TLV710 and TLV711 use an undervoltage lockout circuit to keep the output shut off until the internal circuitry is operating properly.

THERMAL INFORMATION

Thermal protection disables the output when the junction temperature rises to approximately +165°C, allowing the device to cool. When the junction temperature cools to approximately +145°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TLV710 and TLV711 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TLV710/ TLV711 into thermal shutdown degrades device reliability.

POWER DISSIPATION

The ability to remove heat from a die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air.

Performance data for the TLV710 evaluation module (EVM) are shown in Table 1. The EVM is a 2-layer board with 2 ounces of copper per side. The dimension and layout are shown in Figure 70 and Figure 71. Using heavier copper increases the effectiveness of removing heat from the device. The addition of plated through-holes in the heat-dissipating layer also improves the heatsink effectiveness. Power dissipation depends on input voltage and load conditions.

Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element, as shown in Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

PACKAGE MOUNTING

Solder pad footprint recommendations for the TLV710 and TLV711 are available from the Texas Instruments Web site at www.ti.com. The recommended land pattern for the DSE (SON-6) package is shown in Figure 72.

Table 1. TLV710 EVM Dissipation Ratings

PACKAGE	$R_{\theta JA}$	T_A < +25°C	T_A = +70°C	T_A = +85°C
DSE	170°C/W	585mW	320mW	235mW

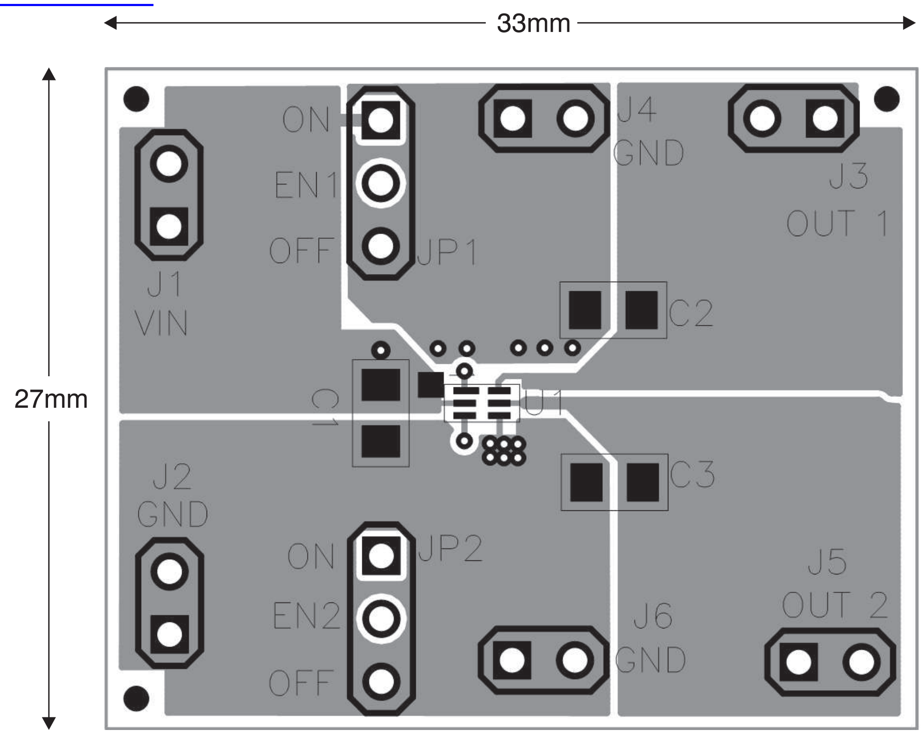


Figure 70. Top Layer

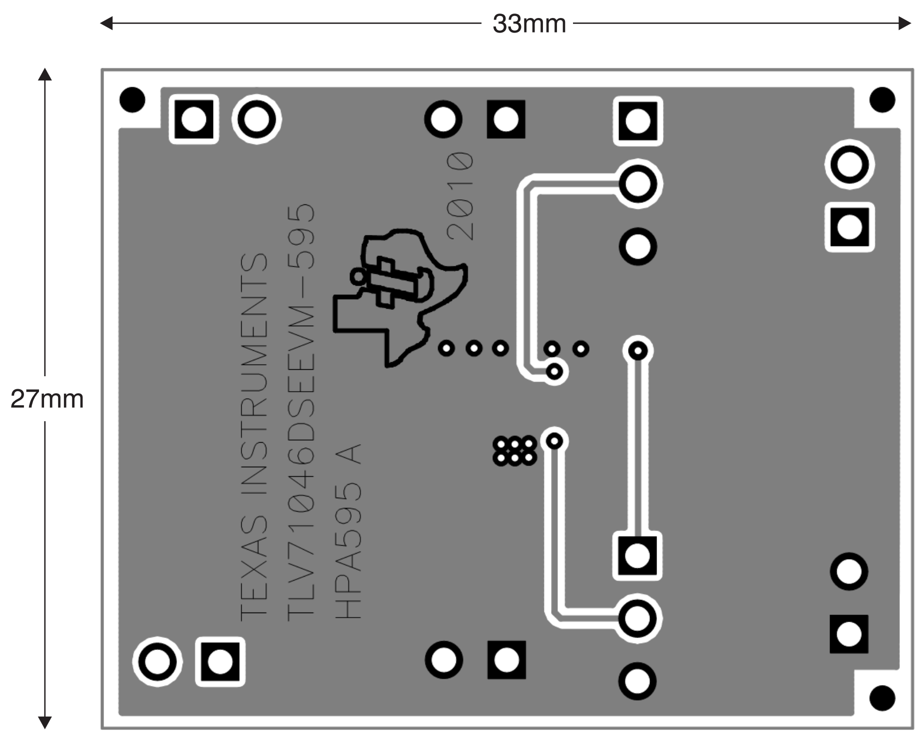
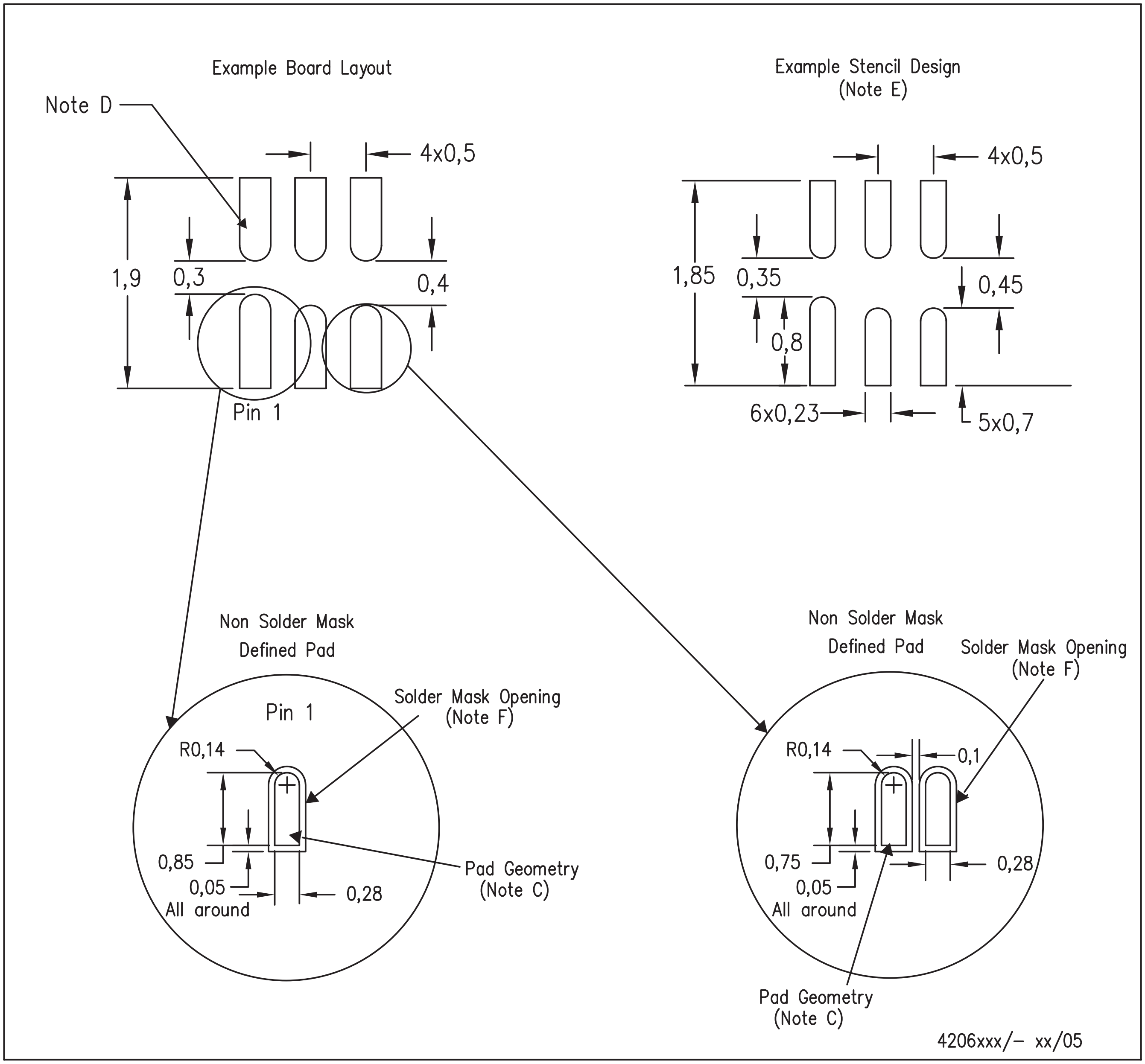


Figure 71. Bottom Layer

DSE (S-PDSO-N6)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is a QFN that does not have a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

Figure 72. Land Pattern Drawing for DSE (SON-6) Package

查询"TLV7101828"供应商

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Pea
TLV7101828DSER	ACTIVE	WSON	DSE	6	3000	TBD	Call TI	Call TI
TLV7101828DSET	ACTIVE	WSON	DSE	6	250	TBD	Call TI	Call TI
TLV7113333DSER	PREVIEW	WSON	DSE	6	3000	TBD	Call TI	Call TI
TLV7113333DSET	PREVIEW	WSON	DSE	6	250	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.t information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable fo
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retard in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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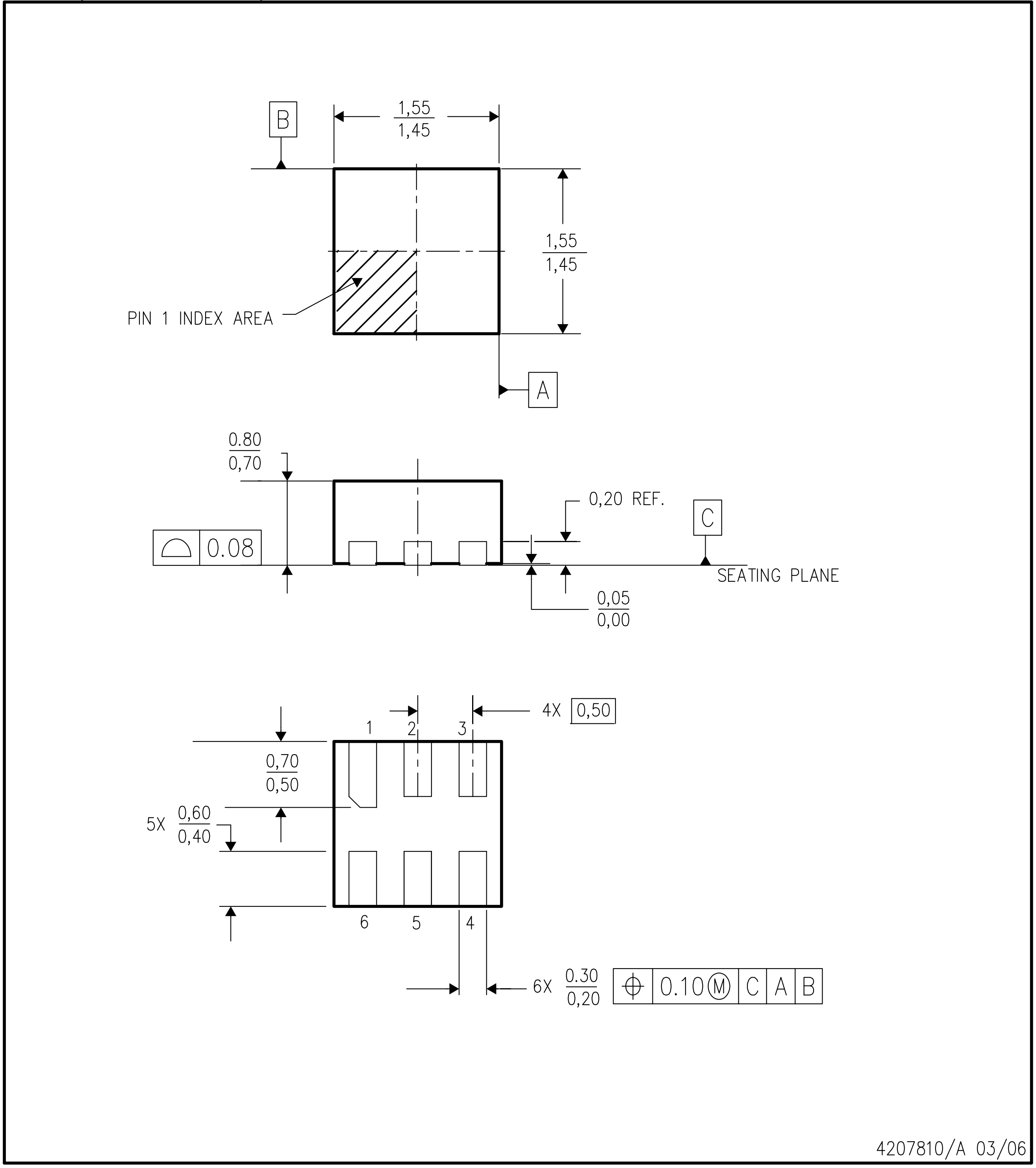
DSE (S-PDSO-N6) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Small Outline No-Lead (SON) package configuration.
- D. This package is lead-free.

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