LC²MOS Complete, 12-Bit, 100 kHz Sampling ADC

AD7876

1.1 Scope.

This specification covers the detail requirement for a monolithic CMOS 12-bit sampling A/D converter. It features a track/hold amplifier, 8 μs successive approximation ADC, 3 V buried Zener reference and an analog input range of ±10 V.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	AD7876TQ/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

Package	Description
Q-24	24-Pin Cerdip

1.3 Absolute Maximum Ratings.

V_{DD} to AGND . . . . . −0.3 V dc to +7 V dc
V_{SS} to AGND . . . . . +0.3 V dc to −7.0 V dc
AGND to DGND . . . . . −0.3 V dc to V_{DD} + 0.3 V dc
V_{IN} to AGND . . . . . −15 V dc to +15 V dc
REF OUT to AGND . . . . . 0 V dc to V_{DD}
Digital Inputs to DGND . . . . . −0.3 V dc to V_{DD} + 0.3 V dc
Digital Outputs to DGND . . . . . −0.3 V dc to V_{DD} + 0.3 V dc
Power Dissipation (T_A = +75°C), P_D . . . . . 450 mW
Lead Temperature (Soldering 10 sec) . . . . . +300°C
Storage Temperature Range . . . . . −65°C to +150°C
Thermal Resistance, Junction-to-Case . . . . . See MIL-M-38510, Appendix C

1.4 Recommended Operating Conditions.

Supply Voltage
V_{DD} . . . . . +4.75 V dc to +5.25 V dc
V_{SS} . . . . . −4.75 V dc to −5.25 V dc
AGND . . . . . 0 V dc
DGND . . . . . 0 V dc
External Clock Frequency, f_{CLK} . . . . . 2.5 MHz
Ambient Operating Temperature Range . . . . . −55°C to +125°C

AD7876—SPECIFICATIONS

Table 1.

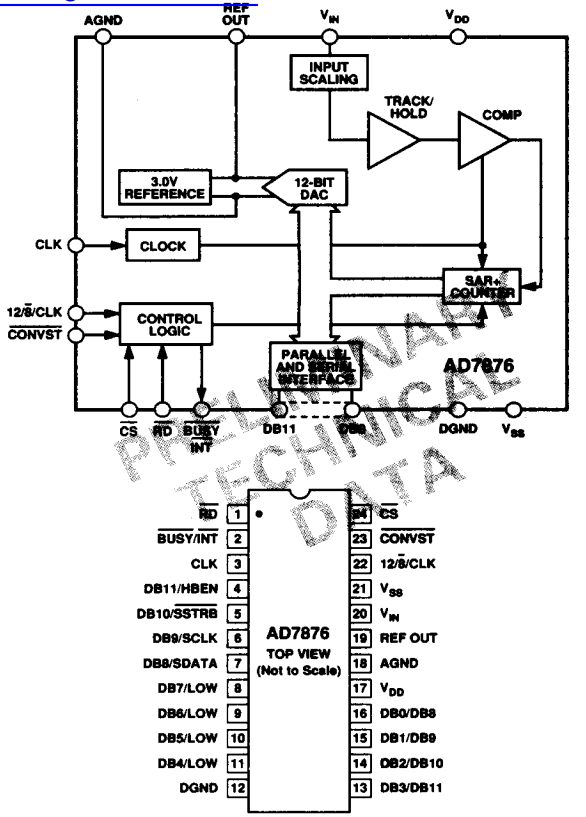
Test	Symbol	Device	Limits Min	Limits Max	Sub Groups	Test Condition[1] (−55°C ≤ T_A ≤ +125°C unless otherwise noted)	Unit
Resolution	RES	All	12		1, 2, 3	Guaranteed Minimum Resolution	Bits
Integral Nonlinearity	INL	All		±1	1, 2, 3		LSB
Differential Nonlinearity	DNL	All		+1	1, 2, 3		LSB
Bipolar Zero Error	BZ_E	All		±6	1, 2, 3		LSB
Full-Scale Error[2]	F_{SE}	All		±8	1		LSB
Full-Scale Error Temperature Coefficient[2]	ΔFSE/ΔT	All		±60	1, 2, 3		ppm/°C
Track/Hold Acquisition Time	t_{ACQ}	All		2	9, 10, 11		μs
Analog Input Voltage Range	V_{IN}	All		±10	1, 2, 3		V
Analog Input Current	I_{IN}	All		±600	1, 2, 3		μA
REF OUT Voltage	V_{REF}	All	2.99	3.01	1		V
REF OUT Voltage Temperature Coefficient	$\Delta/V_{REF}\Delta T$	All		±60	1, 2, 3		ppm/°C
Reference Load Sensitivity	$\Delta/V_{REF}\Delta I$	All		−1.0	1, 2, 3	Reference Load Current Change = 0 μA to 500 μA[3]	mV
Logic Input High Voltage	V_{INH}	All	2.4		1, 2, 3		V
Logic Input Low Voltage	V_{INL}	All		0.8	1, 2, 3		V
Input Current	I_{IN}	All		±10	1, 2, 3	V_{IN} = 0 V to V_{DD}	μA
		All		±10	1, 2, 3	12/$\overline{8}$/CLK Input Only, V_{IN} = V_{SS} to V_{DD}	μA
Input Capacitance[3]	C_{IN}	All		10	1, 2, 3		pF
Output Logic High Voltage	V_{OH}	All	4.0		1, 2, 3	I_{SOURCE} = 40 μA	V
Output Logic Low Voltage	V_{OL}	All		0.4	1, 2, 3	I_{SINK} = 1.6 mA	V
DB11–DB0 Floating State Leakage Current	I_L	All		10	1, 2, 3		μA
DB11–DB0 Floating State Output Capacitance[3]	C_{OUT}	All		15	4		pF
External Clock Conversion Time	t_{CONV} (Ext)	All		8.0	9, 10, 11	f_{CLK} = 2.5 MHz	μs
Internal Clock Conversion Time	t_{CONV} (Int)	All	7	9	9, 10, 11		μs
Supply Current	I_{DD}	All		13	1, 2, 3		mA
	I_{SS}	All		6	1, 2, 3		mA
$\overline{CONVST}$ Pulse Width[4]	t_1	All	50		9	Input tr, tf = 5.0 ns (10% to 90% of +5.0 V), Timing Voltage Reference Level = 1.6 V, See Figure 1	ns
$\overline{CS}$ to $\overline{RD}$ Setup Time[4] (Mode 1)	t_2	All	0				ns
$\overline{RD}$ Pulse Width	t_3	All	75		9, 10, 11		ns
$\overline{CS}$ to $\overline{RD}$ Hold Time[4] (Mode 1)	t_4	All	0		9		ns
$\overline{RD}$ to $\overline{INT}$ Delay Time[4]	t_5	All		70	9		ns
Data Access Time After $\overline{RD}$[5]	t_6	All		70	9, 10, 11		ns
Bus Relinquish Time After $\overline{RD}$[6]	t_7	All	5.0	50	9, 10, 11		ns
HBEN to $\overline{RD}$ Setup Time[4]	t_8	All	0		9		ns
HBEN to $\overline{RD}$ Hold Time[4]	t_9	All	0		9		ns

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Test	Symbol	Device	Limits Min	Limits Max	Sub Groups	Test Condition[1] ($-55°C \le T_A \le +125°C$ unless otherwise noted)	Unit
$\overline{SSTRB}$ to SCLK Falling Edge Setup Time	t_{10}	All	100		9	Input tr, tf = 5.0 ns (10% to 90% of +5.0 V), Timing Voltage Reference Level = 1.6 V, See Figure 1	ns
SCLK Cycle Time[4, 7]	t_{11}	All	370		9		ns
SCLK to Valid Data Delay Time[4, 8]	t_{12}	All		150	9		ns
SCLK Rising Edge to $\overline{SSTRB}$[4]	t_{13}	All	20	100	9		ns
Bus Relinquish Time After SCLK[4]	t_{14}	All	10	100	9		ns
$\overline{CS}$ to $\overline{RD}$ Setup Time (Mode 2)[4]	t_{15}	All	60		9		ns
Propagation Delay Time, $\overline{CS}$ to $\overline{BUSY}$[4]	t_{16}	All		120	9		ns
Data Setup Time Prior to $\overline{BUSY}$[4]	t_{17}	All	200		9		ns
$\overline{CS}$ to $\overline{RD}$ Hold Time (Mode 2)[4]	t_{18}	All			9		ns
HBEN to $\overline{CS}$ Setup Time[4]	t_{19}	All	0		9		ns
HBEN to $\overline{CS}$ Hold Time[4]	t_{20}	All	0		9		ns

NOTES
[1]V_{DD} = +4.75 V to +5.25 V; V_{SS} = −4.75 V or −5.25 V, AGND = DGND = 0 V; f_{CLK} = +2.5 MHz external, unless otherwise specified.
[2]Includes internal reference error and is calculated after bipolar zero error has been adjusted out.
[3]Reference load should not be changed during conversion.
[4]Sample tested at +25°C to ensure compliance.
[5]t_6 is defined as the time required for an output to cross 0.8 V or 2.4 V.
[6]t_7 is defined as the time required for the data lines to change 0.5 V.
[7]SCLK mark/space ratio (measured from a voltage level of 1.6 V) is 40/60 to 60/40.
[8]SDATA will drive higher capacitive loads but this will add to t^{12} since it increases the external RC time constant (4.7 kΩ||C_L) and hence the time to reach 2.4 V, C_L = 35 pF.

3.2.1 Functional Block Diagram and Terminal Assignments.

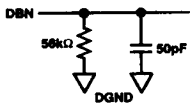


3.2.4 Microcircuit Technology Group.

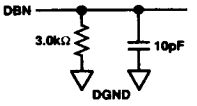
This microcircuit is covered by technology group (81).

4.2.1 Life Test/Burn-In Circuit.

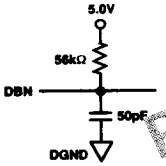
Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



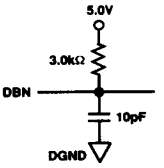
a. Load Circuit for Access Time, High-Z to V_{OH}



c. Load Circuit for OutputFloat Delay, V_{OH} to High-Z



b. Load Circuit for Access Time, High-Z to V_{OL}



d. Load Circuit for Output Float Delay, V_{OL} to High-Z

Figure 1. Output Load Circuits and Waveforms