

2SK3582TK

For ECM

- Application for Ultra-compact ECM

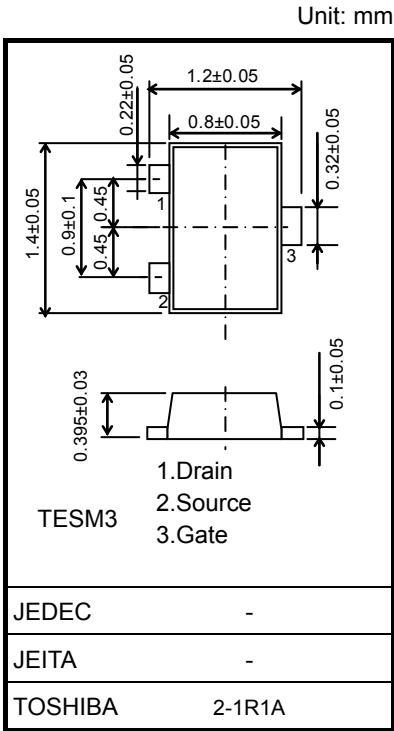
Absolute Maximum Ratings (Ta=25°C)

Characteristic	Symbol	Rating	Unit
Gate-Drain voltage	V <sub>GDO</sub>	-20	V
Gate Current	I <sub>G</sub>	10	mA
Drain power dissipation (Ta = 25°C)	P <sub>D</sub>	100	mW
Junction Temperature	T <sub>j</sub>	125	°C
Storage temperature range	T <sub>stg</sub>	-55~125	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.  
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

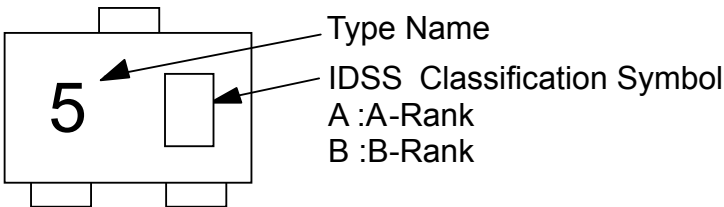
IDSS CLASSIFICATION

A-Rank      80 to 200 μA  
B-Rank      170 to 300μA

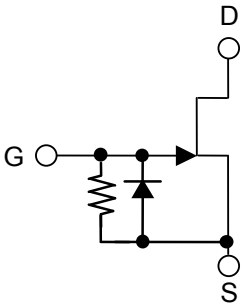


Weight: 2.2mg (typ.)

Marking



Equivalent Circuit

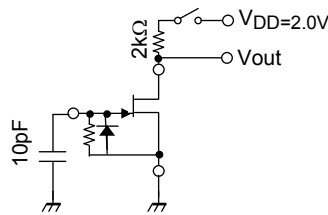


**Electrical Characteristics (Ta=25°C)**

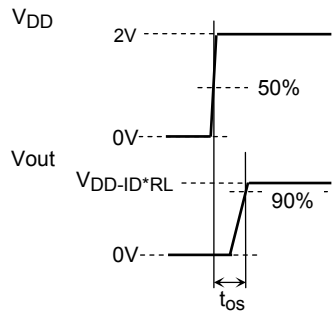
Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Drain Current	$I_{DSS}$	$V_{DS} = 2\text{ V}, V_{GS} = 0$	80	—	300	$\mu\text{A}$
Drain Current	$I_D$	$V_{DD} = 2\text{ V}, R_L = 2\text{ k}\Omega, C_g = 10\text{ pF}$	—	—	340	$\mu\text{A}$
Gate-Source Cut-off Voltage	$V_{GS(OFF)}$	$V_{DS} = 2\text{ V}, I_D = 1\mu\text{A}$	-0.1	—	-0.65	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = 2\text{ V}, V_{GS} = 0\text{ V}$	0.55	1.0	—	mS
Gate-Drain Voltage	$V_{(BR)GDO}$	$I_G = -10\mu\text{A}$	-20	—	—	V
Input capacitance	$C_{iss}$	$V_{DS} = 2\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	3.6	—	pF
Voltage Gain	$G_v$	$V_{DD} = 2\text{ V}, R_L = 2\text{ k}\Omega, C_g = 10\text{ pF}, f = 1\text{ kHz}, v_{in} = 100\text{ mV}$	-5.0	0	+2.0	dB
Delta Voltage Gain	$DG_v(f)$	$V_{DD} = 2\text{ V}, R_L = 2\text{ k}\Omega, C_g = 10\text{ pF}, f = 1\text{ kHz to } 100\text{ Hz}, v_{in} = 100\text{ mV}$	—	0	-1.0	dB
Delta Voltage Gain	$DG_v(V)$	$V_{DD} = 2\text{ V to } 1.5\text{ V}, R_L = 2\text{ k}\Omega, C_g = 10\text{ pF}, f = 1\text{ kHz}, v_{in} = 100\text{ mV}$	—	-1.0	-3.0	dB
Noise Voltage	$V_N$	$V_{DD} = 2\text{ V}, R_L = 1\text{ k}\Omega, C_g = 10\text{ pF}, G_v = 80\text{ dB}, \text{A-Curve Filter}$	—	—	50	mV
Total Harmonic Distortion	THD	$V_{DD} = 2\text{ V}, R_L = 2\text{ k}\Omega, C_g = 10\text{ pF}, f = 1\text{ kHz}, v_{in} = 50\text{ mV}$	—	1.0	—	%
Time Output Stability	$t_{os}$	$V_{DD} = 2\text{ V}, R_L = 2\text{ k}\Omega, C_g = 10\text{ pF}$	—	100	200	ms

**Time Output Stability Test Method**

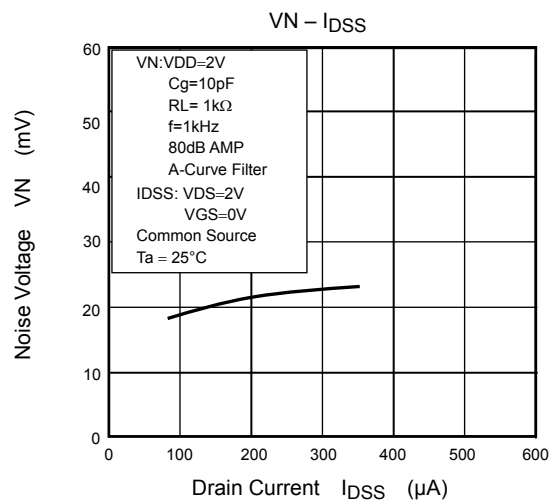
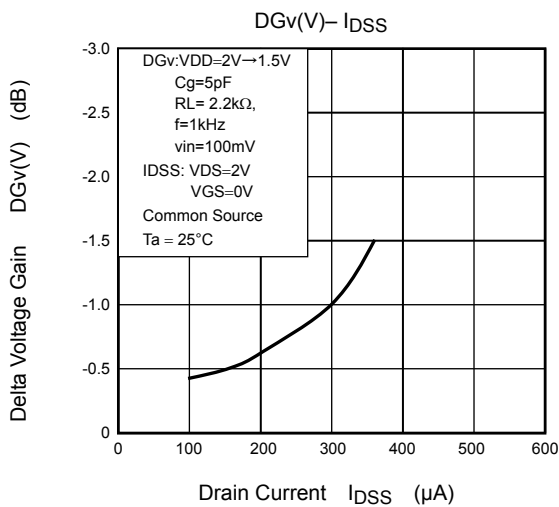
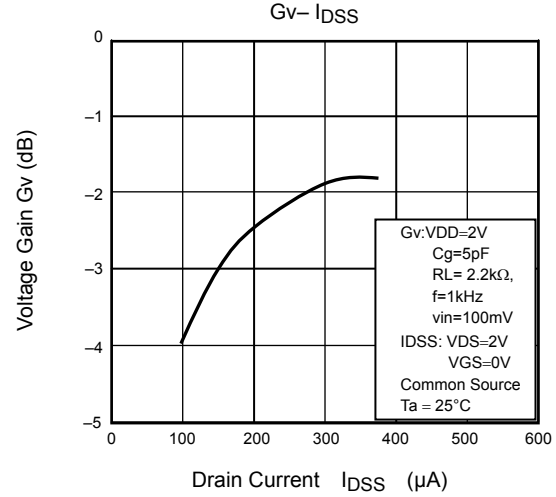
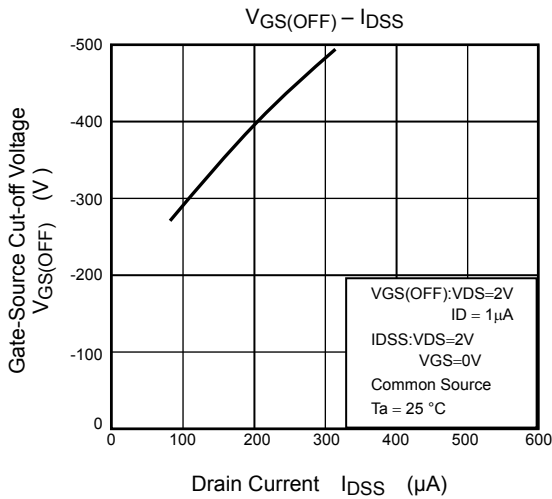
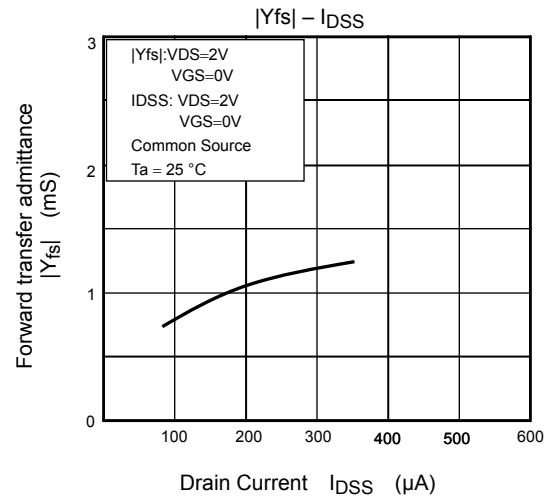
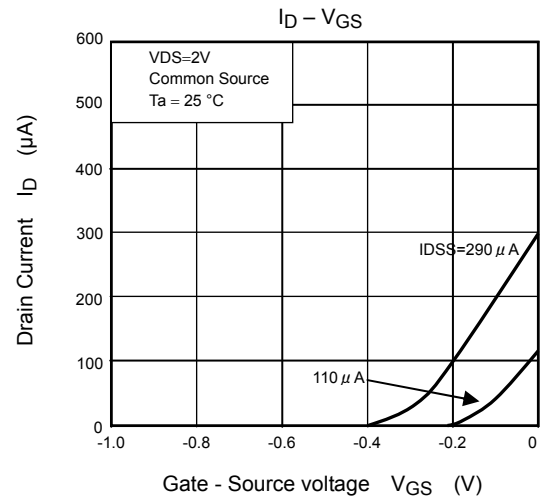
a) TEST CIRCUIT



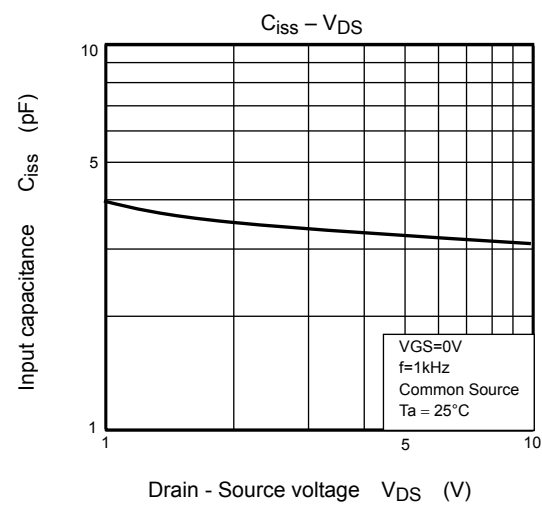
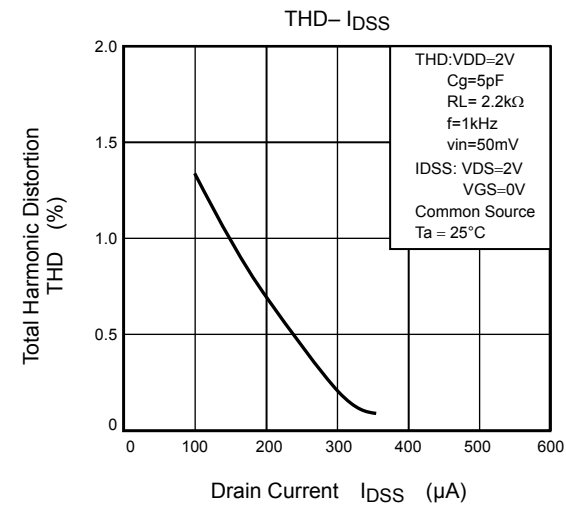
b) TEST SIGNAL



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