L6388E

High-voltage high and low side driver

Features

- High voltage rail up to 600V
- dV/dt immunity ±50V/nsec in full temperature range
- Driver current capability:
  - 400mA source,
  - 650mA sink
- Switching times 70/40 nsec rise/fall with 1nF load
- 3.3V, 5V, 15V CMOS/TTL inputs comparators with hysteresys and pull down
- Internal bootstrap diode
- Outputs in phase with inputs
- Dead time and interlocking function

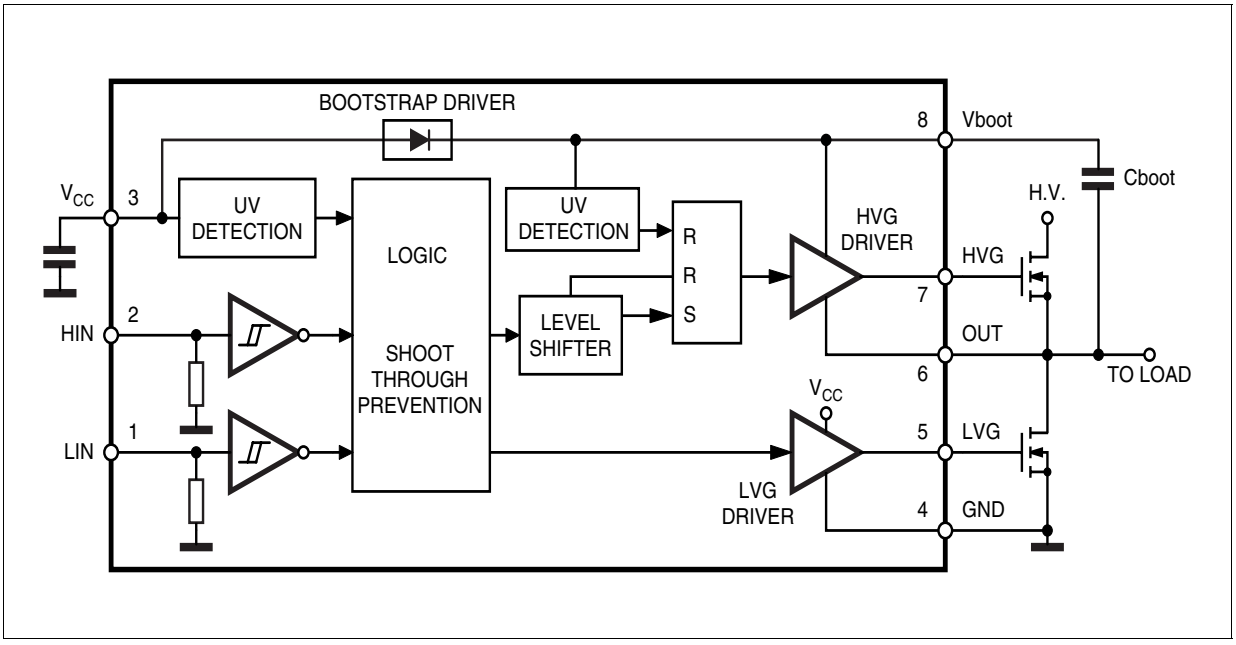
Description

The L6388E is an high-voltage device, manufactured with the BCD"OFF-LINE" technology.

It has a Driver structure that enables to drive independent referenced N Channel Power MOS or IGBT. The High Side(Floating) Section is enabled to work with voltage Rail up to 600V.

The Logic Inputs are CMOS/TTL compatible for ease of interfacing with controlling devices.

Figure 1. Block diagram



Contents

1 Electrical data

1.1 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{out}	Output voltage	-3 to V_{boot} -18	V
V_{cc}	Supply voltage	- 0.3 to +18	V
V_{boot}	Floating supply voltage	-1 to 618	V
V_{hvg}	High side gate output voltage	-1 to V_{boot}	V
V_{lvg}	Low side gate output voltage	-0.3 to V_{cc} +0.3	V
V_i	Logic input voltage	-0.3 to V_{cc} +0.3	V
dV_{out}/d_t	Allowed output slew rate	50	V/ns
P_{tot}	Total power dissipation (T_J = 85 °C)	750	mW
T_j	Junction temperature	150	°C
T_s	Storage temperature	-50 to 150	°C

Note: ESD immunity for pins 6, 7 and 8 is guaranteed up to 900 V (Human Body Model)

1.2 Thermal data

Table 2. Thermal data

Symbol	Parameter	SO-8	DIP-8	Unit
$R_{th(JA)}$	Thermal Resistance Junction to ambient	150	100	°C/W

1.3 Recommended operating conditions

Table 3. Recommended operating conditions

Symbol	Pin	Parameter	Test condition	Min	Typ	Max	Unit
V_{out}	6	Output voltage		(1)		580	V
V_{BS} (2)	8	Floating supply voltage		(1)		17	V
f_{sw}		Switching frequency	HVG,LVG load C_L = 1nF			400	kHz
V_{cc}	3	Supply voltage				17	V
T_J		Junction temperature		-45		125	°C

1. If the condition Vboot - Vout < 18V is guaranteed, Vout can range from -3 to 580V
2. $V_{BS} = V_{boot} - V_{out}$

2 Pin connection

Figure 2. Pin connection (Top view)

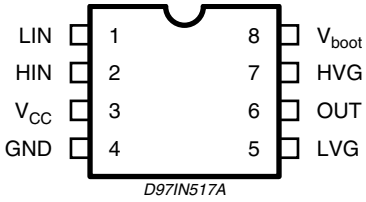


Table 4. Pin description

N°	Pin	Type	Function
1	LIN	I	Low side driver logic input
2	HIN	I	High side driver logic input
3	V_{cc}		Low voltage power supply
4	GND		Ground
5	LVG (1)	O	Low side driver output
6	VOUT	O	High side driver floating reference
7	HVG (1)	O	High side driver output
8	V_{boot}		Bootstrap supply voltage

1. The circuit guarantees 0.3V maximum on the pin (@ Isink = 10mA). This allows to omit the "bleeder" resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low.

3 Electrical characteristics

3.1 AC operation

Table 5. AC operation electrical characteristcs (V_{CC} = 15V; T_J = 25°C)

Symbol	Pin	Parameter	Test condition	Min	Typ	Max	Unit
t_{on}	1 vs 5 2 vs 7	High/low side driver turn-on propagation delay	V_{out} = 0V		225	300	ns
t_{off}		High/low side driver turn-off propagation delay	V_{out} = 0V		160	220	ns
t_r	5, 7	Rise time	C_L = 1000pF		70	100	ns
t_f	5, 7	Fall time	C_L = 1000pF		40	80	ns
DT	5, 7	Dead time		220	320	420	ns

3.2 DC operation

Table 6. DC operation electrical characteristcs (V_{CC} = 15V; T_J = 25°C)

Symbol	Pin	Parameter	Test condition	Min	Typ	Max	Unit
Low supply voltage section							
V_{ccth1}	3	V_{cc} UV turn on threshold		9.1	9.6	10.1	V
V_{ccth2}		V_{cc} UV turn off threshold		7.9	8.3	8.8	V
V_{cchys}		V_{cc} UV hysteresis		0.9			V
I_{qccu}		Undervoltage quiescent supply current	$V_{cc} \leq$ 9V		250	330	µA
I_{qcc}		Quiescent current	V_{cc} = 15V		350	450	µA
R_{dson}		Bootstrap driver on resistance (1)	$V_{cc} \geq$ 12.5V		125		Ω
Bootstrapped supply voltage section							
V_{BSth1}	8	V_{BS} UV turn on threshold		8.5	9.5	10.5	V
V_{BSth2}		V_{BS} UV turn off threshold		7.2	8.2	9.2	V
V_{BShys}		V_{BS} UV hysteresis		0.9			V
I_{QBS}		V_{BS} quiescent current	HVG ON			250	µA
I_{LK}		High voltage leakage current	V_{hvg} = V_{out} = V_{boot} = 600V			10	µA

Table 6. DC operation electrical characteristcs (continued)(V_{CC} = 15V; T_J = 25°C)

Symbol	Pin	Parameter	Test condition	Min	Typ	Max	Unit
High/low side driver							
I_{so}	5,7	Source short circuit current	$V_{IN} = V_{ih}$ (tp < 10µs)	300	400		mA
I_{si}		Sink short circuit current	$V_{IN} = V_{il}$ (tp < 10µs)	500	650		mA
Logic inputs							
V_{il}	1, 2	Low level logic input voltage				1.1	V
V_{ih}		High level logic input voltage		1.8			V
I_{ih}		High level logic input current	V_{IN} = 15V		20	70	µA
I_{il}		Low level logic input current	V_{IN} = 0V	-1			µA

1. $R_{DS(on)}$ is tested in the following way:

$$R_{DSON} = \frac{(V_{CC} - V_{CBOOT1}) - (V_{CC} - V_{CBOOT2})}{I_1(V_{CC}, V_{CBOOT1}) - I_2(V_{CC}, V_{CBOOT2})}$$

where I_1 is pin 8 current when $V_{CBOOT} = V_{CBOOT1}$, I_2 when $V_{CBOOT} = V_{CBOOT2}$

4 Waveforms definitions

Figure 3. Dead time waveforms definitions

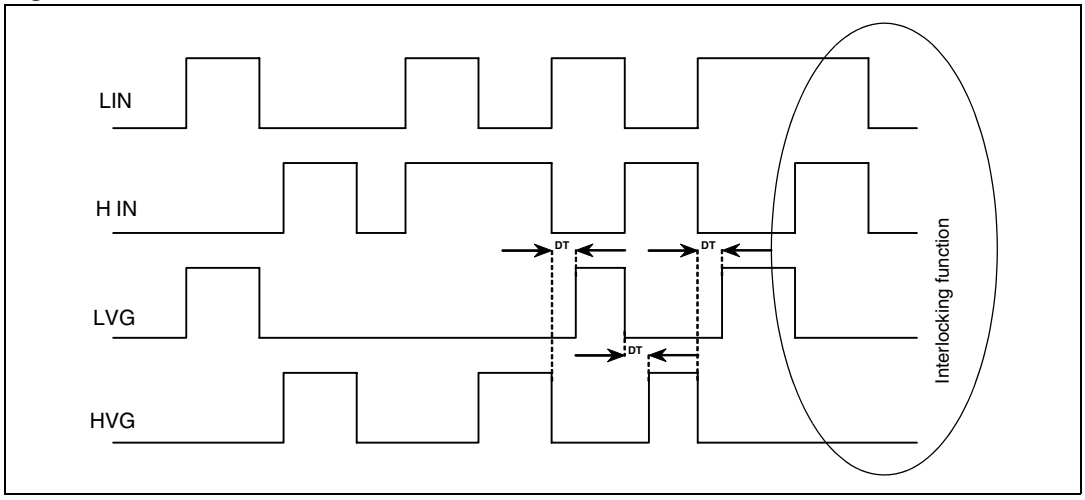
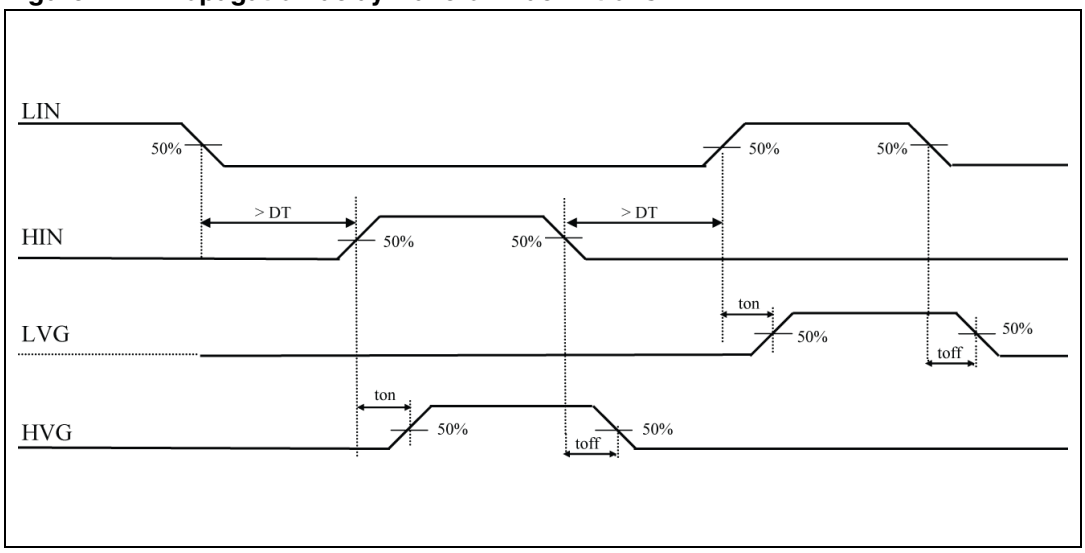


Figure 4. Propagation delay waveform definitions



5 Input logic

Input logic is provided with an interlocking circuitry which avoids the two outputs (LVG, HVG) to be active at the same time when both the logic input pins (LIN, HIN) are at a high logic level. In addition, to prevent cross conduction of the external MOSFETs, after each output is turned-off the other output cannot be turned-on before a certain amount of time (DT) (see *Figure 3*).

6 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode (*Figure 5* a). In the L6388E a patented integrated structure replaces the external diode. It is realized by a high voltage DMOS, driven synchronously with the low side driver (LVG), with in series a diode, as shown in *Figure 5* b. An internal charge pump (*Figure 5* b) provides the DMOS driving voltage. The diode connected in series to the DMOS has been added to avoid undesirable turn on of it.

6.1 C_{BOOT} selection and charging

To choose the proper C_{BOOT} value the external MOS can be seen as an equivalent capacitor. This capacitor C_{EXT} is related to the MOS total gate charge:

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors C_{EXT} and C_{BOOT} is proportional to the cyclical voltage loss. It has to be:

$$C_{BOOT} >>> C_{EXT}$$

e.g.: if Q_{gate} is 30nC and V_{gate} is 10V, C_{EXT} is 3nF. With C_{BOOT} = 100nF the drop would be 300mV.

If HVG has to be supplied for a long time, the C_{BOOT} selection has to take into account also the leakage losses.

e.g.: HVG steady state consumption is lower than 200µA, so if HVG T_{ON} is 5ms, C_{BOOT} has to supply 1µC to C_{EXT}. This charge on a 1µF capacitor means a voltage drop of 1V.

The internal bootstrap driver gives great advantages: the external fast recovery diode can be avoided (it usually has great leakage current).

This structure can work only if V_{OUT} is close to GND (or lower) and in the meanwhile the LVG is on. The charging time (T_{charge}) of the C_{BOOT} is the time in which both conditions are fulfilled and it has to be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS R_{DSON} (typical value: 125 Ω). At low frequency this drop can be neglected. Anyway increasing the frequency it must be taken in to account.

The following equation is useful to compute the drop on the bootstrap DMOS:

$$V_{drop} = I_{charge}R_{dson} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}}R_{dson}$$

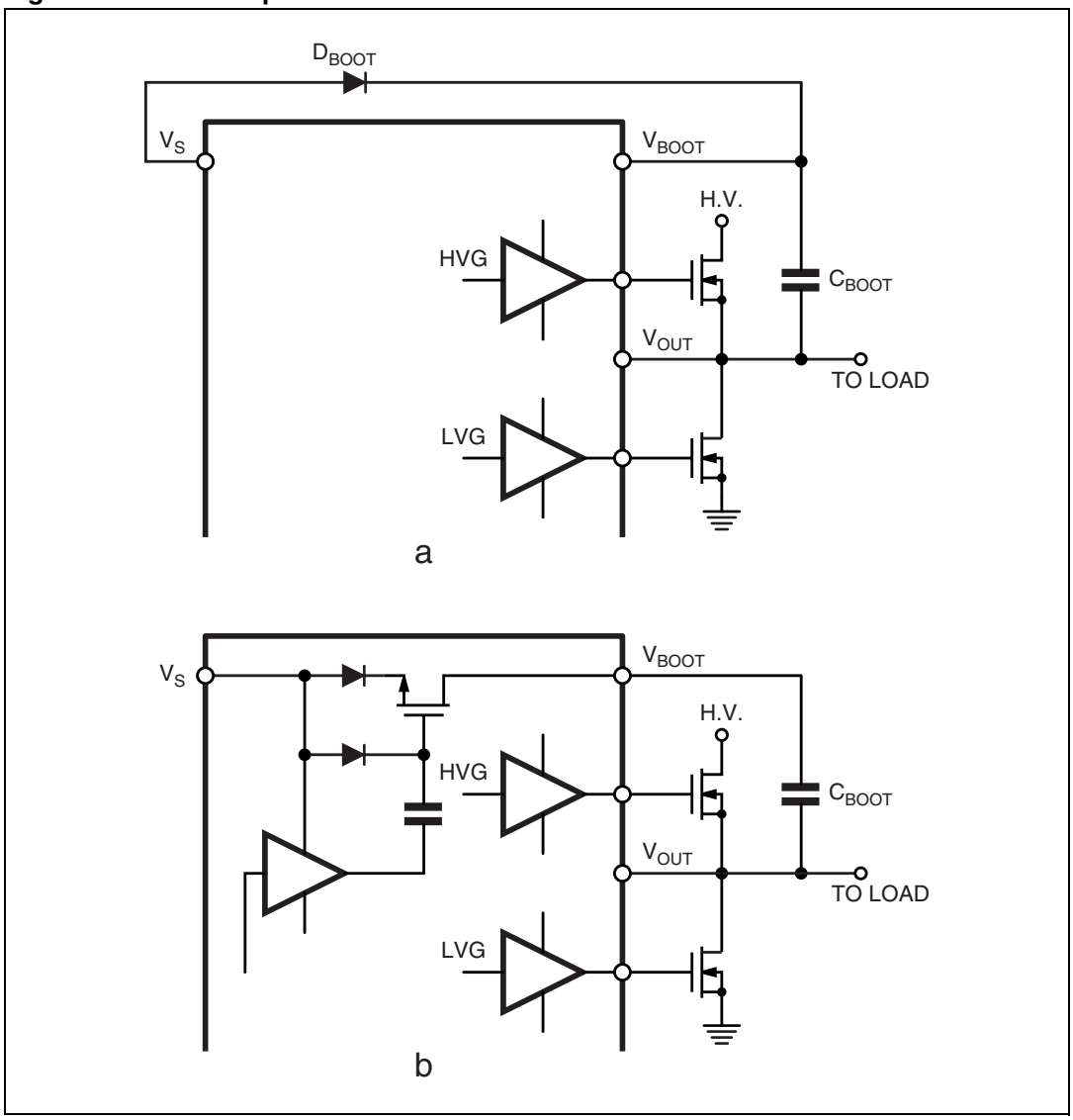
where Q_{gate} is the gate charge of the external power MOS, R_{dson} is the on resistance of the bootstrap DMOS, and T_{charge} is the charging time of the bootstrap capacitor.

For example: using a power MOS with a total gate charge of 30nC the drop on the bootstrap DMOS is about 1V, if the T_{charge} is 5µs. In fact:

$$V_{drop} = \frac{30nC}{5\mu s} \cdot 125\Omega \sim 0.8V$$

V_{drop} has to be taken into account when the voltage drop on C_{BOOT} is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

Figure 5. Bootstrap driver



7 Typical characteristic

Figure 6. Typical rise and fall times vs load capacitance

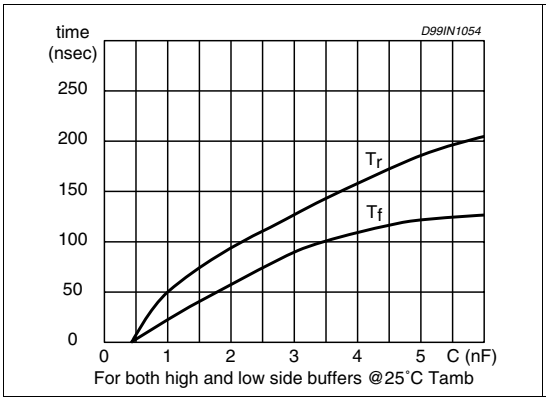


Figure 7. Quiescent current vs supply voltage

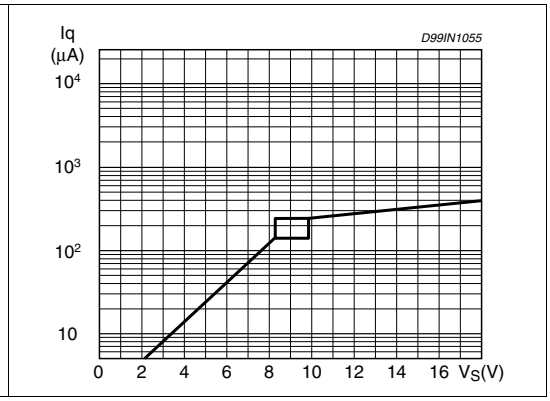


Figure 8. V_{BOOT} UV turn on threshold vs temperature

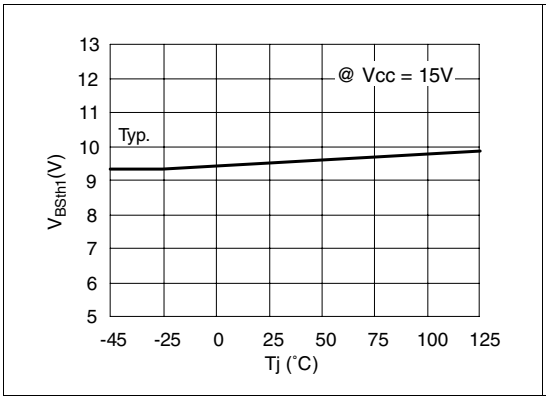


Figure 9. V_{CC} UV turn off threshold vs temperature

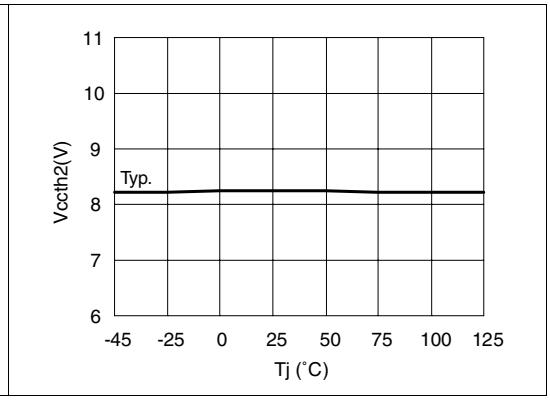


Figure 10. V_{BOOT} UV turn off threshold vs temperature

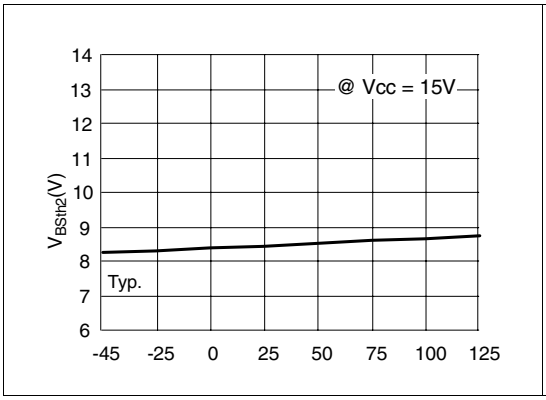


Figure 11. Output source current vs temperature

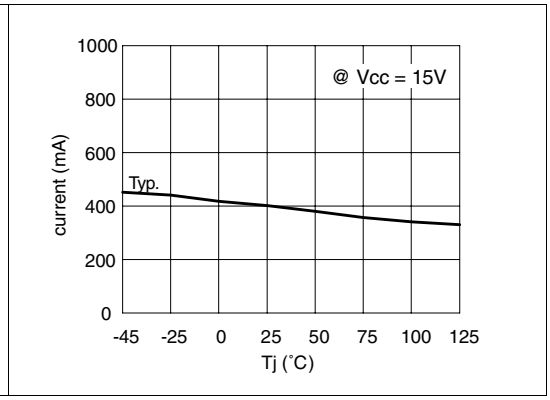


Figure 12. V_{CC} UV turn on threshold vs temperature

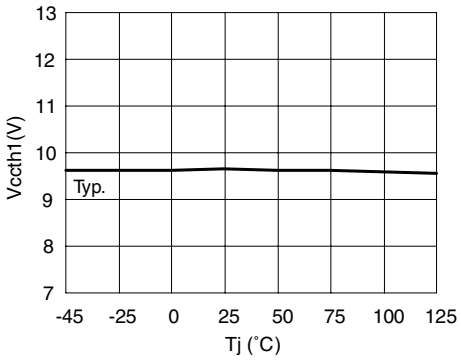
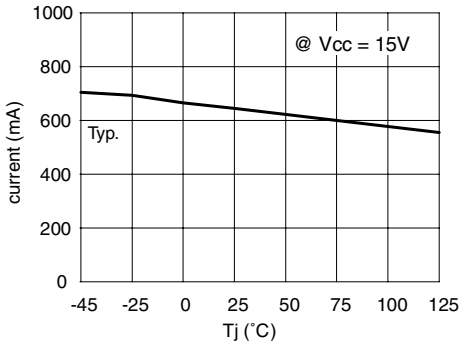


Figure 13. Output sink current vs temperature



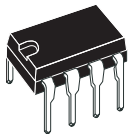
8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Figure 14. DIP-8 mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

OUTLINE AND MECHANICAL DATA



DIP-8

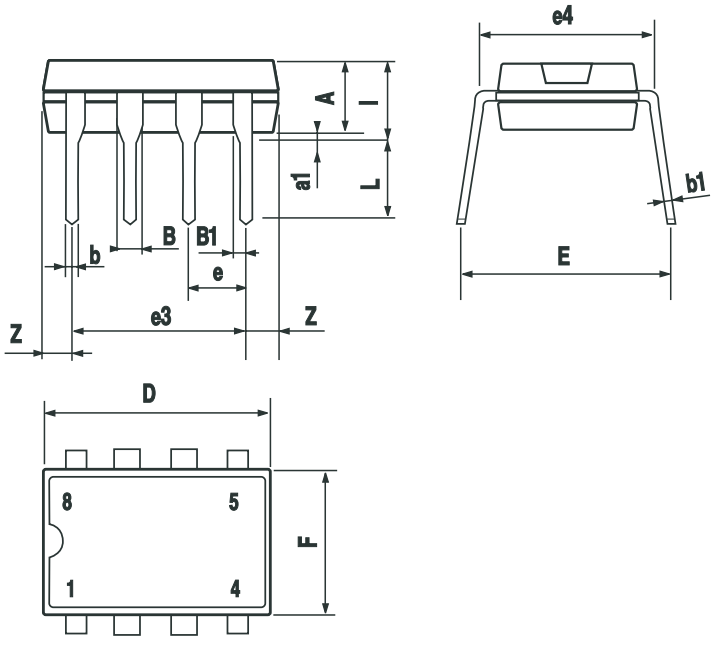
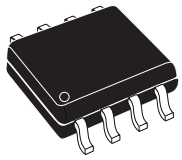


Figure 15. SO-8 mechanical data and package dimensions

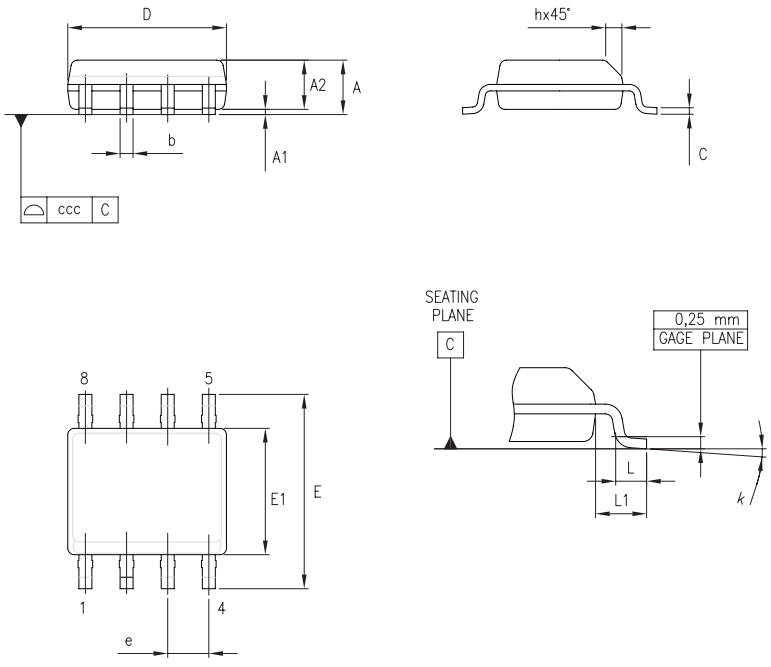
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.750			0.0689
A1	0.100		0.250	0.0039		0.0098
A2	1.250			0.0492		
b	0.280		0.480	0.0110		0.0189
c	0.170		0.230	0.0067		0.0091
D (1)	4.800	4.900	5.000	0.1890	0.1929	0.1969
E	5.800	6.000	6.200	0.2283	0.2362	0.2441
E1(2)	3.800	3.900	4.000	0.1496	0.1535	0.1575
e		1.270			0.0500	
h	0.250		0.500	0.0098		0.0197
L	0.400		1.270	0.0157		0.0500
L1		1.040			0.0409	
k	0°		8°	0°		8°
ccc			0.100			0.0039

Notes: 1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, potrusions or gate burrs shall not exceed 0.15mm in total (both side).
2. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

OUTLINE AND MECHANICAL DATA



SO-8



9 Order codes

Table 7. Order codes

Part number	Package	Packaging
L6388E	DIP-8	Tube
L6388ED	SO-8	Tube
L6388ED013TR	SO-8	Tape and reel

10 Revision history

Table 8. Document revision history

Date	Revision	Changes
11-Oct-2007	1	First release

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