

QUAD BISTABLE TRANSPARENT LATCH

FEATURES

- Complementary Q and \bar{Q} outputs
- VCC and GND on the centre pins
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT75 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT75 have four bistable latches. The two latches are simultaneously controlled by one of two active HIGH enable inputs (LE₁₋₂ and LE₃₋₄). When LE_{n-n} is HIGH, the data enters the latches and appears at the nQ outputs. The nQ outputs follow the data inputs (nD) as long as LE_{n-n} is HIGH (transparent). The data on the nD inputs one set-up time prior to the HIGH-to-LOW transition of the LE_{n-n} will be stored in the latches. The latched outputs remain stable as long as the LE_{n-n} is LOW.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PHL} / t _{PLH}	propagation delay nD to nQ, n \bar{Q} LE _{n-n} to nQ, n \bar{Q}	C _L = 15 pF V _{CC} = 5 V	11 11	12 11	ns ns
C _I	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per latch	notes 1 and 2	42	42	pF

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μ W):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:
 f_i = input frequency in MHz C_L = output load capacitance in pF
 f_o = output frequency in MHz V_{CC} = supply voltage in V
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
 For HCT the condition is V_I = GND to V_{CC} - 1.5 V

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z).
 16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 14, 11, 8	1 \bar{Q} to 4 \bar{Q}	complementary latch outputs
2, 3, 6, 7	1D to 4D	data inputs
4	LE ₃₋₄	latch enable input, latches 3 and 4 (active HIGH)
5	V _{CC}	positive supply voltage
12	GND	ground (0 V)
13	LE ₁₋₂	latch enable input, latches 1 and 2 (active HIGH)
16, 15, 10, 9	1Q to 4Q	latch outputs

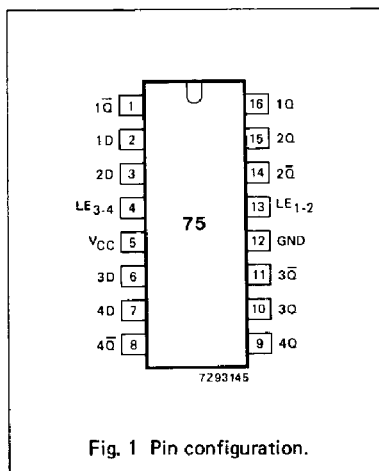


Fig. 1 Pin configuration.

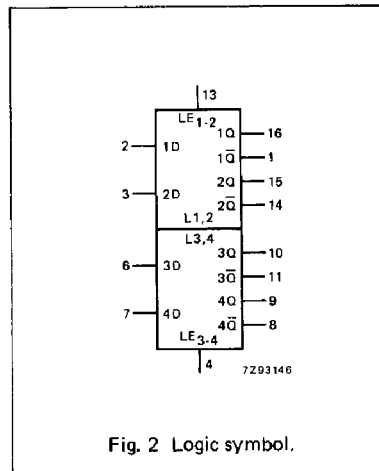


Fig. 2 Logic symbol.

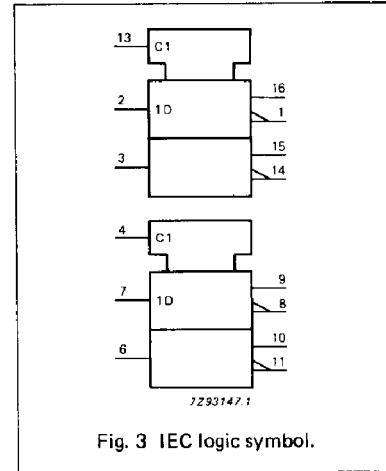
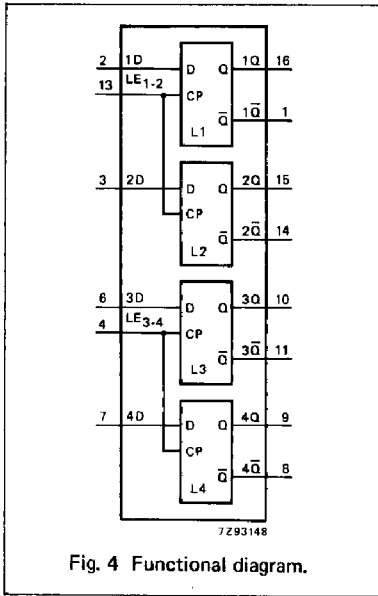


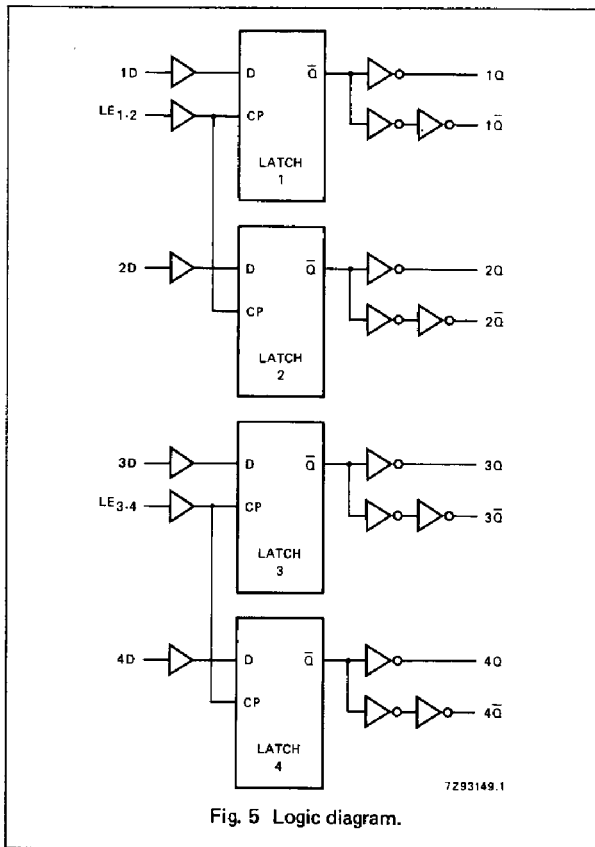
Fig. 3 IEC logic symbol.



FUNCTION TABLE

OPERATING MODES	INPUTS		OUTPUTS	
	LE _{n-n}	nD	nQ	nQ̄
data enabled	H	L	L	H
	H	H	H	L
data latched	L	X	q	q̄

H = HIGH voltage level
 L = LOW voltage level
 q = lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW LE_{n-n} transition
 X = don't care



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HC							V _{CC} V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.		max.		
t _{PHL} / t _{PLH}	propagation delay nD to nQ		33 12 10	110 22 19		140 28 24		165 33 28	ns	2.0 4.5 6.0	Fig. 6
t _{PHL} / t _{PLH}	propagation delay nD to nQ̄		39 14 11	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 7
t _{PHL} / t _{PLH}	propagation delay LE _{n-n} to nQ		33 12 10	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 8
t _{PHL} / t _{PLH}	propagation delay LE _{n-n} to nQ̄		39 14 11	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 8
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7
t _W	enable pulse width HIGH	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t _{su}	set-up time nD to LE _{n-n}	60 12 10	14 5 4		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 9
t _h	hold time nD to LE _{n-n}	3 3 3	-8 -3 -2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig. 9

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

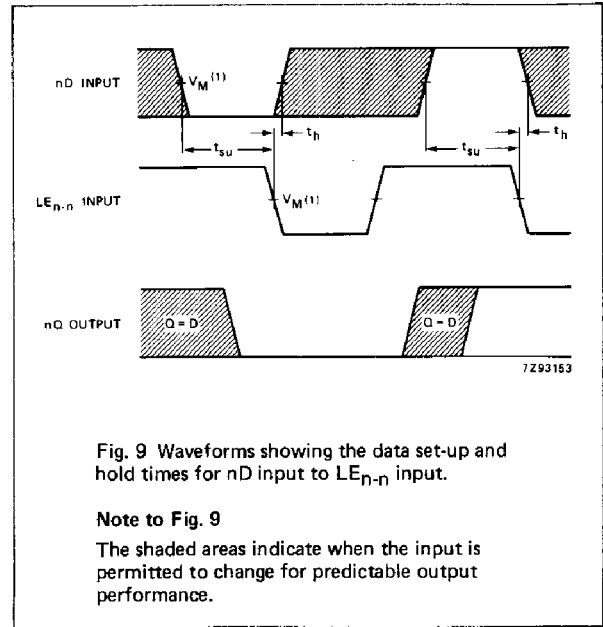
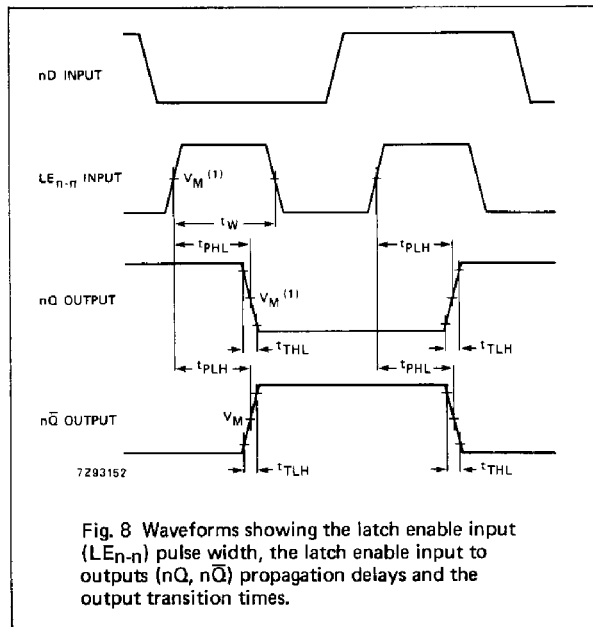
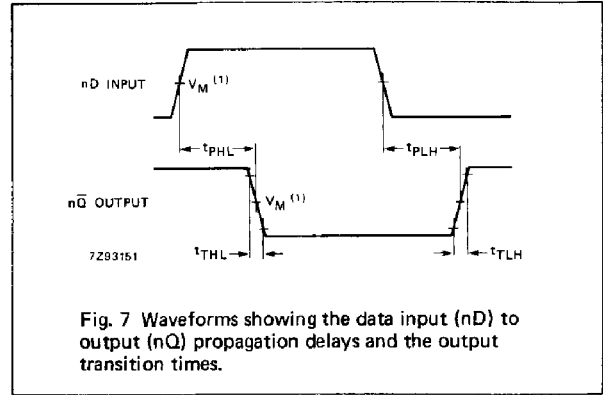
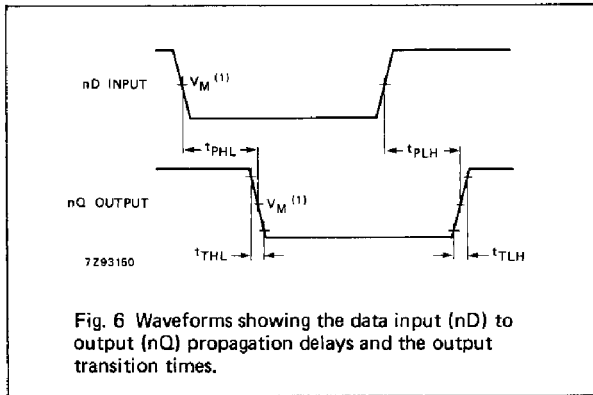
INPUT	UNIT LOAD COEFFICIENT
nD	0.75
LE _{n-n}	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)						UNIT	TEST CONDITIONS		
		74HCT							V_{CC} V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t_{PHL}/t_{PLH}	propagation delay nD to nQ		15	28		35		42	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay nD to n \bar{Q}		15	28		35		42	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay LE _{n-n} to nQ		13	28		35		42	ns	4.5	Fig. 8
t_{PHL}/t_{PLH}	propagation delay LE _{n-n} to n \bar{Q}		15	30		38		45	ns	4.5	Fig. 8
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7
t_W	enable pulse width HIGH	16	4		20		24		ns	4.5	Fig. 8
t_{su}	set-up time nD to LE _{n-n}	12	4		15		18		ns	4.5	Fig. 9
t_h	hold time nD to LE _{n-n}	3	-2		3		3		ns	4.5	Fig. 9

AC WAVEFORMS



Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_1 = \text{GND to } V_{CC}$.
 HCT: $V_M = 1.3 \text{ V}$; $V_1 = \text{GND to } 3 \text{ V}$.

Note to Fig. 9

The shaded areas indicate when the input is permitted to change for predictable output performance.