Octal bus transceiver/register (3-State)

74AC646
74ACT646

FEATURES

- 74ACT646 has TTL-compatible inputs
- 74AC646 has CMOS-compatible inputs
- 3-State outputs source/sink 24mA
- 3-State outputs drive bus lines or buffer memory address registers
- Meets or exceeds JEDEC standard for 74AC(T)XX family
- Superior ground bounce noise immunity

DESCRIPTION

The 74AC646/74ACT646 is an octal bus transceiver/register consisting of non-inverting bus transceiver circuits with 3-State outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the internal registers.

Data on the 'A' or 'B' bus will be clocked in the internal registers, as the appropriate clock (CP_{AB} or CP_{BA}) goes to a HIGH logic level. Output enable ($\overline{OE}$) and direction (DIR) inputs are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the 'A' or 'B' register, or in both. The select source inputs (S_{AB} and S_{BA}) can multiplex stored and real-time (transparent mode) data.

The direction (DIR) input determines which bus will receive data when $\overline{OE}$ is active (LOW). In the isolation mode (OE = HIGH), 'A' data may be stored in the 'B' register and/or 'B' data may be stored in the 'A' register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, 'A' or 'B' may be driven at a time.

The '646' is functionally identical to the '648' but has non-inverting data paths.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL			UNIT
			AC		ACT	
			V_{CC} = 3.3V	V_{CC} = 5.0V	V_{CC} = 5.0V	
t_{PLH}/t_{PHL}	Propagation delay An, Bn to Bn, An; CP_{AB}, CP_{BA} to Bn, An; S_{AB}, S_{BA} to Bn, An	C_L = 50pF	5.1 6.0 6.5	3.5 4.2 4.6	5.8 5.9 6.6	ns
C_I	Input capacitance		4.5			pF
C_{PD}	Power dissipation capacitance per channel	V_{in} = GND to V_{CC}[1] outputs enabled outputs disabled	33 6		30 6	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING AND PACKAGE INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
24-Pin Plastic SO	–40°C to +85°C	74AC646 D 74ACT646 D	74AC646 D 74ACT646 D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74AC646 DB 74ACT646 DB	74AC646 DB 74ACT646 DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74AC646 PW 74ACT646 PW	74AC646PW DH 74ACT646PW DH	SOT355-1

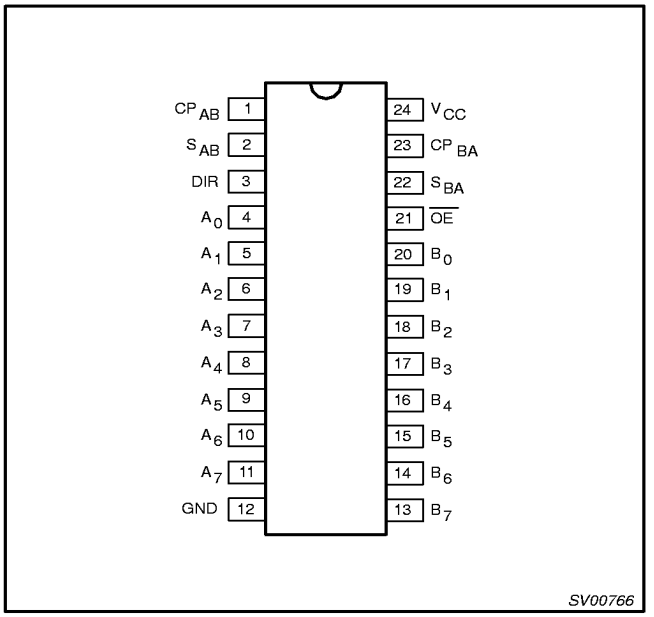
Octal bus transceiver/register (3-State)

74AC646
74ACT646

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	CP_{AB}	'A' to 'B' clock input (LOW-to-HIGH, edge-triggered)
2	S_{AB}	Select 'A' to 'B' source input
3	DIR	Direction control input
4, 5, 6, 7, 8, 9, 10, 11	A_0 to A_7	'A' data inputs/outputs
12	GND	Ground (0V)
20, 19, 18, 17, 16, 15, 14, 13	B_0 to B_7	'B' data inputs/outputs
21	$\overline{OE}$	Output enable input (active LOW)
22	S_{BA}	Select 'B' to 'A' source input
23	CP_{BA}	'B' to 'A' clock input (LOW-to-HIGH, edge-triggered)
24	V_{CC}	Positive supply voltage

PIN CONFIGURATION



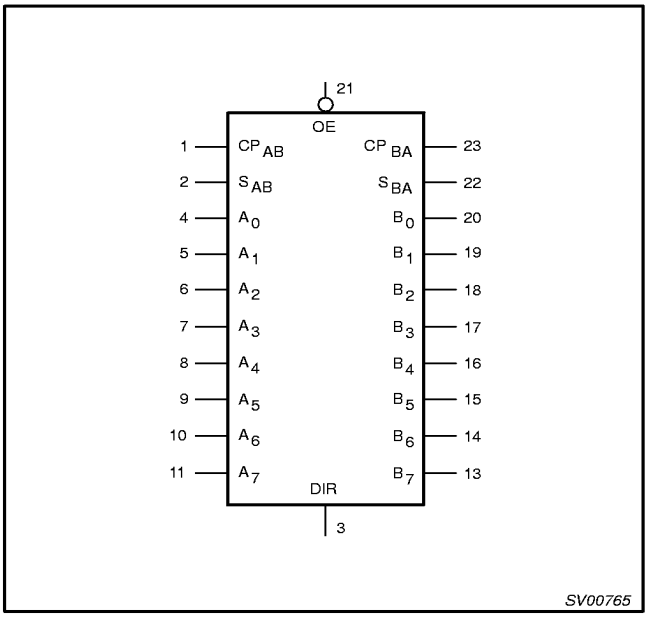
FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
$\overline{OE}$	DIR	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	A_0 to A_7	B_0 to B_7	
X X	X X	↑ X	X ↑	X X	X X	input un *	un * input	Store A, B unspecified * Store B, A unspecified *
H H	X X	↑ H or L	↑ H or L	X X	X X	input	input	Store A and B data, Isolation hold storage
L L	L L	X X	X H or L	X X	L H	output	input	Real-time B data to A bus Stored B data to A bus
L L	H H	X H or L	X X	L H	X X	input	output	Real-time A data to B bus Stored A data to B bus

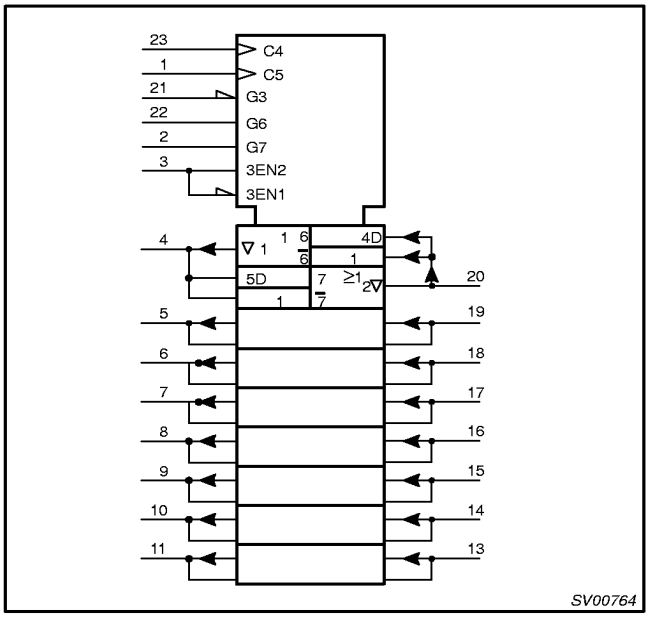
* The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

un = unspecified
H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW–to–HIGH level transition

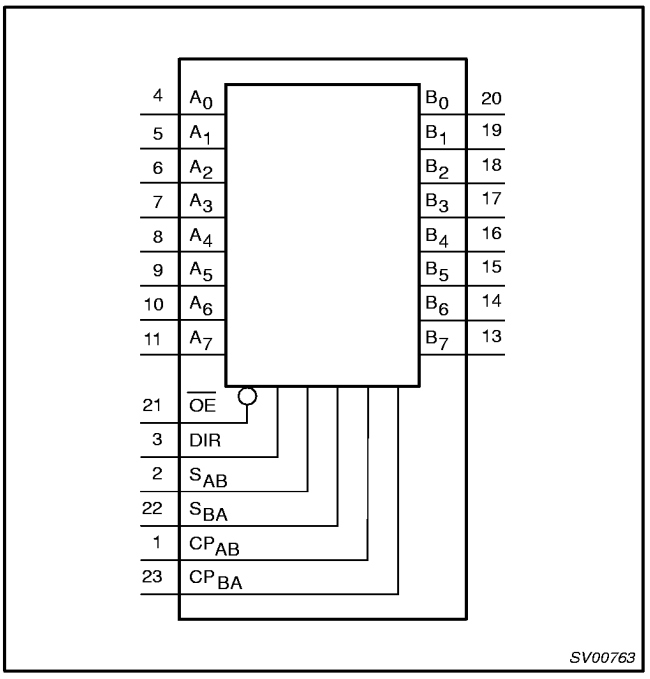
LOGIC SYMBOL



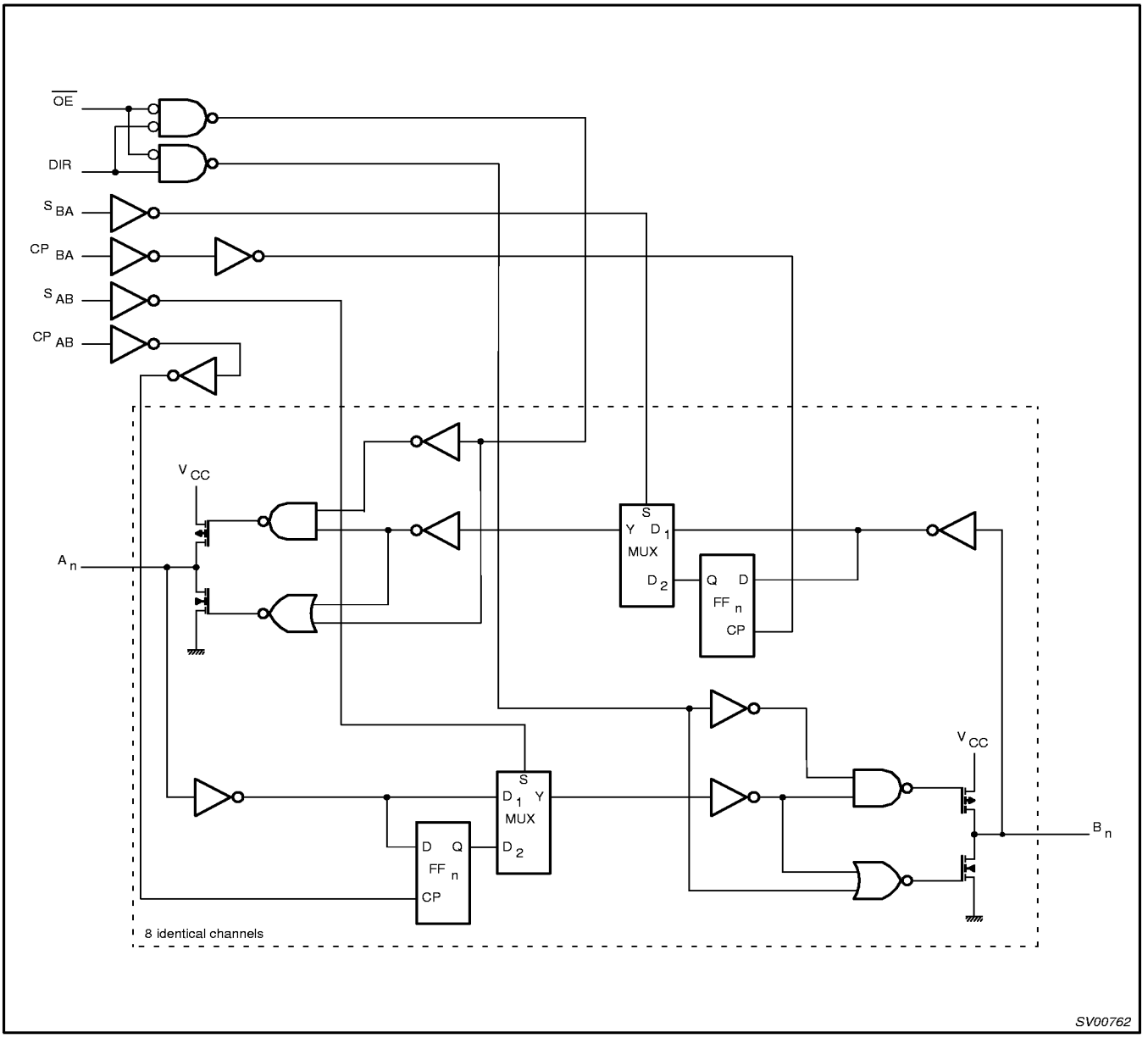
LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage for 'AC	2.0	6.0	V
V_{CC}	DC supply voltage for 'ACT	4.5	5.5	V
V_I	DC input voltage range	0	V_{CC}	V
V_O	DC output voltage range	0	V_{CC}	V
T_{amb}	Operating free-air temperature range	–40	+85	°C
$\Delta V/\Delta t$	Minimum input edge rate — AC devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125		mV/ns
	— ACT devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125		

ABSOLUTE MAXIMUM RATINGS[1]

in accordance with the Absolute Maximum Rating System (IEC134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	V_I = –0.5V	–20	mA
		V_I = V_{CC} + 0.5V	+20	
V_I	DC input voltage		–0.5 to V_{CC} +0.5	V
I_{OK}	DC output diode current	V_O = –0.5V	–20	mA
		V_O = V_{CC} + 0.5V	+20	
V_O	DC output voltage		–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current		± 50	mA
I_{CC}, I_{GND}	DC V_{CC} or GND current per output		± 50	mA
I_{CC}, I_{GND}	DC V_{CC} or GND current		± 200	mA
T_{stg}	Storage temperature range		–65 to 150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	500 500	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS FOR AC FAMILY

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	V_{CC} (V)	LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{OUT} = 0.1V or (V_{CC} – 0.1V)	3.0	2.1	1.5		V
			4.5	3.15	2.25		
			5.5	3.85	2.75		
V_{IL}	LOW level Input voltage	V_{OUT} = 0.1V or (V_{CC} – 0.1V)	3.0		1.5	0.9	V
			4.5		2.25	1.35	
			5.5		2.75	1.65	
V_{OH}	HIGH level output voltage	I_{OUT} = –50 μA	3.0	2.9	2.99		V
			4.5	4.4	4.49		
			5.5	5.4	5.49		
		V_{IN} = V_{IL} or V_{IH}, I_{OH} = –12mA[1]	3.0	2.46			V
		V_{IN} = V_{IL} or V_{IH}, I_{OH} = –24mA[1]	4.5	3.76			
		V_{IN} = V_{IL} or V_{IH}, I_{OH} = –24mA[1]	5.5	4.76			
V_{OL}	LOW level output voltage	I_{OUT} = 50 μA	3.0		0.01	0.1	V
			4.5		0.01	0.1	
			5.5		0.01	0.1	
		V_{IN} = V_{IL} or V_{IH}, I_{OL} = 12mA[1]	3.0			0.44	V
		V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24mA[1]	4.5			0.44	
		V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24mA[1]	5.5			0.44	
I_{IN}	Input leakage current	V_{IN} = V_{CC}, GND	5.5			±1.0	μA
I_{OZ}	3-State output OFF-state current	V_{IN} = V_{IL}, V_{IH} V_{OUT} = V_{CC}, GND	5.5			±2.5	μA
I_{OLD}	Dynamic output current[2]	V_{OLD} = 1.65V max	5.5	75			mA
I_{OHD}	Dynamic output current[2]	V_{OHD} = 3.85V min	5.5			–75	mA
I_{CC}	Quiescent supply current	V_{IN} = V_{CC} or GND	5.5			40	μA

NOTES:
1. All outputs loaded
2. Maximum test duration 2.0 ms; one output loaded at a time

DC ELECTRICAL CHARACTERISTICS FOR ACT FAMILY

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	V_{CC} (V)	LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{OUT} = 0.1V or (V_{CC} – 0.1V)	4.5	2.0	1.5		V
			5.5	2.0	1.5		
V_{IL}	LOW level Input voltage	V_{OUT} = 0.1V or (V_{CC} – 0.1V)	4.5		1.5	0.8	V
			5.5		1.5	0.8	
V_{OH}	HIGH level output voltage	I_{OUT} = –50 μA	4.5	4.4	4.49		V
			5.5	5.4	5.49		
		V_{IN} = V_{IL} or V_{IH}, I_{OH} = –24mA[1]	4.5	3.76			V
		V_{IN} = V_{IL} or V_{IH}, I_{OH} = –24mA[1]	5.5	4.76			
V_{OL}	LOW level output voltage	I_{OUT} = 50 μA	4.5		0.01	0.1	V
			5.5		0.01	0.1	
		V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24mA[1]	4.5			0.44	V
		V_{IN} = V_{IL} or V_{IH}, I_{OL} = 24mA[1]	5.5			0.44	
I_{IN}	Input leakage current	V_{IN} = V_{CC}, GND	5.5			±1.0	μA
I_{OZ}	3-State output OFF-state current	V_{IN} = V_{IL}, V_{IH} V_{OUT} = V_{CC}, GND	5.5			±2.5	μA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{IN} = V_{CC} – 2.1V Other inputs at V_{CC} or GND; I_{OUT} = 0	5.5			1.5	mA
I_{OLD}	Dynamic output current[2]	V_{OLD} = 1.65V max	5.5	75			mA
I_{OHD}	Dynamic output current[2]	V_{OHD} = 3.85V min	5.5			–75	mA
I_{CC}	Quiescent supply current	V_{IN} = V_{CC} or GND	5.5			40	μA

NOTES:
1. All outputs loaded
2. Maximum test duration 2.0ms, one output loaded at a time

AC CHARACTERISTICS FOR (74AC646)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; .

SYMBOL	PARAMETER	V_{CC}[1]	LIMITS					UNIT	WAVEFORM
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C			
			MIN	TYP	MAX	MIN	MAX		
t_{PLH}	Propagation delay An, Bn to Bn, An	3.3 5.0	2.0 1.5	5.0 3.4	12 8	1.5 1.0	13.5 9	ns	1
t_{PHL}	Propagation delay An, Bn to Bn, An	3.3 5.0	2.0 1.5	5.2 3.7	12 8	1.5 1.0	13.5 9	ns	1
t_{PLH}	Propagation delay CP_{AB}, CP_{BA} to Bn, An	3.3 5.0	2.0 1.5	5.9 4.0	14 9.5	1.5 1.0	16 11	ns	2
t_{PHL}	Propagation delay CP_{AB}, CP_{BA} to Bn, An	3.3 5.0	2.0 1.5	6.1 4.3	14 9.5	1.5 1.0	16 11	ns	2
t_{PLH}	Propagation delay S_{AB}, S_{BA} to Bn, An	3.3 5.0	2.0 1.5	6.2 4.2	13 9	1.5 1.0	15 10	ns	3
t_{PHL}	Propagation delay S_{AB}, S_{BA} to Bn, An	3.3 5.0	2.0 1.5	6.8 4.9	13 9	1.5 1.0	15 10	ns	3
t_{PZH}	3-State output enable time $\overline{OE}$ to B_n, A_n	3.3 5.0	2.0 1.5	5.6 3.9	11 7.5	1.5 1.0	12.5 8.5	ns	4
t_{PZL}	3-State output enable time $\overline{OE}$ to B_n, A_n	3.3 5.0	2.0 1.5	6.5 4.5	11 7.5	1.5 1.0	12.5 8.5	ns	4
t_{PHZ}	3-State output disable time $\overline{OE}$ to B_n, A_n	3.3 5.0	2.0 1.5	4.9 3.2	11 7.5	1.5 1.0	12 8.5	ns	4
t_{PLZ}	3-State output disable time $\overline{OE}$ to B_n, A_n	3.3 5.0	2.0 1.5	4.5 3.2	11 7.5	1.5 1.0	12 8.5	ns	4
t_{PZH}	3-State output enable time DIR to B_n, A_n	3.3 5.0	2.0 1.5	5.5 3.8	10.5 7	1.5 1.0	12 8	ns	5
t_{PZL}	3-State output enable time DIR to B_n, A_n	3.3 5.0	2.0 1.5	6.4 4.5	10.5 7	1.5 1.0	12 8	ns	5
t_{PHZ}	3-State output disable time DIR to B_n, A_n	3.3 5.0	2.0 1.5	5.1 2.9	10.5 7	1.5 1.0	11.5 8	ns	5
t_{PLZ}	3-State output disable time DIR to B_n, A_n	3.3 5.0	2.0 1.5	4.6 2.7	10.5 7	1.5 1.0	11.5 8	ns	5
t_w	Clock pulse width HIGH or LOW CP_{AB} or CP_{BA}	3.3 5.0	4 3	2 1		4.5 3.5		ns	2
t_{su}	Set up time A_n, B_n to CP_{AB}, CP_{BA}	3.3 5.0	3.5 3.0	0.5 0.3		4 3.5		ns	2
t_h	Hold time A_n, B_n to CP_{AB}, CP_{BA}	3.3 5.0	0.5 1.0	–0.2 –0.1		1.0 1.5		ns	2
f_{max}	Maximum clock pulse frequency	3.3 5.0	75 110	120 180		60 100		MHz	2

NOTE:

1. Voltage range 3.3V is V_{CC} = 3.3V ± 0.3V
   Voltage range 5.0V is V_{CC} = 5.0V ± 0.5V

AC CHARACTERISTICS FOR (74ACT646)

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; .

SYMBOL	PARAMETER	V_{CC}[1]	LIMITS					UNIT	WAVEFORM
			T_{amb} = +25°C			T_{amb} = −40°C to +85°C			
			MIN	TYP	MAX	MIN	MAX		
t_{PLH}	Propagation delay An, Bn to Bn, An	5.0	2.0	6.1	10	1.5	11.5	ns	1
t_{PHL}	Propagation delay An, Bn to Bn, An	5.0	2.0	5.5	10	1.5	11.5	ns	1
t_{PLH}	Propagation delay CP_{AB}, CP_{BA} to Bn, An	5.0	2.0	5.9	14	1.5	16	ns	2
t_{PHL}	Propagation delay CP_{AB}, CP_{BA} to Bn, An	5.0	2.0	5.9	14	1.5	16	ns	2
t_{PLH}	Propagation delay S_{AB}, S_{BA} to Bn, An	5.0	2.0	6.4	11	1.5	12.5	ns	3
t_{PHL}	Propagation delay S_{AB}, S_{BA} to Bn, An	5.0	2.0	6.9	11	1.5	12.5	ns	3
t_{PZH}	3-State output enable time $\overline{OE}$ to Bn, An	5.0	2.0	4.9	10.5	1.5	12	ns	4
t_{PZL}	3-State output enable time $\overline{OE}$ to Bn, An	5.0	2.0	6	10.5	1.5	12	ns	4
t_{PHZ}	3-State output disable time $\overline{OE}$ to Bn, An	5.0	2.0	4.6	10.5	1.5	11.5	ns	4
t_{PLZ}	3-State output disable time $\overline{OE}$ to Bn, An	5.0	2.0	4.5	10.5	1.5	11.5	ns	4
t_{PZH}	3-State output enable time DIR to Bn, An	5.0	2.0	4.9	10	1.5	11.5	ns	5
t_{PZL}	3-State output enable time DIR to Bn, An	5.0	2.0	5.8	10	1.5	11.5	ns	5
t_{PHZ}	3-State output disable time DIR to Bn, An	5.0	2.0	3.8	10	1.5	11	ns	5
t_{PLZ}	3-State output disable time DIR to Bn, An	5.0	2.0	3.9	10	1.5	11	ns	5
t_w	Clock pulse width HIGH or LOW CP_{AB} or CP_{BA}	5.0	5.0	3		5.5		ns	2
t_{su}	Set up time A_n, B_n to CP_{AB}, CP_{BA}	5.0	5.0	1.4		5.5		ns	2
t_h	Hold time A_n, B_n to CP_{AB}, CP_{BA}	5.0	0.5	−1.3		1.0		ns	2
f_{max}	Maximum clock pulse frequency	5.0	110	180		100		MHz	2

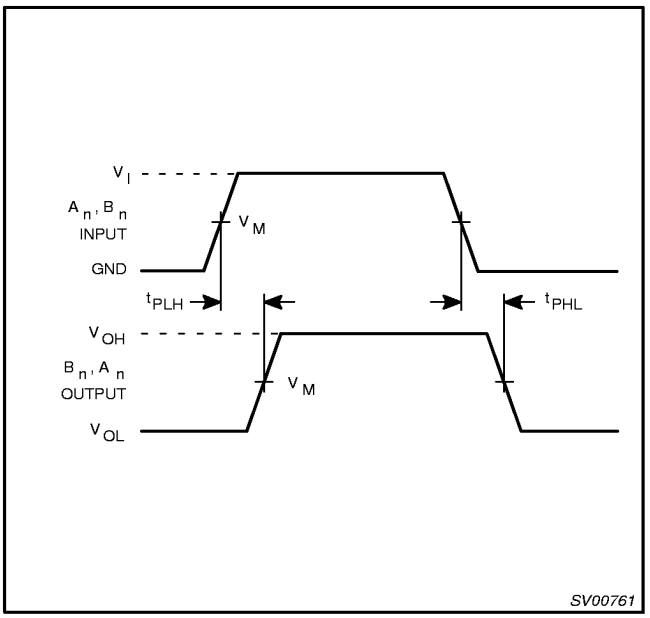
NOTE:

1. These values are at V_{CC} = 5.0V ± 0.5V

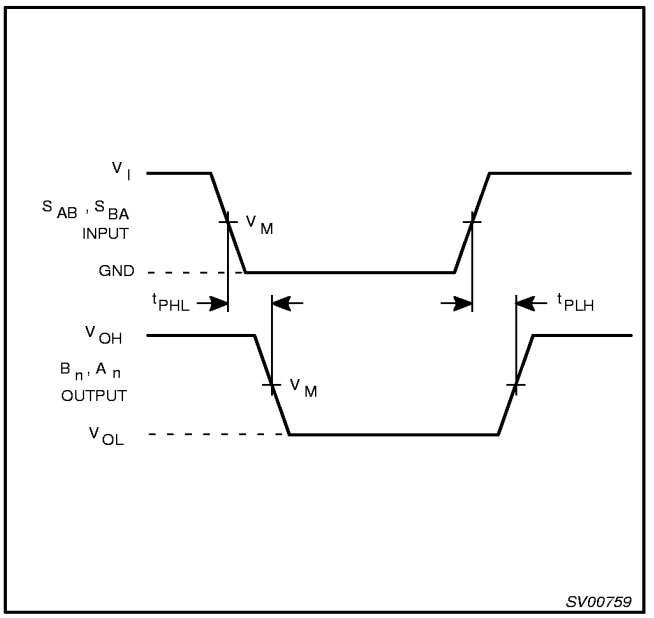
AC WAVEFORMS

V_{OL} and V_{OH} are the typical output voltage drops that occur with the output load.

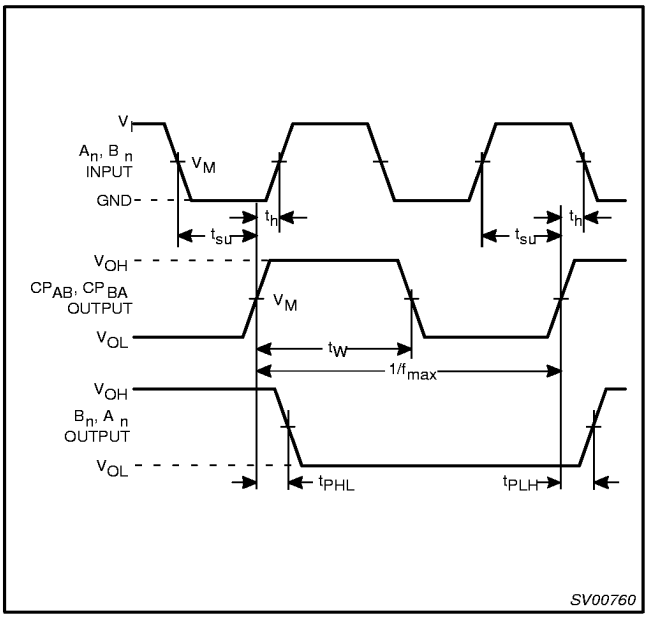
$V_X = V_{OL} + 0.3V$
$V_Y = V_{OH} - 0.3V$



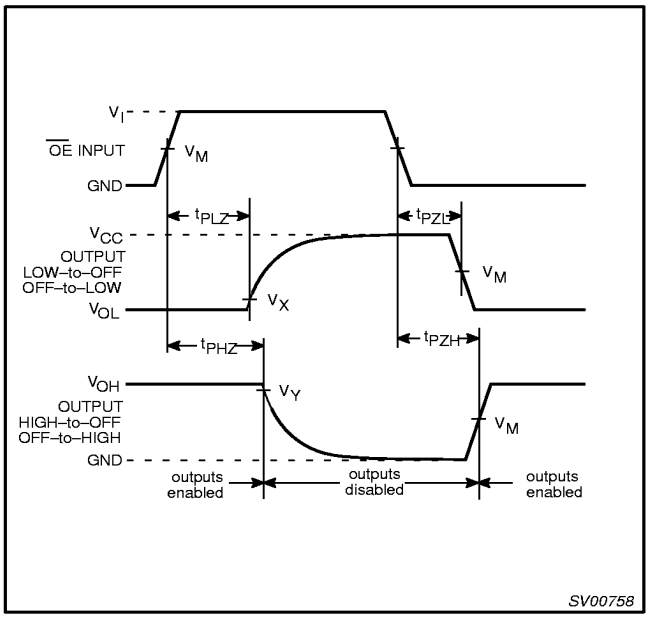
Waveform 1. Input An, Bn to output Bn, An propagation delays.



Waveform 3. Input S_{AB}, S_{BA} to output B_n, A_n propagation delay times.



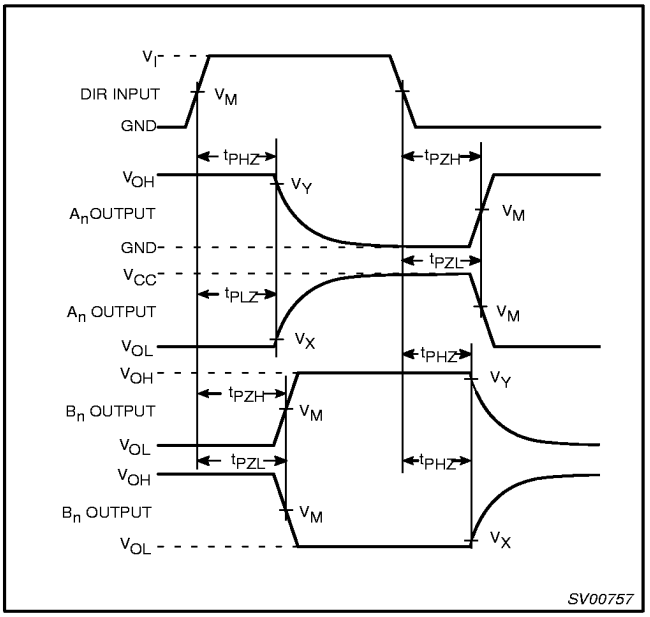
Waveform 2.A_n, B_n to CP_{AB}, CP_{BA} set-up and hold times, clock CP_{AB}, CP_{BA} pulse width, maximum clock pulse frequency and the CP_{AB}, CP_{BA} to output B_n, A_n propagation delays.



Waveform 4. Input $\overline{OE}$ to output A_n, B_n 3-State enable and disable times.

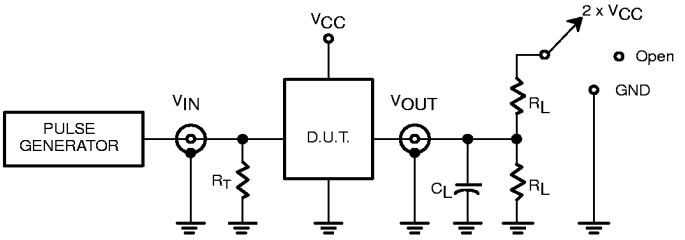
AC WAVEFORMS (Continued)

V_{OL} and V_{OH} are the typical output voltage drops that occur with the output load.
$V_X = V_{OL} + 0.3V$
$V_Y = V_{OH} - 0.3V$



Waveform 5. Input DIR to output A_n, B_n 3-State enable and disable times.

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	Open

FAMILY	V_{IN} Input Requirements	V_m Input	V_m Output
AC	GND to V_{CC}	50% V_{CC}	50% V_{CC}
ACT	GND to 3.0V	1.5V	50% V_{CC}

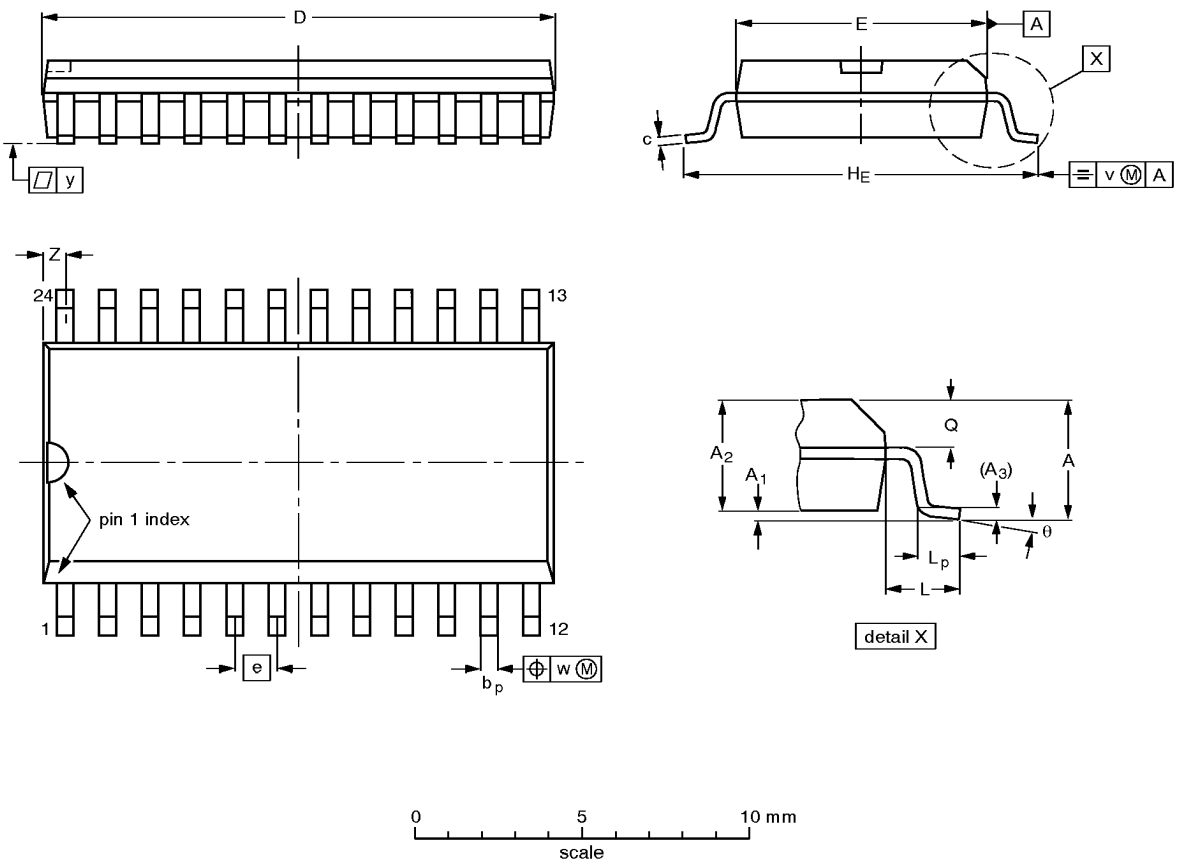
DEFINITIONS

R_L = Load resistor; see AC characteristics for value.
C_L = Load capacitance, see AC characteristics
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SV00451

Waveform 6. Load circuitry for switching times.

SO24: plastic small outline package; 24 leads; body width 7.5 mm SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

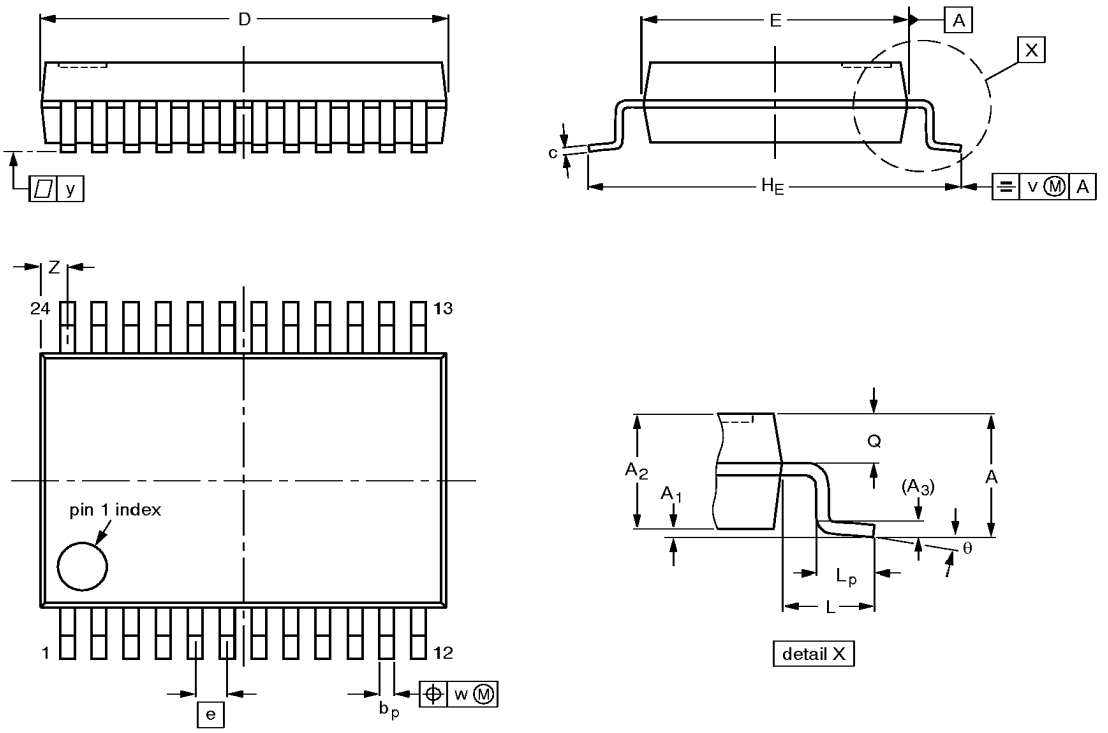
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

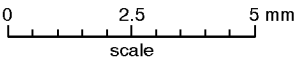
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~92-11-17~~ 95-01-24

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**





DIMENSIONS (mm are the original dimensions)

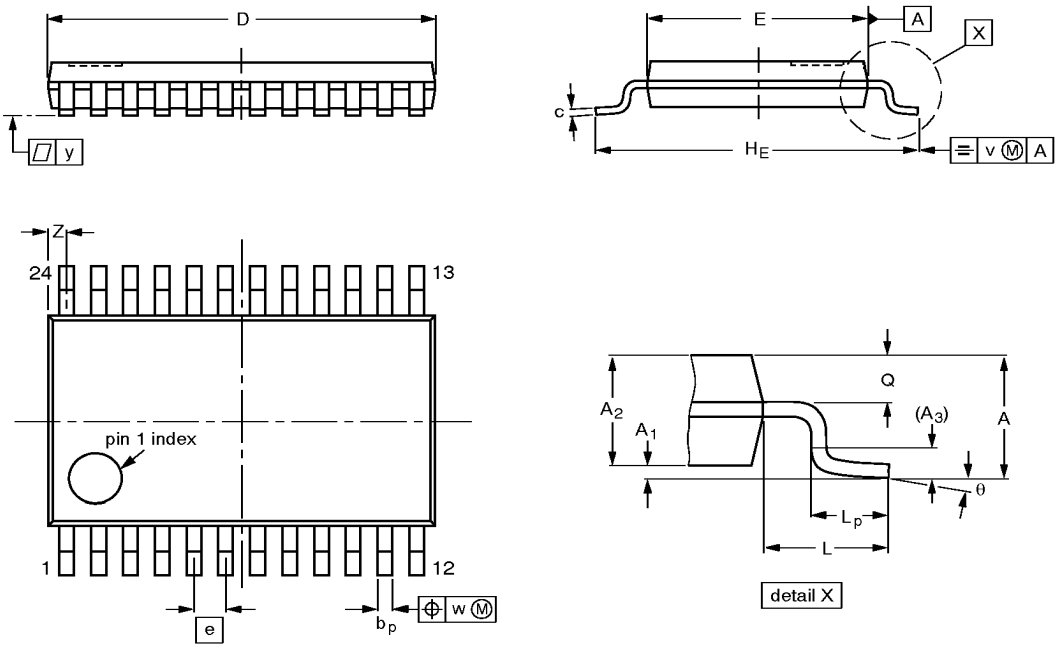
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

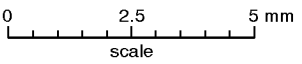
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				~~93-09-08~~ 95-02-04

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153AD				~~93-06-16~~ 95-02-04