

SCDS264D - JANUARY 2008-REVISED JANUARY 2010

4-CHANNEL DIFFERENTIAL 8:16 MULTIPLEXER SWITCH FOR DVI/HDMI APPLICATIONS

Check for Samples: TS3DV421

FEATURES

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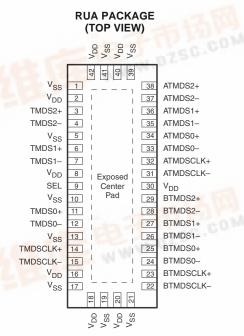
- Compatible With HDMI v1.3 DVI 1.0 **High-Speed Digital Interface**
 - Wide Bandwidth of Over 3.8 Gbps
 - Serial Data Stream at 10x Pixel Clock Rate
 - Supports All Video Formats up to 1080p and SXGA (1280 x 1024 at 75 Hz)
 - High Bandwidth of 4.95 Gbps (Single Link)
 - HDCP Compatible
- Low Crosstalk $(X_{TALK} = -50 \text{ dB Typ at } 1.65 \text{ Gbps})$
- Off Isolation (O_{IRR} = -50 dB Typ at 1.65 Gbps)
- Low Bit-to-Bit Skew ($t_{sk(o)} = 0.1$ ns Max)
- Low and Flat ON-State Resistance $(r_{ON} = 12.5 \Omega Max, r_{ON(flat)} = 0.5 \Omega Typ)$
- Low Input/Output Capacitance $(C_{ON} = 4.5 \text{ pF Max})$
- Enables Application-Specific Operating Voltage Selection
 - V_{DD} Operating Range From 1.5 V to 2.1 V When V_{ss} = GND
 - V_{DD} Operating Range From 3.0 V to 3.6 V When $V_{SS} = 1.5 V$
- Ioff Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- For DisplayPort Applications: $V_{DD} = 1.8 V$, $V_{SS} = GND$
- For HDMI /DVI Applications: $V_{DD} = 3.3 V$, $V_{SS} = 1.5 V$

APPLICATIONS

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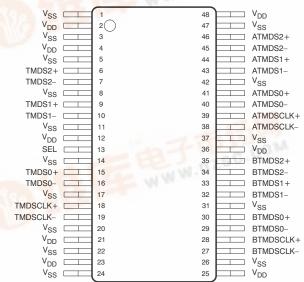
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- **DVI/HDMI Signal Switching**
- **Differential DVI, HDMI Signal Multiplexing for** Audio/Video Receivers and High-Definition **Televisions (HDTVs)**



For RUA, the exposed center pad must be connected to V_{SS} or electronically open. For this part to be used in HDMI/TMDS applications, V_{SS} can be elevated to 1.5 V. See Figure 1.





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DESCRIPTION/ORDERING INFORMATION

The TS3DV421 is a 4-channel differential 2:1 multiplexer/demultiplexer digital video switch controlled with one select input (SEL). SEL controls the data path of the multiplexer/demultiplexer and can be connected to any GPIO in the system, using an external voltage divider system. The device provides high bandwidth necessary for DVI and HDMI applications. This device expands the high-speed physical link interface from a single HDMI port to two HDMI ports (A or B port). The unselected channel is set to a high-impedance state.

The most common application for the TS3DV421 is in the sink application. In this case, there are two sources (i.e., DVD, set-top box, or game console) that must be routed to one HDMI receiver. The TS3DV421 can route the signals where one HDMI receiver (in a DLP, LCD TV, PDP, or other high-definition display) can be expanded to three ports.

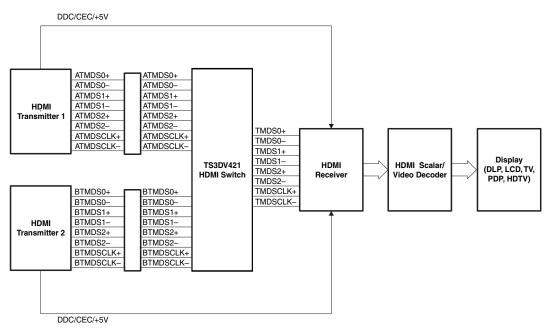
The HDMI application calls for a $100-\Omega$ differential impedance between the differential lines (TMDSn+ and TMDSn-). Additionally, because the TS3DV421 is a high-bandwidth, low-r_{ON} pass transistor-type switch, a properly designed board retains a $100-\Omega$ differential impedance through the switch. The unselected port is in the high-impedance mode, such that the receiver receives information from only one source. HDCP encryption is passed through the switch for the HDMI receiver to decode.

Table 1. ORDERING INFORMATION

T _A	PACKAG	E ⁽¹⁾ (2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
4000 1- 0500	QFN – RUA Tape and reel		TS3DV421RUAR	SD421	
–40°C to 85°C	TVSOP – DGV	Tape and reel	TS3DV421DGVR	SD421	

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



TYPICAL APPLICATION

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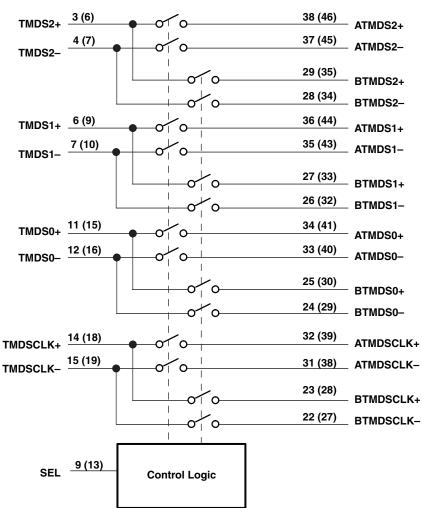
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SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High impedance BTMDSn- = High impedance BTMDSCLK+ = High impedance BTMDSCLK- = High impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
Н	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High impedance ATMDSn- = High impedance ATMDSCLK+ = High impedance ATMDSCLK- = High impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-

Table 2. FUNCTION TABLE



FUNCTIONAL DIAGRAM

A. TVSOP package pin identification in parenthesis.

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		_	TERM	INAL FUNCTIONS			
	TERMINAL						
	N	ю.	TYPE	DESCRIPTION			
NAME	QFN (RUA)	TVSOP (DGV)					
ATMDS0-	33	40	I/O	Port A, channel 0, TMDS negative signal			
ATMDS0+	34	41	I/O	Port A, channel 0, TMDS positive signal			
ATMDS1-	35	43	I/O	Port A, channel 1, TMDS negative signal			
ATMDS1+	36	44	I/O	Port A, channel 1, TMDS positive signal			
ATMDS2-	37	45	I/O	Port A, channel 2, TMDS negative signal			
ATMDS2+	38	46	I/O	Port A, channel 2, TMDS positive signal			
ATMDSCLK-	31	38	I/O	Port A TMDS negative clock			
ATMDSCLK+	32	39	I/O	Port A TMDS positive clock			
BTMDS0-	24	29	I/O	Port B, channel 0, TMDS negative signal			
BTMDS0+	25	30	I/O	Port B, channel 0, TMDS positive signal			
BTMDS1-	26	32	I/O	Port B, channel 1, TMDS negative signal			
BTMDS1+	27	33	I/O	Port B, channel 1, TMDS positive signal			
BTMDS2-	28	34	I/O	Port B, channel 2, TMDS negative signal			
BTMDS2+	29	35	I/O	Port B, channel 2, TMDS positive signal			
BTMDSCLK-	22	27	I/O	Port B TMDS negative clock			
BTMDSCLK+	23	28	I/O	Port B TMDS positive clock			
SEL	9	13	I	Select pin to choose between port A or port B. Referenced to V_{SS}			
TMDS0-	12	16	I/O	TMDS channel 0 negative signal			
TMDS0+	11	15	I/O	TMDS channel 0 positive signal			
TMDS1-	7	10	I/O	TMDS channel 1 negative signal			
TMDS1+	6	9	I/O	TMDS channel 1 positive signal			
TMDS2-	4	7	I/O	TMDS channel 2 negative signal			
TMDS2+	3	6	I/O	TMDS channel 2 positive signal			
TMDSCLK-	15	19	I/O	TMDS negative clock			
TMDSCLK+	14	18	I/O	TMDS positive clock			
V _{DD}	2, 8, 16, 18, 20, 30, 40, 42	2, 4, 12, 21, 23, 25, 36, 48	Power	Positive power supply voltage			
V _{SS}	1, 5, 10, 13, 17, 19, 21, 39, 41	1, 3, 5, 8, 14, 17, 20, 22, 24, 26, 31, 37, 42, 47	Power	Negative power supply voltage			



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ABSOLUTE MINIMUM AND MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted), - All voltages are with respect to V_{SS}

			MIN	MAX	UNIT
V_{DD}	Supply voltage range	-0.5	2.5	V	
V_{IN}	Control input voltage range ⁽²⁾	-0.5	2.5	V	
V _{I/O}	Switch I/O voltage range ^{(2) (3)}	-0.5	2.5	V	
I _{IK}	Control input clamp current	V _{IN} < V _{SS}		50	mA
I _{I/OK}	I/O port clamp current		50	mA	
I _{I/O}	ON-state switch current ⁽⁴⁾		100	mA	
I _{DD}	Continuous current through V _{DD}			100	mA
I _{SS}	Continuous current through V _{SS}			100	mA
0	Declars thermal impedance (5)	DGV package		58.0	°C/W
θ_{JA}	Package thermal impedance ⁽⁵⁾	RUA package		51.2	C/vv
T _{stg}	Storage temperature range	-65	150	°C	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(3) V_I and V_O are used to denote specific conditions for $V_{I/O}$.

(4) I_I and I_O are used to denote specific conditions for $I_{I/O}$.

(5) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V	Supply voltage	$V_{SS} = GND$	1.5	1.8	2.1	V
V _{DD}	Supply voltage	V _{SS} = 1.5 V	3	3.3	3.6	v
V _{IH}	High-level input voltage	$3 \text{ V} < \text{V}_{\text{DD}} < 3.6 \text{ V}, \text{ V}_{\text{SS}} = 1.5 \text{ V}$	0.65(V _{DD} – V _{SS}) + V _{SS}			V
V _{IL}	Low-level input voltage	$1.5 \text{ V} < \text{V}_{\text{DD}} < 2.1 \text{ V}, \text{ V}_{\text{SS}} = 0 \text{ V}$			$\begin{array}{c} 0.35(V_{DD}-V_{SS})\\ + V_{SS} \end{array}$	V
V _{IO}	Switch input/output voltage		0		V _{DD}	V
T _A	Operating free-air temperature		0		85	°C

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ELECTRICAL CHARACTERISTICS FOR 1.8-V SUPPLY⁽¹⁾

 V_{DD} = 1.5 V to 2.1 V, V_{SS} = 0 V, T_A = -40°C to 85°C (unless otherwise noted)

PARA	METER		TEST CO	NDITIONS		MIN	TYP ⁽²⁾	MAX	UNIT
V _{IK}	SEL	$V_{DD} = 2.1 V,$	I _{IN} = -18 mA				-0.7	-1.2	V
IIH	SEL	V _{DD} = 2.1 V,	$V_{IN} = V_{DD}$					±1	μA
IIL	SEL	$V_{DD} = 2.1 V,$	$V_{IN} = V_{SS}$					±1	μA
I _{off}		$V_{DD} = 0,$	$V_0 = 0$ to 2.1 V,	V ₁ = 0				1	μA
I _{CC}		$V_{DD} = 2.1 V,$	$I_{I/O} = 0,$	Switch ON or OFF			230	450	μA
C _{IN}	SEL	f = 1 MHz,	$V_{IN} = 0$				0.7	1	pF
C _{OFF}	B port	$V_I = 0,$	f = 1 MHz,	Outputs open,	Switch OFF		1	1.5	pF
C _{ON}	·	$V_{I} = 0,$	f = 1 MHz,	Outputs open,	Switch ON		4	4.5	pF
r _{on}		V _{DD} = 1.8 V,	$V_{SS} \le V_I \le V_{DD},$	$I_0 = -40 \text{ mA}$			12.5	20	Ω
r _{on(flat)} (3	i)	V _{DD} = 1.8 V,	V _I = 1.65 V to 1.8 V	$I_O = -40 \text{ mA}$			0.5		Ω
Δr_{on} ⁽⁴⁾		V _{DD} = 1.8 V,	$V_{SS} \leq V_{I} \leq V_{DD},$	$I_O = -40 \text{ mA}$			-0.1	0.2	Ω
Dynami	c								
X _{TALK}		$R_L = 50 \Omega$,	f = 825 MHz	See Figure 7			-50		dB
O _{IRR}		$R_L = 50 \Omega$,	f = 825 MHz	See Figure 8			-50		dB
BW				See Figure 6			1.9		GHz
Max data	a rate			See Figure 6			3.8		Gbps

V₁, V₀, I₁, and I₀ refer to I/O pins. V_{IN} refers to the control inputs.
All typical values are at V_{DD} = 1.8 V (unless otherwise noted), T_A = 25°C.
r_{on(flat)} is the difference of r_{on} in a given channel at specified voltages.

(4) Δr_{on} is the difference of r_{on} from centerports to any other port.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{DD} = 1.5 V to 2.1 V, V_{SS} = 0 V, R_L = 200 Ω , C_L = 10 pF (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP ⁽¹⁾	МАХ	UNIT
t _{pd} ⁽²⁾	TMDSn or xTMDSn	xTMDSn or TMDSn		0.25		ns
t _{PZH} , t _{PZL}	SEL	TMDSn or xTMDSn	0.5		9	ns
t _{PHZ} , t _{PLZ}	SEL	TMDSn or xTMDSn	0.5		5	ns
t _{sk(o)} ⁽³⁾	TMDSn or xTMDSn	xTMDSn or TMDSn		0.06		ns
t _{sk(p)} ⁽⁴⁾				0.06	0.1	ns

(1)

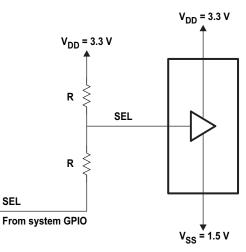
All typical values are at V_{DD} = 1.8 V (unless otherwise noted), T_A = 25°C. The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load (2) capacitance when driven by an ideal voltage source (zero output impedance).

Output skew between center port to any other port (3)

(4) Skew between opposite transitions of the same output in a given device $|t_{PHL} - t_{PLH}|$

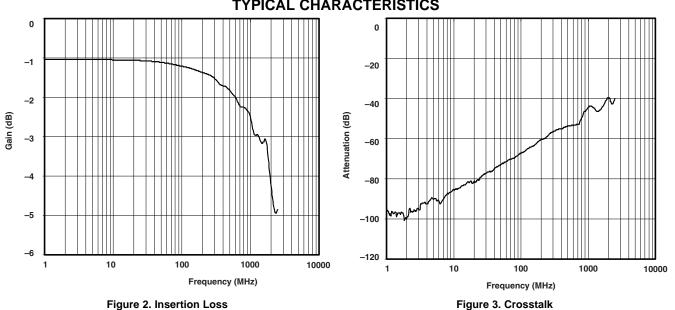


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This example circuit shows connecting control inputs to GPIOs of an application using V_{SS} = 1.5 V, which allows the device to pass TMDS signal levels





TYPICAL CHARACTERISTICS

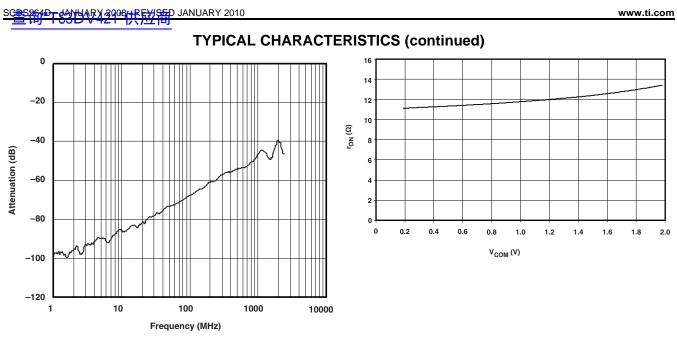


Figure 4. Off Isolation vs Frequency

Figure 5. r_{ON} vs V_{COM}

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PARAMETER MEASUREMENT INFORMATION

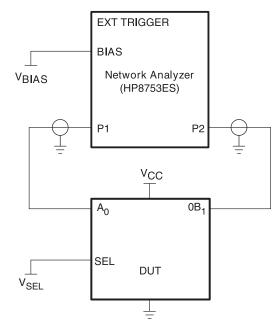


Figure 6. Test Circuit for Frequency Response (BW)

Frequency response is measured at the output of the ON channel. For example, when V_{SEL} is low and A_0 is the input, the output is measured at $0B_1$. All unused analog I/O ports are left open.

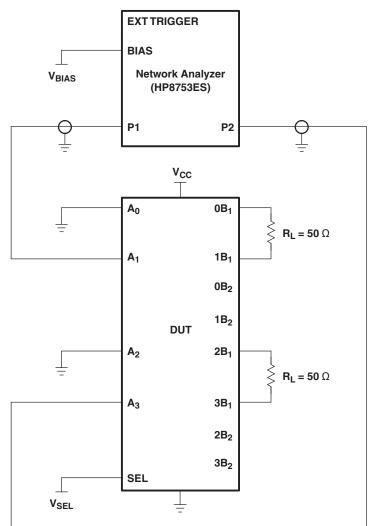
HP8753ES setup

Average = 4 RBW = 3 kHz $V_{BIAS} = 0.35 V$ ST = 2 s P1 = 0 dBM SCESEAPT CANHARY 2010

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PARAMETER MEASUREMENT INFORMATION (continued)

Figure 7. Test Circuit for Crosstalk (X_{TALK})

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when V_{SEL} is low and A_0 is the input, the output is measured at $1B_1$. All unused analog input (A) ports are connected to GND, and output (B) ports are connected to GND through $50-\Omega$ pulldown resistors.

HP8753ES setup

Average = 4

$$RBW = 3 kHz$$

 $V_{BIAS} = 0.35 V$

$$P1 = 0 \text{ dBM}$$



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PARAMETER MEASUREMENT INFORMATION (continued)

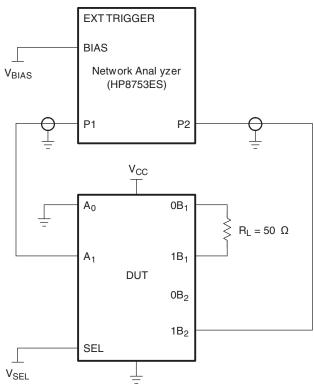


Figure 8. Test Circuit for OFF Isolation (OIRR)

OFF isolation is measured at the output of the OFF channel. For example, when V_{SEL} is low and A_0 is the input, the output is measured at $0B_2$. All unused analog input (A) ports are left open, and output (B) ports are connected to GND through $50-\Omega$ pulldown resistors.

HP8753ES setup

Average = 4 RBW = 3 kHz

 $V_{BIAS} = 0.35 V$

ST = 2

P1 = 0 dBM

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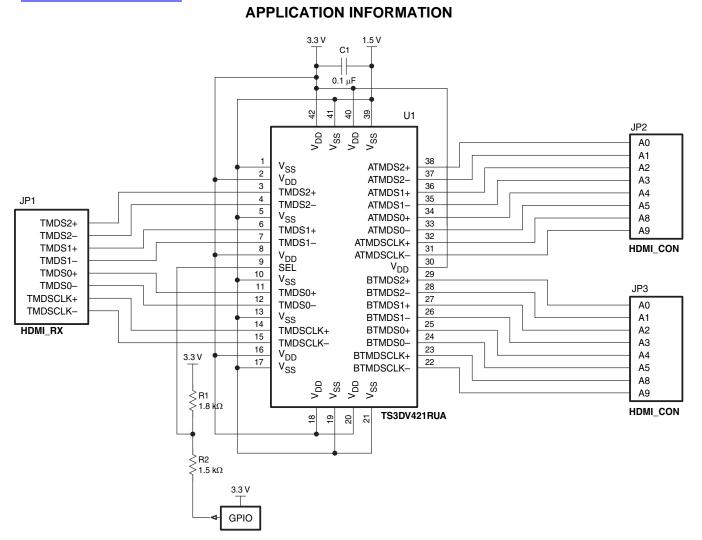


Figure 9. Reference Circuit for HDMI Application

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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Pe
TS3DV421DGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TS3DV421DGVRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TS3DV421RUAR	ACTIVE	WQFN	RUA	42	3000	TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www. information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retard in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

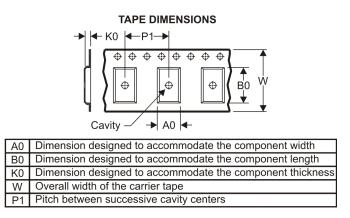
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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal	
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Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3DV421DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1



PACKAGE MATERIALS INFORMATION

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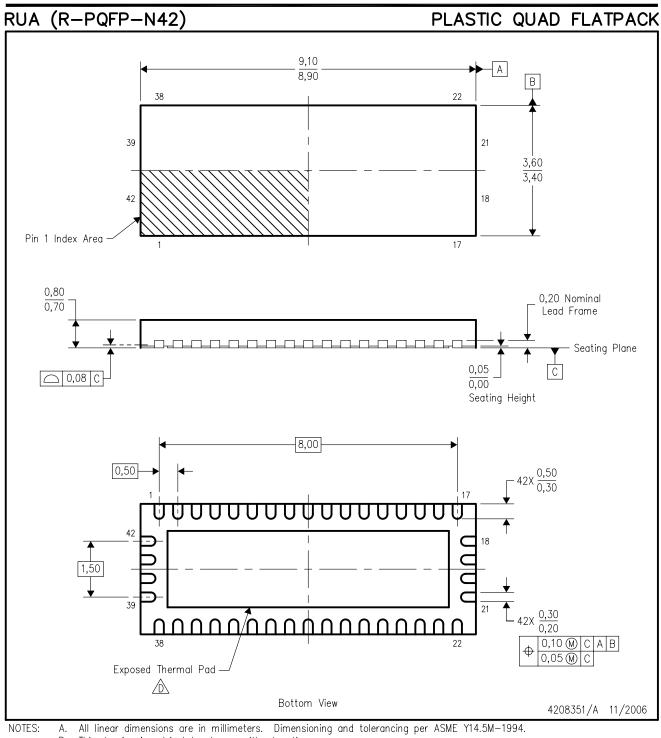


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3DV421DGVR	TVSOP	DGV	48	2000	346.0	346.0	33.0

MECHANICAL DATA

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- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.

The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.





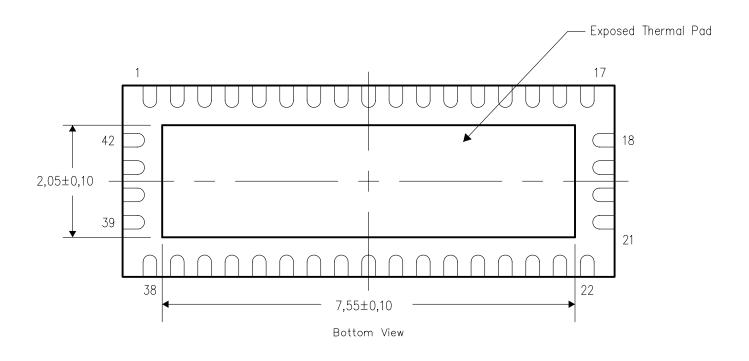
THERMAL PAD MECHANICAL DATA RUA (R-PQFP-N42)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



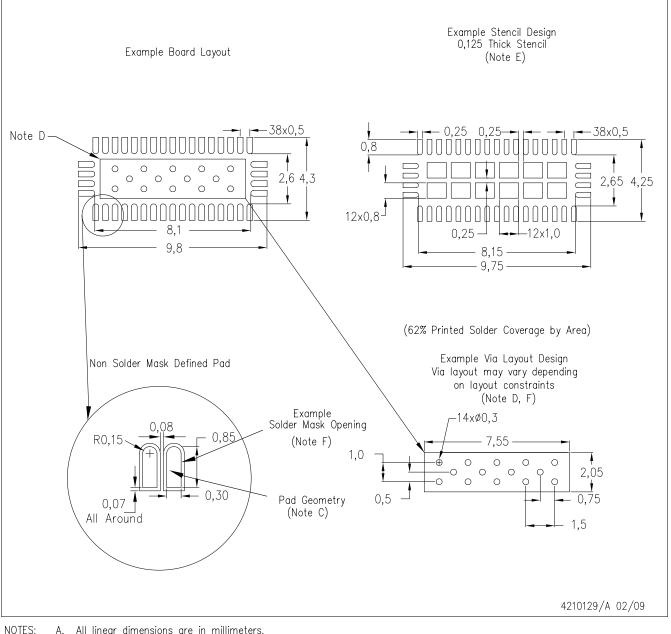
NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

LAND PATTERN

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RUA (R-PWQFN-N42)



All linear dimensions are in millimeters. Α.

- This drawing is subject to change without notice. Β.
- Publication IPC-7351 is recommended for alternate designs. C.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.



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