National Semiconductor

DM54S182/DM74S182 Look-Ahead Carry Generators

General Description

These circuits are high-speed, look-ahead carry generators, capable of anticipating a carry across four binary adders or groups of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin designation table.

When used in conjunction with the 181 arithmetic logic unit, these generators provide high-speed carry look-ahead capability for any word length. Each S182 generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

Carry input and output of the ALU's are in their true form, and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions, as explained on the 181 data sheet are also applicable to and compatible with the look-ahead generator. Positive logic equations for the S182 are:

$$C_{n+x} = \overline{G}0 + \overline{P}0\, C_n$$

$$C_{n+y} = \overline{G}1 + \overline{P}1\,\overline{G}0 + \overline{P}1\,\overline{P}0\, C_n$$

$$C_{n+z} = \overline{G}2 + \overline{P}2\,\overline{G}1 + \overline{P}2\,\overline{P}1\,\overline{G}0 + \overline{P}2\,\overline{P}1\,\overline{P}0\, C_n$$

$$\overline{G} = \overline{G}3\,(\overline{P}3 + \overline{G}2)\,(\overline{P}3 + \overline{P}2 + \overline{G}1)\,(\overline{P}3 + \overline{P}2 + \overline{P}1 + \overline{G}0)$$

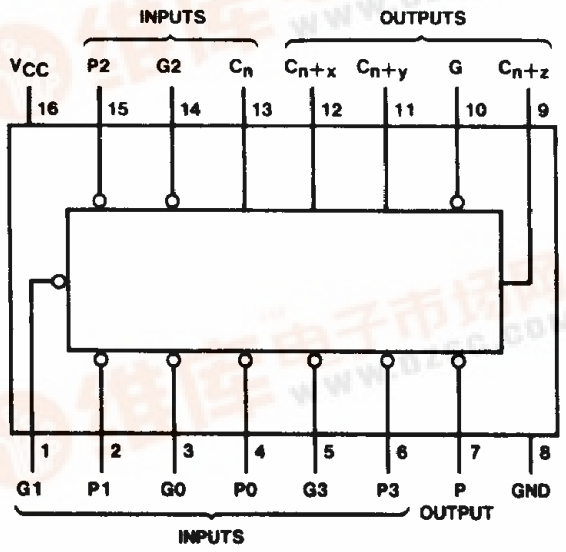
$$\overline{P} = \overline{P}3\,\overline{P}2\,\overline{P}1\,\overline{P}0$$

Features

- Typical propagation delay time 7 ns
- Typical power dissipation 260 mW

Connection Diagram

Dual-In-Line Package



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Order Number DM54S182J or DM74S182N
See NS Package Number J16A or N16E

Pin Designations

Designation	Pin Nos.	Function
G0, G1, G2, G3	3, 1, 14, 5	Active Low Carry Generate Inputs
P0, P1, P2, P3	4, 2, 15, 6	Active Low Carry Propagate Inputs
C_n	13	Carry Input
C_{n+x}, C_{n+y}, C_{n+z}	12, 11, 9	Carry Outputs
G	10	Active Low Carry Generate Output
P	7	Active Low Carry Propagate Output
V_{CC}	16	Supply Voltage
GND	8	Ground

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S182			DM74S182			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	P0, P1 or G3			200	μA
			P3			100	
			P2			150	
			C_n			50	
			G0, G2			350	
			G1			400	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	P0, P1 or G3			−8	mA
			P3			−4	
			P2			−6	
			C_n			−2	
			G0, G2			−14	
			G1			−16	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)	DM54		39	55	mA
			DM74		39	55	
I_{CCL}	Supply Currents with Outputs Low	V_{CC} = Max (Note 4)	DM54		69	99	mA
			DM74		69	109	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

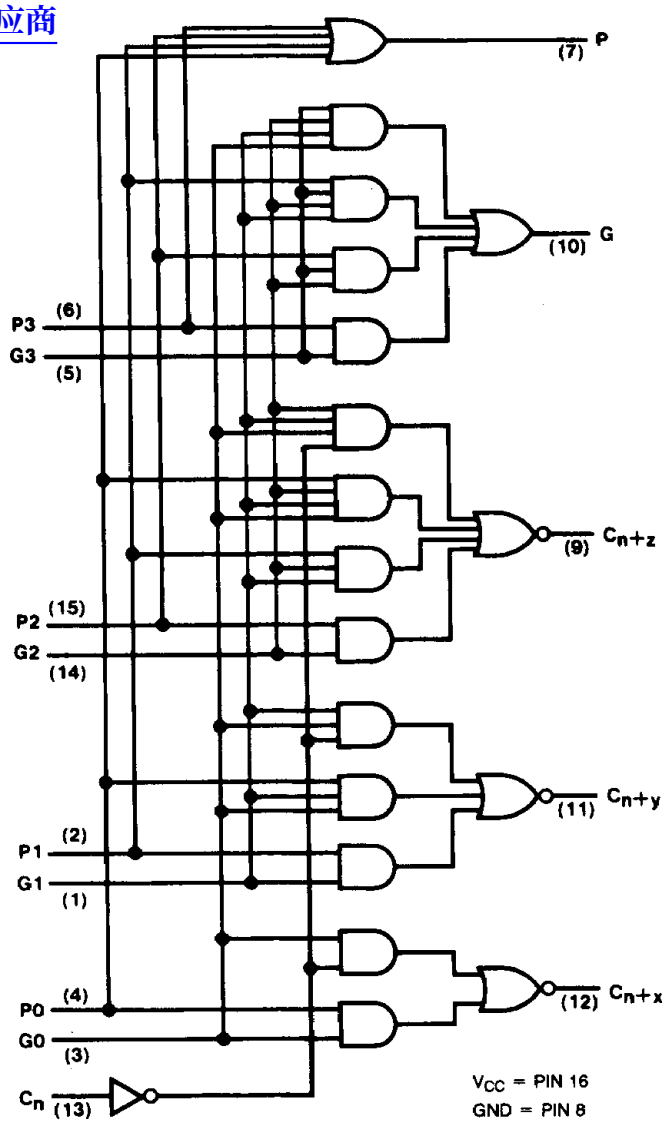
Note 3: I_{CCH} is measured with all outputs open, inputs P3 and G3 at 4.5V, and all other inputs grounded.

Note 4: I_{CCL} is measured with all outputs open, inputs G0, G1, and G2 at 4.5V, and all other inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Min	
t_{PLH}	Propagation Delay Time Low to High Level Output	GN or PN to C_n + x, y, z		7		10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	GN or PN to C_n + x, y, z		7		11	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	GN or PN to G		7.5		11	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	GN or PN to G		10.5		14	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	PN to P		6.5		10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	PN to P		10		14	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C_n to to C_n + x, y, z		10		13	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C_n to to C_n + x, y, z		10.5		14	ns

Logic Diagram



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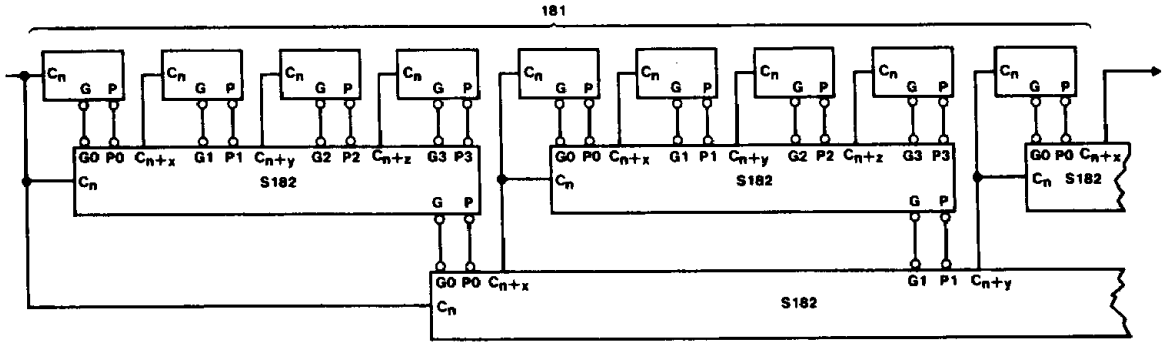
Typical Application

64-Bit ALU, Full-Carry Look Ahead in Three Levels



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A and B inputs, and F outputs of 181 are not shown.