

## 250mA, Ultralow $I_Q$ , Fast Transient Response, RF LOW-DROPOUT LINEAR REGULATOR

### FEATURES

- **Very Low Dropout:**
  - 65mV Typical at 100mA
  - 130mV Typical at 200mA
  - 163mV Typical at 250mA
- **2% Accuracy Over Load/Line/Temperature**
- **Ultralow  $I_Q$ : 7.9 $\mu$ A**
- **Excellent Load Transient Performance:  $\pm 50$ mV for 200mA Loading/Unloading Transient**
- **Available in Fixed-Output Voltages From 0.9V to 5V Using Innovative Factory EEPROM Programming**
- **High PSRR: 70dB at 1kHz**
- **Stable with a 1.0 $\mu$ F Ceramic Capacitor**
- **Thermal Shutdown and Overcurrent Protection**
- **Available in 4-Ball, 0.4mm Pitch Wafer-Level Chip Scale and 1.5mm x 1.5mm SON Packages**

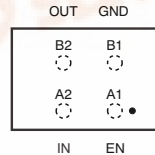
### APPLICATIONS

- **Wireless Handsets, Smart Phones, PDAs**
- **MP3 Players and Other Handheld Products**
- **Wireless LAN, Bluetooth®, Zigbee®**
- **Remote Controls**
- **Portable Consumer Products**

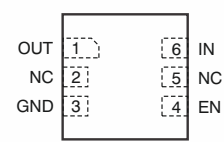
### DESCRIPTION

The TPS727xx family of low-dropout (LDO) linear regulators are ultralow quiescent current LDOs with excellent line and ultra-fast load transient performance and are designed for power-sensitive applications. The LDO output voltage level is preset by the use of innovative factory EEPROM programming. A precision bandgap and error amplifier provides overall 2% accuracy over load, line, and temperature extremes. The TPS727xx family is available in 1.5mm x 1.5mm SON and wafer chip-scale (WCSP) packages that make it ideal for handheld applications. This family of devices is fully specified over a temperature range of  $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

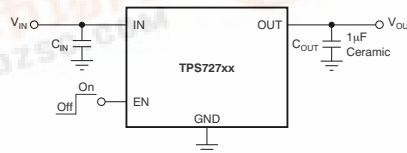
**YFF PACKAGE  
WCSP-4  
(Top View)**



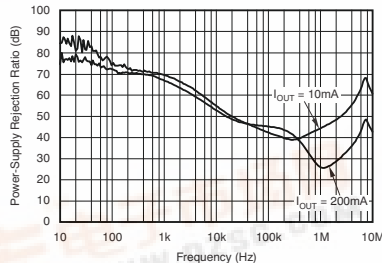
**DSE PACKAGE  
1.5mm x 1.5mm SON-6  
(Top View)**



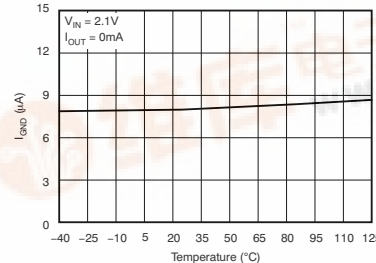
**TYPICAL APPLICATION CIRCUIT**



**PSRR vs FREQUENCY**



**GROUND PIN CURRENT vs TEMPERATURE**



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	V <sub>OUT</sub> <sup>(2)</sup>
TPS727xxx yyy z	<b>XXX</b> is the nominal output voltage. <b>YYY</b> is package designator. <b>Z</b> is package tape and reel quantity (R = 3000, T = 250).

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at [www.ti.com](http://www.ti.com).
- (2) Output voltages from 0.9V to 5.0V in 50mV increments are available through the use of innovative factory EEPROM programming; minimum order quantities may apply. Contact factory for details and availability.

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

At T<sub>J</sub> = –40°C to +125°C (unless otherwise noted). All voltages are with respect to GND.

PARAMETER	TPS727xx	UNIT
Input voltage range, V <sub>IN</sub>	–0.3 to +6.0	V
Enable voltage range, V <sub>EN</sub>	–0.3 to +6.0 <sup>(2)</sup>	V
Output voltage range, V <sub>OUT</sub>	–0.3 to +6.0	V
Maximum output current, I <sub>OUT</sub>	Internally limited	
Output short-circuit duration	Indefinite	
Total continuous power dissipation, P <sub>DISS</sub>	See <a href="#">Dissipation Ratings</a> Table	
ESD rating	Human body model (HBM)	2 kV
	Charged device model (CDM)	500 V
Operating junction temperature range, T <sub>J</sub>	–55 to +150	°C
Storage temperature range, T <sub>STG</sub>	–55 to +150	°C

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) V<sub>EN</sub> absolute maximum rating is V<sub>IN</sub> or 6.0V, whichever is less.

### DISSIPATION RATINGS

BOARD	PACKAGE	R <sub>θJC</sub>	R <sub>θJA</sub>	DERATING FACTOR ABOVE T <sub>A</sub> = +25°C	T <sub>A</sub> < +25°C	T <sub>A</sub> = +70°C	T <sub>A</sub> = +85°C
High-K <sup>(1)</sup>	DSE	—	206°C/W	4.85mW/°C	485mW	269mW	194mW
High-K <sup>(1)</sup>	YFF	85°C/W	268°C/W	3.7mW/°C	370mW	205mW	150mW

- (1) The JEDEC high-K (2s2p) board used to derive this data was a 3-inch × 3-inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

## ELECTRICAL CHARACTERISTICS

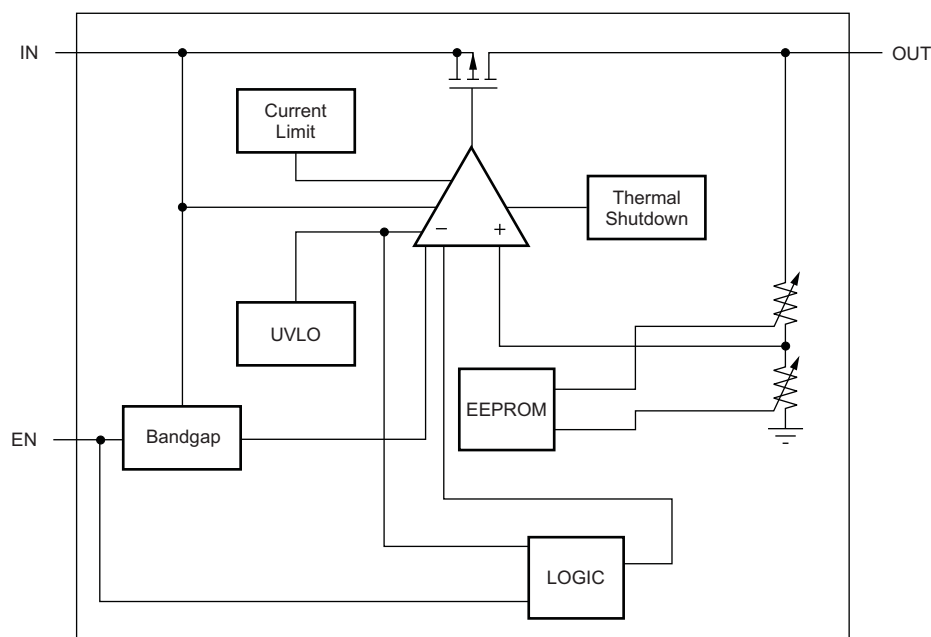
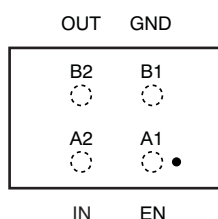
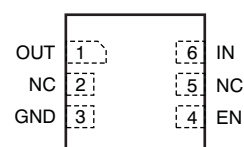
Over operating temperature range ( $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ),  $V_{IN} = V_{OUT(TYP)} + 0.3\text{V}$  or  $2.0\text{V}$ , whichever is greater;  
 $I_{OUT} = 10\text{mA}$ ,  $V_{EN} = 0.9\text{V}$ , and  $C_{OUT} = 1.0\mu\text{F}$ , unless otherwise noted. Typical values are at  $T_J = +25^{\circ}\text{C}$ .

PARAMETER		TEST CONDITIONS	TPS727xx			UNIT
			MIN	TYP	MAX	
$V_{IN}$	Input voltage range		2.0		5.5	V
$V_O$	Output voltage range		0.9		5.0	V
$V_{OUT}^{(1)}$	DC output accuracy	$T_J = +25^{\circ}\text{C}$	-2.5		+2.5	mV
		$V_{OUT} + 0.3\text{V} \leq V_{IN} \leq 5.5\text{V}$ , $0\text{mA} \leq I_{OUT} \leq 200\text{mA}$	-2.0	$\pm 1.0$	+2.0	%
		$V_{OUT} + 0.3\text{V} \leq V_{IN} \leq 5.5\text{V}$ , $0\text{mA} \leq I_{OUT} \leq 250\text{mA}$		$\pm 1.0$		%
$\Delta V_{OUT}$	Load transient	1mA to 200mA or 200mA to 1mA in $1\mu\text{s}$ , $C_{OUT} = 1\mu\text{F}$		$\pm 50.0$		mV
		1mA to 250mA or 250mA to 1mA in $1\mu\text{s}$ , $C_{OUT} = 1\mu\text{F}$		$\pm 65$		mV
$\Delta V_O/\Delta V_{IN}$	Line regulation	$V_{OUT(NOM)} + 0.3\text{V} \leq V_{IN} \leq 5.5\text{V}$ , $I_{OUT} = 10\text{mA}$		8		$\mu\text{V/V}$
$\Delta V_O/\Delta I_{OUT}$	Load regulation	$0\text{mA} \leq I_{OUT} \leq 250\text{mA}$		20		$\mu\text{V/mA}$
$V_{DO}$	Dropout voltage <sup>(2)</sup>	$V_{IN} = 0.98 \times V_{OUT(NOM)}$ , $I_{OUT} = 10\text{mA}$		6.5		mV
		$V_{IN} = 0.98 \times V_{OUT(NOM)}$ , $I_{OUT} = 50\text{mA}$		32.5		mV
		$V_{IN} = 0.98 \times V_{OUT(NOM)}$ , $I_{OUT} = 100\text{mA}$		65		mV
		$V_{IN} = 0.98 \times V_{OUT(NOM)}$ , $I_{OUT} = 200\text{mA}$		130	200	mV
		$V_{IN} = 0.98 \times V_{OUT(NOM)}$ , $I_{OUT} = 250\text{mA}$		162.5		mV
$I_{CL}$	Output current limit	$V_{OUT} = 0.9 \times V_{OUT(NOM)}$	300	400	550	mA
$I_{GND}$	Ground pin current	$I_{OUT} = 0\text{mA}$ , $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$		7.9	12	$\mu\text{A}$
		$I_{OUT} = 200\text{mA}$		110		$\mu\text{A}$
		$I_{OUT} = 250\text{mA}$		130		$\mu\text{A}$
$I_{SHDN}$	Shutdown current ( $I_{GND}$ )	$V_{EN} \leq 0.4\text{V}$ , $V_{IN} = 2\text{V}$ , $T_J = +25^{\circ}\text{C}$		0.12		$\mu\text{A}$
		$V_{EN} \leq 0.4\text{V}$ , $2.0\text{V} < V_{IN} \leq 4.5\text{V}$ , $T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		0.55	2	$\mu\text{A}$
PSRR	Power-supply rejection ratio	$V_{IN} = 2.3\text{V}$ , $V_{OUT} = 1.8\text{V}$ , $I_{OUT} = 10\text{mA}$	$f = 10\text{Hz}$	85		dB
			$f = 100\text{Hz}$	75		dB
			$f = 1\text{kHz}$	70		dB
			$f = 10\text{kHz}$	55		dB
			$f = 100\text{kHz}$	40		dB
			$f = 1\text{MHz}$	45		dB
$V_N$	Output noise voltage	$\text{BW} = 100\text{Hz}$ to $100\text{kHz}$ , $V_{IN} = 2.1\text{V}$ , $V_{OUT} = 1.8\text{V}$ , $I_{OUT} = 10\text{mA}$		33.5		$\mu\text{V}_{\text{RMS}}$
$t_{STR}$	Startup time <sup>(3)</sup>	$C_{OUT} = 1.0\mu\text{F}$ , $0 \leq I_{OUT} \leq 250\text{mA}$		100		$\mu\text{s}$
$V_{HI}$	Enable pin high (enabled)		0.9		$V_{IN}$	V
$V_{LO}$	Enable pin low (disabled)		0		0.4	V
$I_{EN}$	Enable pin current	$EN = 5.5\text{V}$		40	500	nA
UVLO	Undervoltage lock-out	$V_{IN}$ rising	1.85	1.90	1.95	V
$T_{SD}$	Thermal shutdown temperature	Shutdown, temperature increasing		+160		$^{\circ}\text{C}$
		Reset, temperature decreasing		+140		$^{\circ}\text{C}$
$T_J$	Operating junction temperature		-40		+125	$^{\circ}\text{C}$

(1) The output voltage is programmed at the factory.

(2)  $V_{DO}$  is measured for devices with  $V_{OUT(NOM)} \geq 2.35\text{V}$  so that  $V_{IN} \geq 2.3\text{V}$ .

(3) Startup time: Time from EN assertion to  $0.98 \times V_{OUT(NOM)}$ .

**DEVICE INFORMATION****Figure 1. Functional Block Diagram****PIN CONFIGURATIONS****YFF PACKAGE  
WCSP-4  
(TOP VIEW)****DSE PACKAGE  
1,5mm x 1,5mm SON-6  
(TOP VIEW)**

Note: EN pin marked with dot on YFF package.

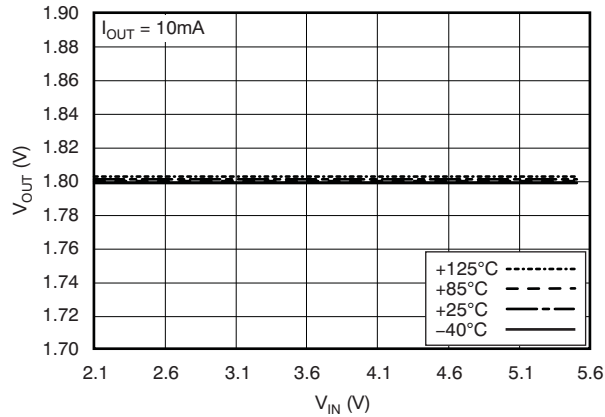
**PIN DESCRIPTIONS**

TPS727xx			DESCRIPTION
NAME	YFF	DSE	
OUT	B2	1	Regulated output voltage pin. A small 1µF ceramic capacitor is needed from this pin to ground to assure stability. See <a href="#">Input and Output Capacitor Requirements</a> in the <i>Application Information</i> section for more details.
NC	—	2	No connection. This pin can be tied to ground to improve thermal dissipation.
GND	B1	3	Ground pin.
EN	A1	4	Enable pin. Driving EN over 0.9V turns on the regulator. Driving EN below 0.4V puts the regulator into shutdown mode, thus reducing the operating current to 120nA, nominal.
NC	—	5	No connection. This pin can be tied to ground to improve thermal dissipation.
IN	A2	6	Input pin. A small capacitor is needed from this pin to ground to assure stability. See <a href="#">Input and Output Capacitor Requirements</a> in the <i>Application Information</i> section for more details.

## TYPICAL CHARACTERISTICS

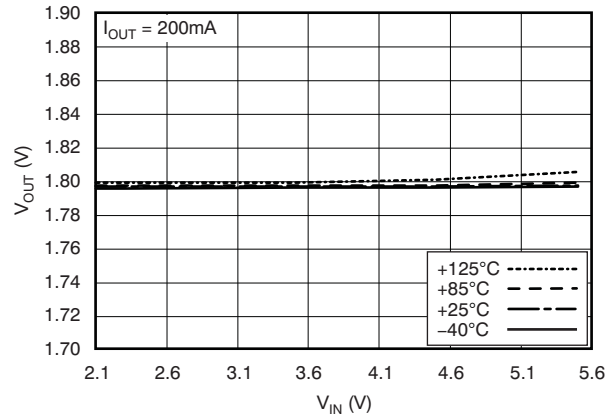
Over operating temperature range ( $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ),  $V_{IN} = V_{OUT(TYP)} + 0.3\text{V}$  or  $2.0\text{V}$ , whichever is greater;  $I_{OUT} = 10\text{mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{OUT} = 1.0\mu\text{F}$ , unless otherwise noted. Typical values are at  $T_J = +25^\circ\text{C}$ .

**LINE REGULATION  
(TPS72718)**



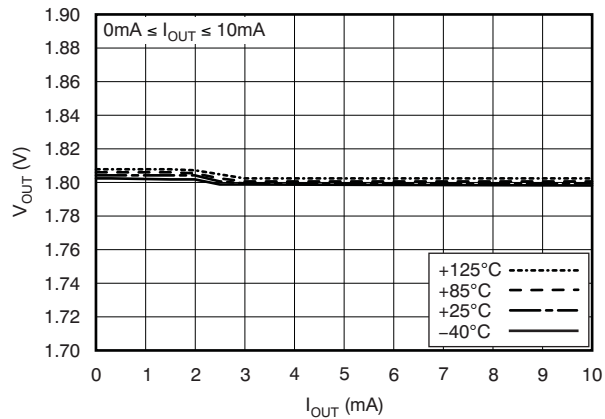
**Figure 2.**

**LINE REGULATION  
(TPS72718)**



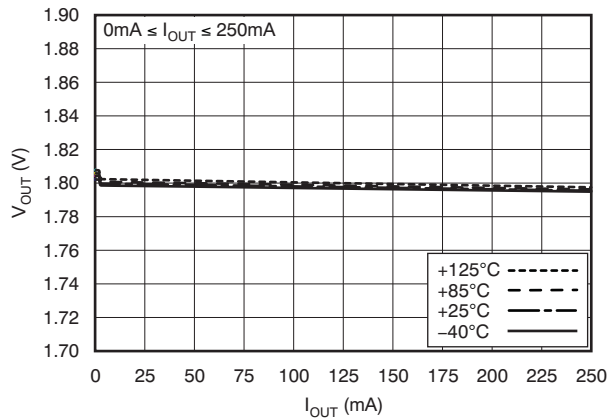
**Figure 3.**

**LOAD REGULATION UNDER LIGHT LOADS  
(TPS72718)**



**Figure 4.**

**LOAD REGULATION  
(TPS72718)**



**Figure 5.**

## TYPICAL CHARACTERISTICS (continued)

Over operating temperature range ( $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ),  $V_{IN} = V_{OUT(TYP)} + 0.3\text{V}$  or  $2.0\text{V}$ , whichever is greater;  $I_{OUT} = 10\text{mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{OUT} = 1.0\mu\text{F}$ , unless otherwise noted. Typical values are at  $T_J = +25^\circ\text{C}$ .

**DROPOUT VOLTAGE vs OUTPUT CURRENT  
(TPS72750)**

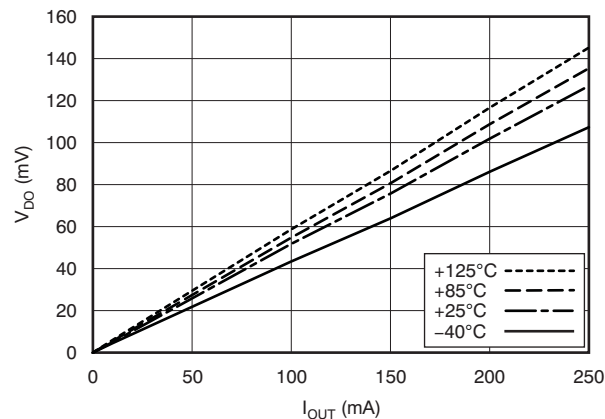


Figure 6.

**DROPOUT VOLTAGE vs INPUT VOLTAGE  
(TPS72750)**

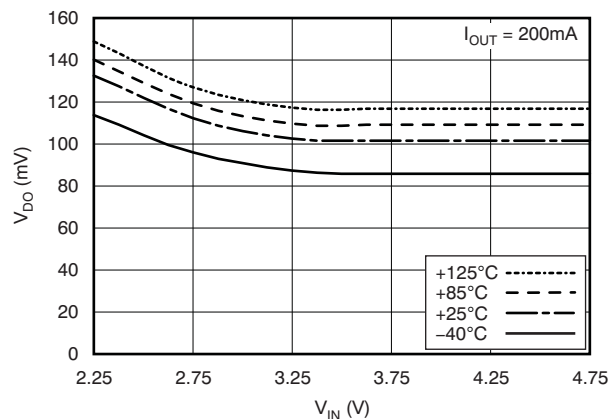


Figure 7.

**OUTPUT VOLTAGE vs TEMPERATURE  
(TPS72718)**

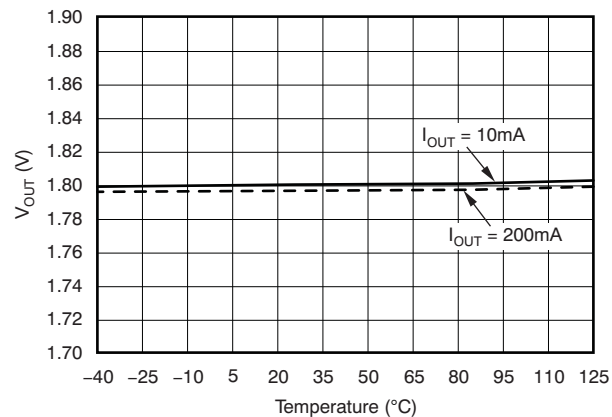


Figure 8.

**GROUND PIN CURRENT vs INPUT VOLTAGE  
(TPS72718)**

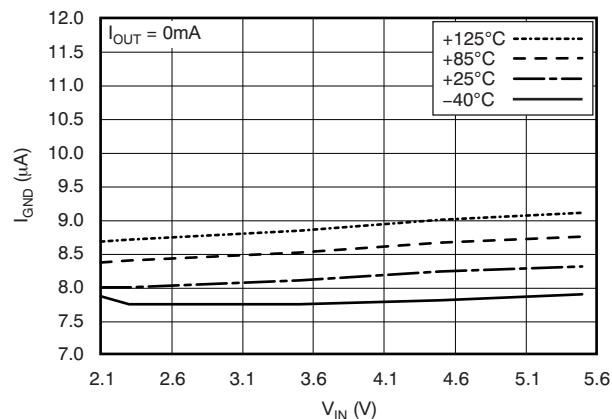


Figure 9.

## TYPICAL CHARACTERISTICS (continued)

Over operating temperature range ( $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ),  $V_{IN} = V_{OUT(TYP)} + 0.3\text{V}$  or  $2.0\text{V}$ , whichever is greater;  $I_{OUT} = 10\text{mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{OUT} = 1.0\mu\text{F}$ , unless otherwise noted. Typical values are at  $T_J = +25^{\circ}\text{C}$ .

**GROUND PIN CURRENT vs LOAD  
(TPS72718)**

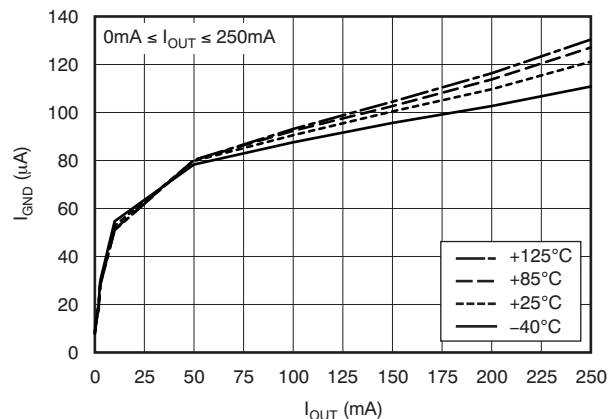


Figure 10.

**GROUND PIN CURRENT vs TEMPERATURE  
(TPS72718)**

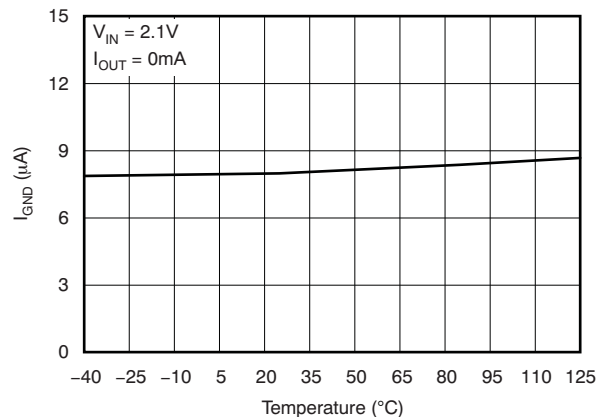


Figure 11.

**SHUTDOWN CURRENT vs INPUT VOLTAGE  
(TPS72718)**

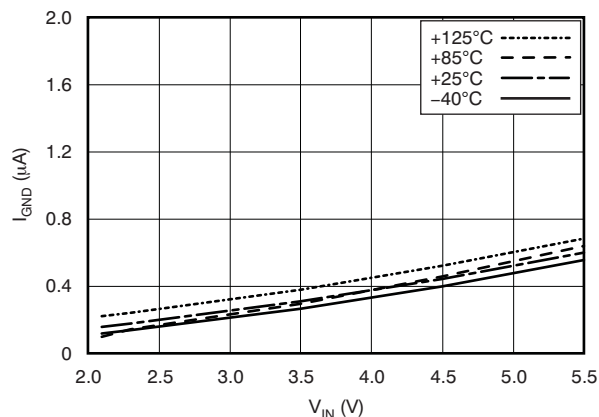


Figure 12.

**CURRENT LIMIT vs INPUT VOLTAGE  
(TPS72718)**

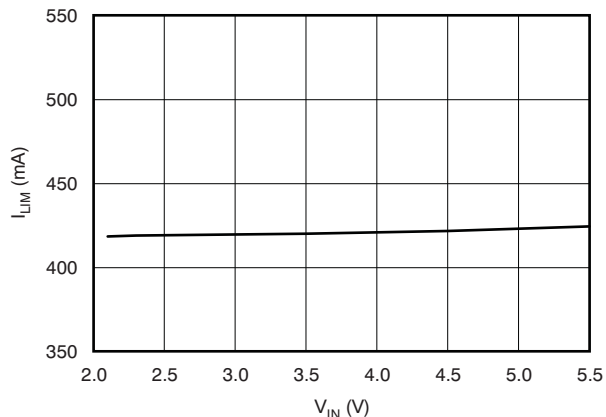


Figure 13.

## TYPICAL CHARACTERISTICS (continued)

Over operating temperature range ( $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ),  $V_{IN} = V_{OUT(TYP)} + 0.3\text{V}$  or  $2.0\text{V}$ , whichever is greater;  $I_{OUT} = 10\text{mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{OUT} = 1.0\mu\text{F}$ , unless otherwise noted. Typical values are at  $T_J = +25^{\circ}\text{C}$ .

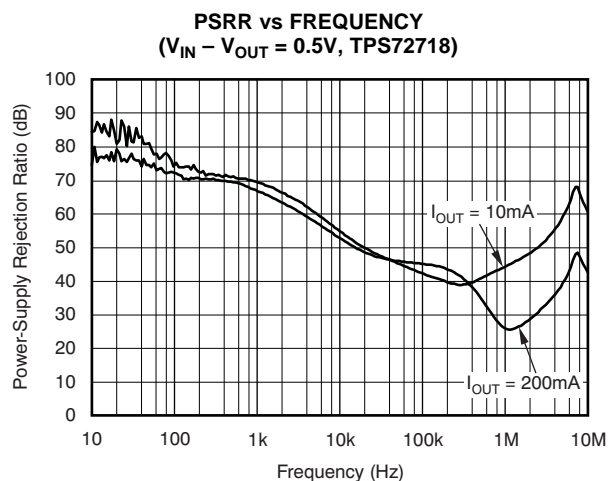


Figure 14.

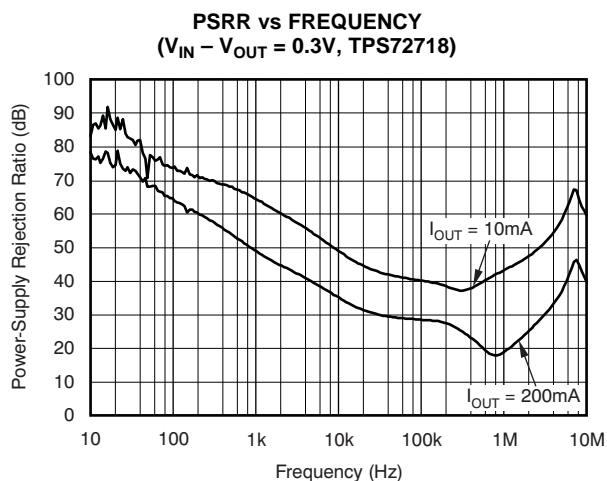


Figure 15.

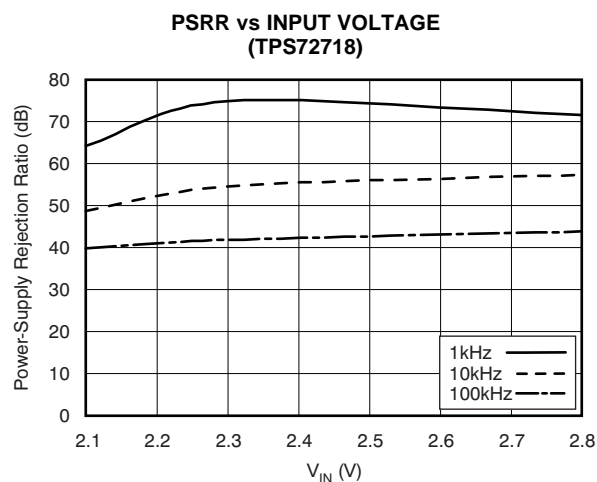


Figure 16.

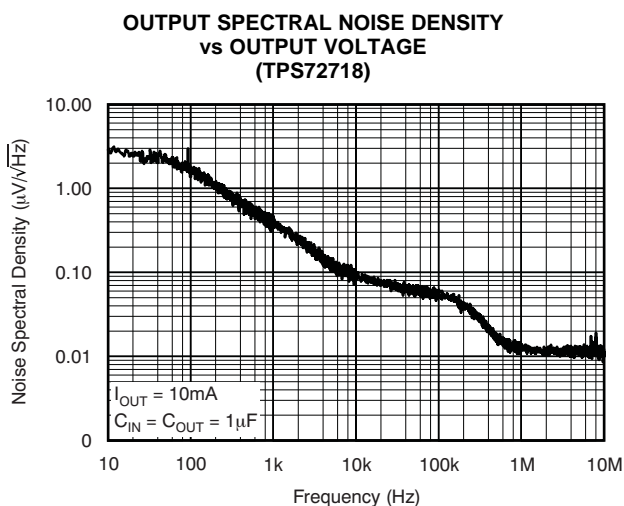


Figure 17.

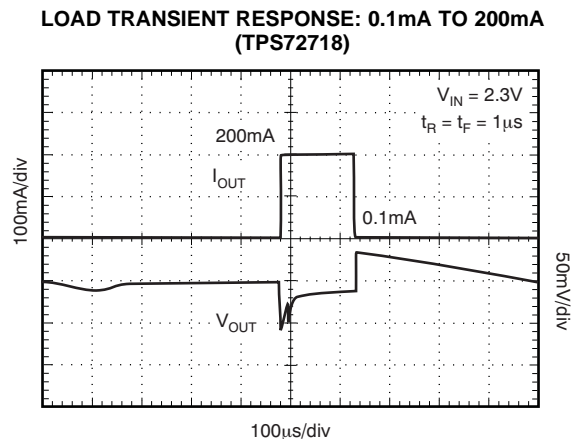


Figure 18.

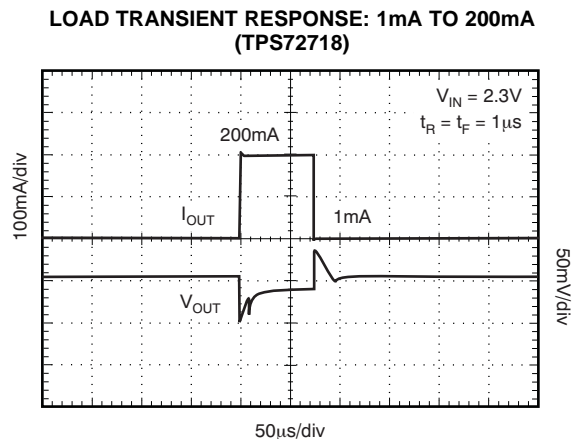


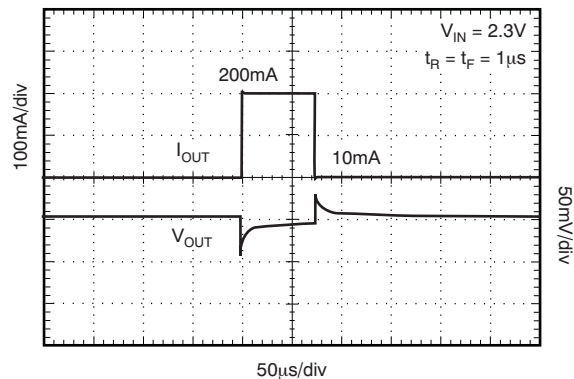
Figure 19.



## TYPICAL CHARACTERISTICS (continued)

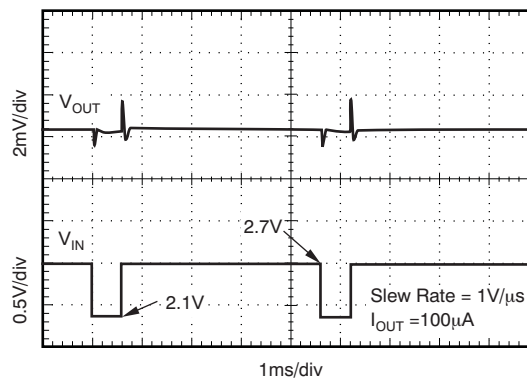
Over operating temperature range ( $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ),  $V_{IN} = V_{OUT(TYP)} + 0.3\text{V}$  or  $2.0\text{V}$ , whichever is greater;  $I_{OUT} = 10\text{mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{OUT} = 1.0\mu\text{F}$ , unless otherwise noted. Typical values are at  $T_J = +25^{\circ}\text{C}$ .

**LOAD TRANSIENT RESPONSE: 10mA TO 200mA  
(TPS72718)**



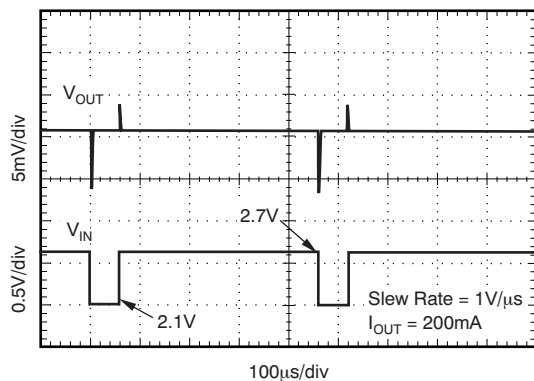
**Figure 20.**

**LINE TRANSIENT RESPONSE  
(TPS72718)**



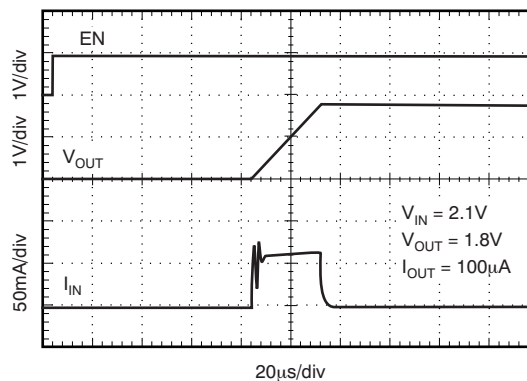
**Figure 21.**

**LINE TRANSIENT RESPONSE  
(TPS72718)**



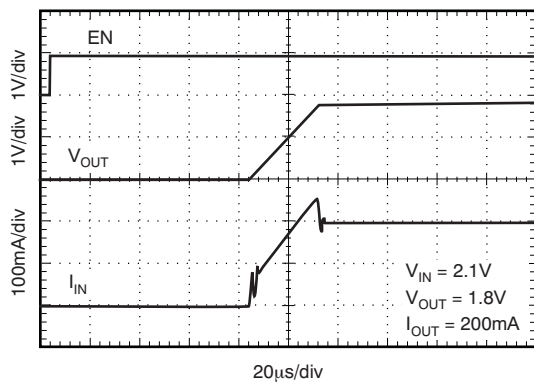
**Figure 22.**

**V\_IN INRUSH CURRENT  
(TPS72718)**



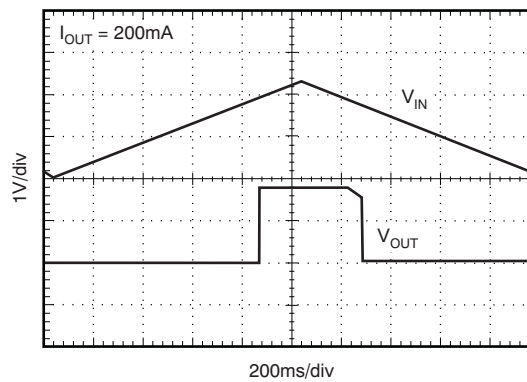
**Figure 23.**

**V\_IN INRUSH CURRENT  
(TPS72718)**



**Figure 24.**

**V\_IN RAMP UP,  
RAMP DOWN RESPONSE (TPS72718)**



**Figure 25.**

## APPLICATION INFORMATION

The TPS727xx family belongs to a family of new generation LDO regulators that consume extremely low quiescent current while simultaneously delivering excellent PSRR with very little headroom ( $V_{IN} - V_{OUT}$  differential voltage), and very good transient response. These features, combined with low noise without a noise reduction pin in an ultrasmall package, make this device ideal for portable applications. This family of regulators offers sub-bandgap output voltages, current limit and thermal protection, and is fully specified from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

### INPUT AND OUTPUT CAPACITOR REQUIREMENTS

Although an input capacitor is not required for stability, it is good analog design practice to connect a  $0.1\mu\text{F}$  to  $1.0\mu\text{F}$  low equivalent series resistance (ESR) capacitor across the IN pin and GND input of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source. If source impedance is not sufficiently low, a  $0.1\mu\text{F}$  input capacitor may be necessary to ensure stability.

The TPS727xx is designed to be stable with standard ceramic capacitors with values of  $1.0\mu\text{F}$  or larger at the output. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be less than  $200\text{m}\Omega$ .

### BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for  $V_{IN}$  and  $V_{OUT}$ , with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device. High ESR capacitors may degrade PSRR.

### INTERNAL CURRENT LIMIT

The TPS727xx internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. In such a case, the output voltage is not regulated, and is  $V_{OUT} =$

$I_{LIMIT} \times R_{LOAD}$ . The PMOS pass transistor dissipates  $(V_{IN} - V_{OUT}) \times I_{LIMIT}$  until thermal shutdown is triggered and the device is turned off. As the device cools down, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown. See the [Thermal Information](#) section for more details.

The PMOS pass element in the TPS727xx has a built-in body diode that conducts current when the voltage at the OUT pin exceeds the voltage at the IN pin. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of rated output current is recommended.

### SOFT START

The startup current is given by [Equation 1](#):

$$I_{SOFT\ START} (\text{mA}) = C_{OUT} (\mu\text{F}) \times 0.07 (\text{V}/\mu\text{s}) + I_{LOAD} (\text{mA}) \quad (1)$$

This equation shows that soft-start current is directly proportional to  $C_{OUT}$ .

The output voltage ramp rate is independent of  $C_{OUT}$  and load current, and has a typical value of  $0.07\text{V}/\mu\text{s}$ .

The TPS727xx automatically adjusts the soft-start current to supply both the load current and the  $C_{OUT}$  charge current. For example, if  $I_{LOAD} = 0\text{mA}$  upon enabling the LDO,  $I_{SOFT\ START} = 1\mu\text{F} \times 0.07\text{V}/\mu\text{s} + 0\text{mA} = 70\text{mA}$ , the current that charges the output capacitor.

If  $I_{LOAD} = 200\text{mA}$ ,  $I_{SOFT\ START} = 1\mu\text{F} \times 0.07\text{V}/\mu\text{s} + 200\text{mA} = 270\text{mA}$ , the current required for charging output capacitor and supplying the load current.

If the output capacitor and load are increased such that the soft-start current exceeds the output current limit, it is clamped at the typical current limit of  $400\text{mA}$ . For example, if  $C_{OUT} = 10\mu\text{F}$  and  $I_{OUT} = 200\text{mA}$ ,  $10\mu\text{F} \times 0.07\text{V}/\mu\text{s} + 200\text{mA} = 900\text{mA}$  is not supplied. Instead, it is clamped at  $400\text{mA}$ .

### SHUTDOWN

The enable pin (EN) is active high and is compatible with standard and low voltage, TTL-CMOS levels. When shutdown capability is not required, EN can be connected to the IN pin.

## DROPOUT VOLTAGE

The TPS727xx uses a PMOS pass transistor to achieve low dropout. When  $(V_{IN} - V_{OUT})$  is less than the dropout voltage ( $V_{DO}$ ), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the  $R_{DS(ON)}$  of the PMOS pass element.  $V_{DO}$  approximately scales with output current because the PMOS device behaves like a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as  $(V_{IN} - V_{OUT})$  approaches dropout. This effect is shown in [Figure 16](#) in the Typical Characteristics section.

## TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response.

## UNDERVOLTAGE LOCK-OUT (UVLO)

The TPS727xx uses an undervoltage lock-out circuit that keeps the output shut off until the input voltage reaches the UVLO threshold voltage.

## THERMAL INFORMATION

### Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design

(including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS727xx has been designed to protect against overload conditions. It is not intended to replace proper heatsinking. Continuously running the TPS727xx into thermal shutdown degrades device reliability.

### Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the [Dissipation Ratings](#) table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

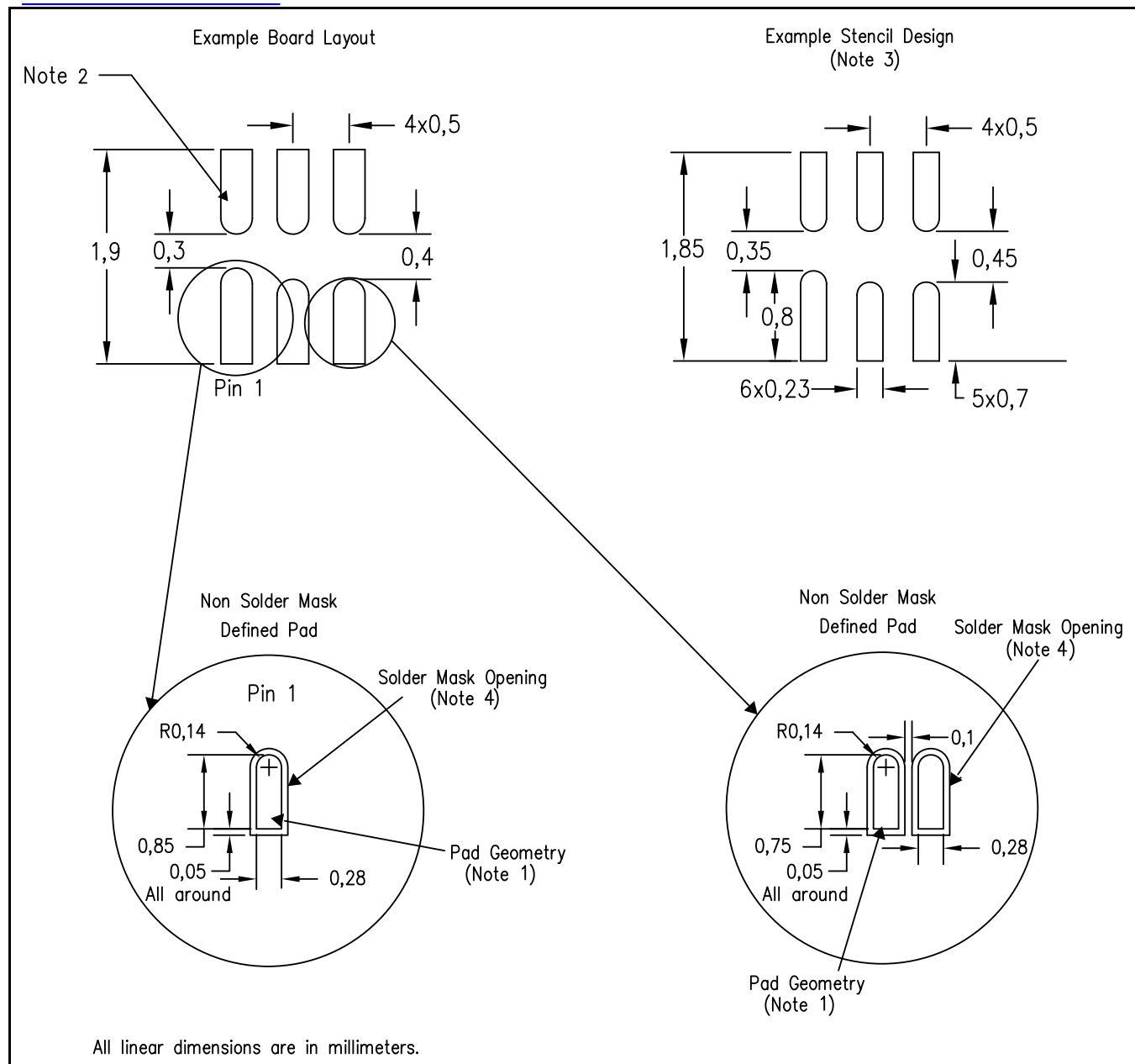
Power dissipation depends on input voltage and load conditions. Power dissipation ( $P_D$ ) is equal to the product of the output current times the voltage drop across the output pass element ( $V_{IN}$  to  $V_{OUT}$ ), as shown in [Equation 2](#):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

### Package Mounting

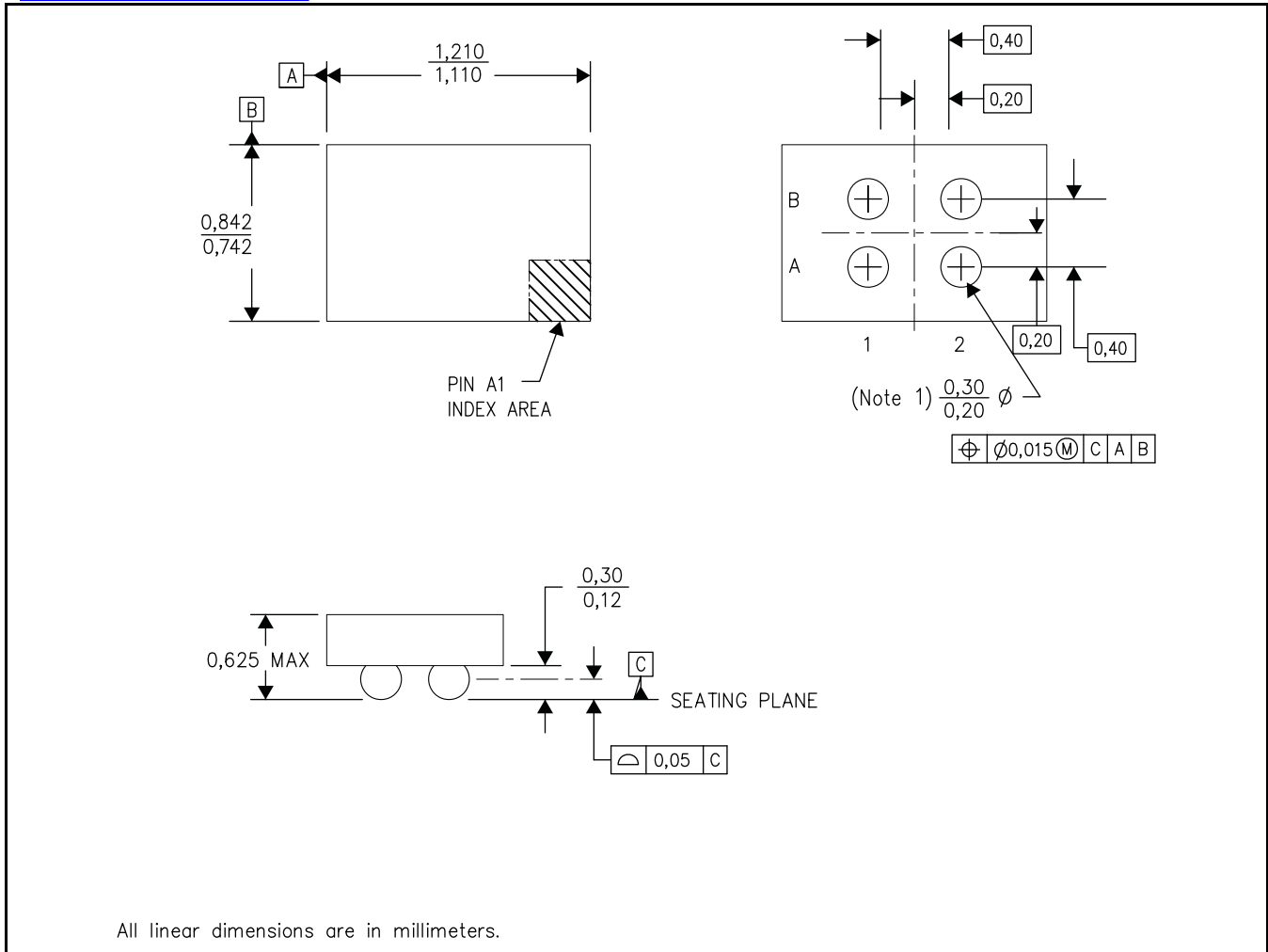
Solder pad footprint recommendations for the TPS727xx are available from the Texas Instruments web site at [www.ti.com](http://www.ti.com).

The recommended land pattern for the DSE package is shown in [Figure 26](#). [Figure 27](#) shows the dimensions of the YFF package.



- (1) Publication IPC-7351 is recommended for alternate designs.
- (2) For more information, refer to TI application notes [SCBA017](#) and [SLUA271](#) (*Quad Flatpack No-Lead Logic Packages* and *QFN/SON PCB Attachment*, respectively) for specific thermal information, via requirements, and additional recommendations for board layout. These documents are available at the Texas Instruments web site (<http://www.ti.com>) by searching for the literature number.
- (3) Laser-cutting apertures with trapedzoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for stencil design considerations.
- (4) Customers should contact their board fabrication site for minimum solder mask tolerances between signal pads.

**Figure 26. Recommended Land Pattern for DSE Package**



- (1) Devices in a YFF package can have a dimension that ranges within a specified tolerance. To determine the exact measurements, contact a local Texas Instruments representative.

**Figure 27. YFF Package Dimensions**

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September, 2009) to Revision B	Page
• Changed title of data sheet .....	1
• Updated <i>Features</i> list .....	1
• Changed footnote 2 to <a href="#">Absolute Maximum Ratings</a> table .....	2
• Revised numerous specifications and parameters in <a href="#">Electrical Characteristics</a> table .....	3
• Revised operating parameters for <a href="#">Figure 5</a> .....	5
• Added operating parameters to <a href="#">Figure 7</a> .....	6
• Replaced <a href="#">Figure 6</a> .....	6
• Updated <a href="#">Figure 10</a> .....	7

Changes from Original (June, 2009) to Revision A	Page
• Changed PSRR value in <i>Features</i> list from 80dB to 70dB .....	1
• Updated YFF WCSP device graphics ( <a href="#">front page</a> , <a href="#">pin drawing</a> , <a href="#">Figure 27</a> ) to accurately reflect package layout .....	1
• Updated format of characteristic performance graphs ( <a href="#">Figure 18</a> through <a href="#">Figure 22</a> ) .....	8
• Changed wording of first paragraph in <i>Internal Current Limit</i> section .....	10



PACKAG

## PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Pe
TPS72711YFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-2600
TPS72711YFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-2600
TPS72715DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
TPS72715DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
TPS72715YFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-2600
TPS72715YFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-2600
TPS727185YFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-2600
TPS727185YFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-2600
TPS72718DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
TPS72718DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
TPS72718YFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-2600
TPS72718YFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-2600
TPS72725DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
TPS72725DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
TPS727285DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600
TPS727285DSET	ACTIVE	WSON	DSE	6	250	TBD	Call TI	Call TI
TPS72728DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-2600



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Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp
TPS72728DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C
TPS72728YFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C
TPS72728YFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C
TPS72730DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C
TPS72730DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C
TPS72733DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C
TPS72733DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/eco> for more information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all semiconductor products having no more than 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in high temperature applications.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die attach between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (as required by UL recognition). TI Green products are suitable for use in applications where RoHS compliance is required. (All other components must not contain Pb, Br, or Sb in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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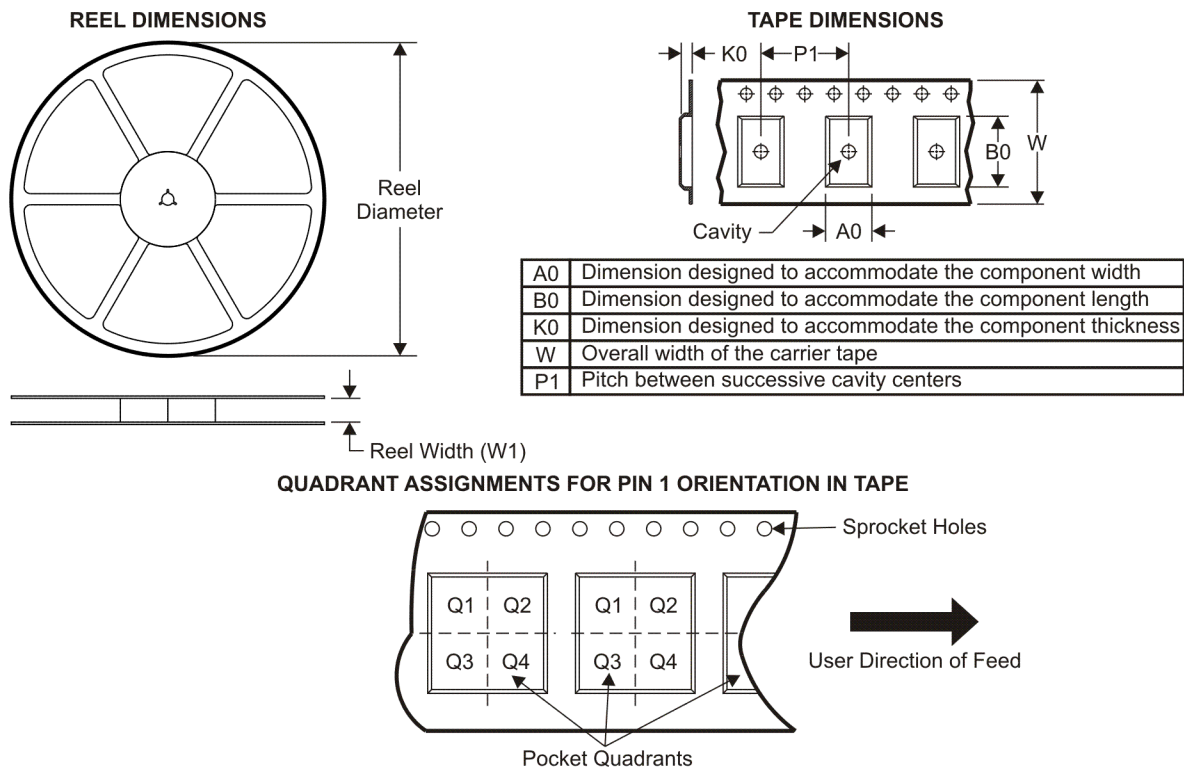


**PACKAG**

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**TAPE AND REEL INFORMATION**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS72725DSER	WSO	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TPS72725DSET	WSO	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TPS727285DSER	WSO	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TPS72728DSER	WSO	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TPS72728DSET	WSO	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TPS72730DSER	WSO	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TPS72730DSET	WSO	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TPS72733DSER	WSO	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TPS72733DSET	WSO	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2

## TAPE AND REEL BOX DIMENSIONS



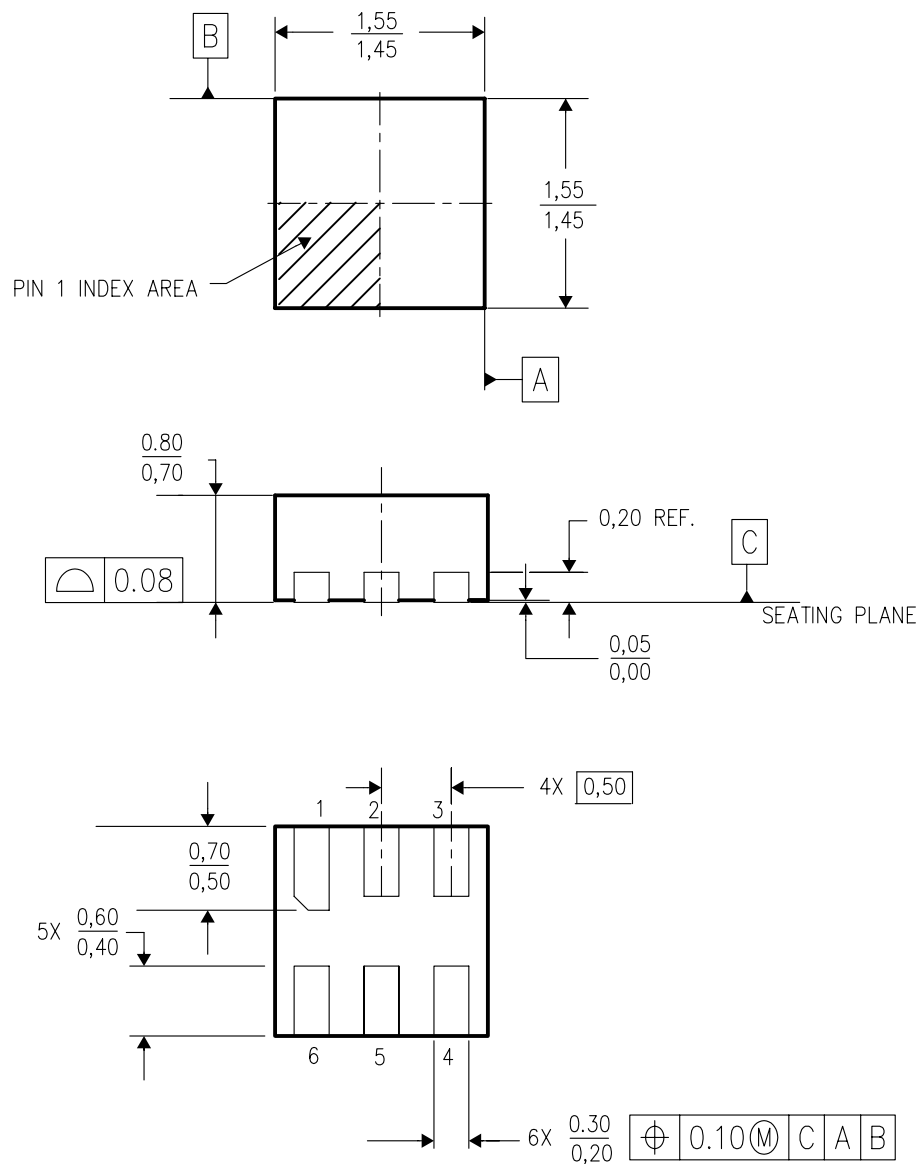
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS72725DSER	WSON	DSE	6	3000	203.0	203.0	35.0
TPS72725DSET	WSON	DSE	6	250	203.0	203.0	35.0
TPS727285DSER	WSON	DSE	6	3000	203.0	203.0	35.0
TPS72728DSER	WSON	DSE	6	3000	203.0	203.0	35.0
TPS72728DSET	WSON	DSE	6	250	203.0	203.0	35.0
TPS72730DSER	WSON	DSE	6	3000	203.0	203.0	35.0
TPS72730DSET	WSON	DSE	6	250	203.0	203.0	35.0
TPS72733DSER	WSON	DSE	6	3000	203.0	203.0	35.0
TPS72733DSET	WSON	DSE	6	250	203.0	203.0	35.0

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## DSE (S-PDSO-N6)

## PLASTIC SMALL OUTLINE

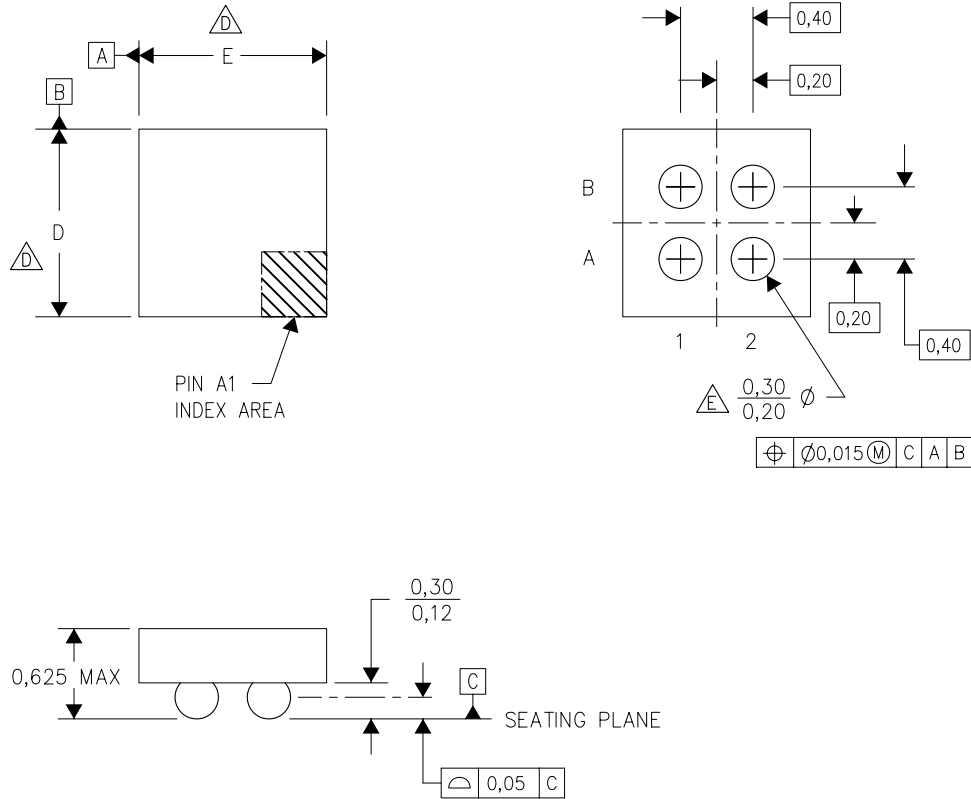


4207810/A 03/06

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Small Outline No-Lead (SON) package configuration.
  - This package is lead-free.

YFF (S-XBGA-N4)

DIE-SIZE BALL GRID ARRAY

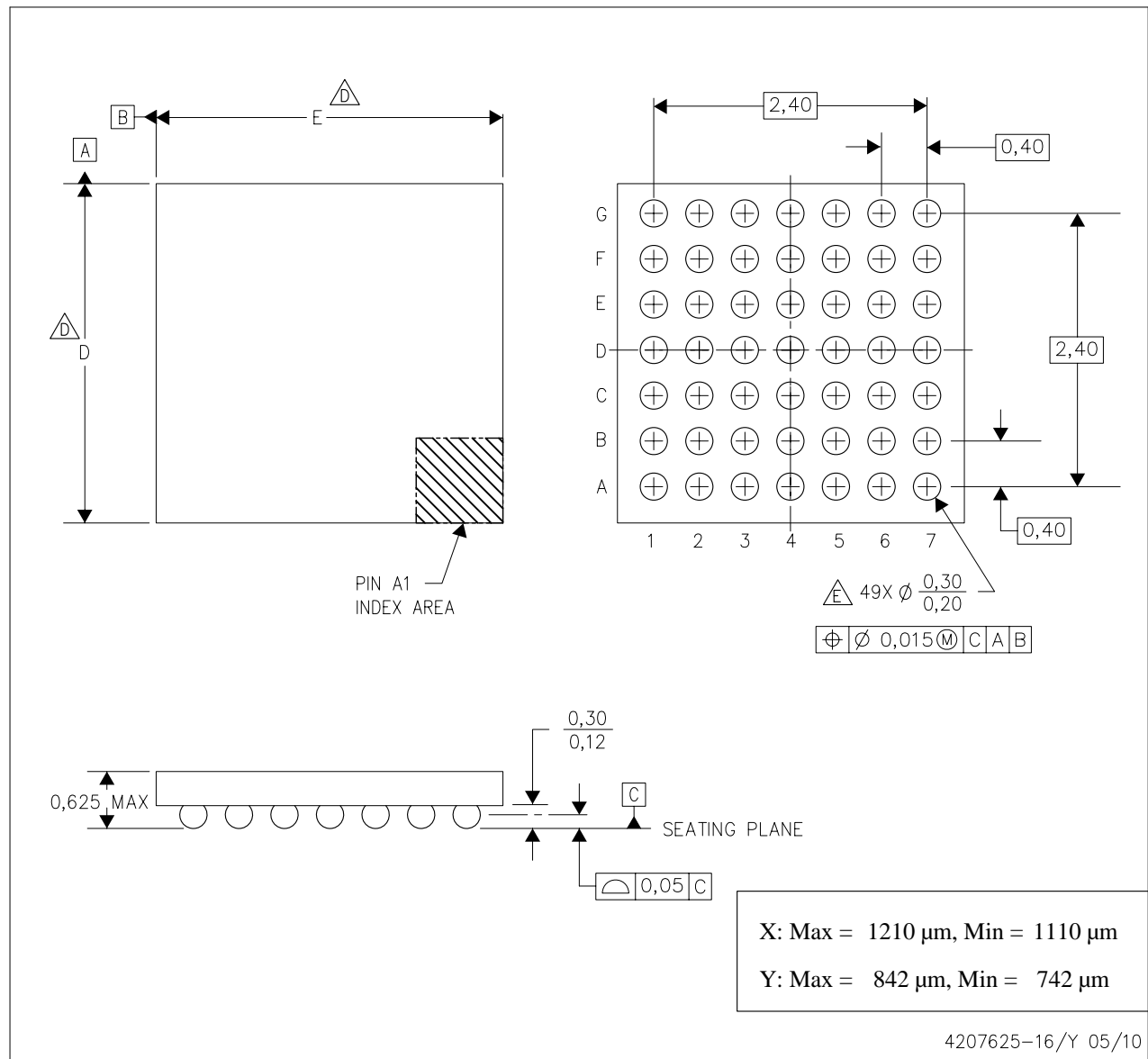
X: Max = 1210  $\mu$ m, Min = 1110  $\mu$ mY: Max = 842  $\mu$ m, Min = 742  $\mu$ m

4207625-2/Y 05/10

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. NanoFree™ package configuration.
  - $\Delta$  Devices in YFF package can have dimensions D ranging from 0.76 to 1.45 mm and dimension E ranging from 0.76 to 1.45 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
  - E. Reference Product Data Sheet for array population.  
2 x 2 matrix pattern is shown for illustration only.
  - F. This package contains Pb-free balls.

YFF (R-XBGA-N49)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. NanoFree™ package configuration.
  - D. Devices in YFF package can have dimension D ranging from 2.73 to 3.45 mm and dimension E ranging from 2.73 to 3.45 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
  - E. Reference Product Data Sheet for array population. 7 x 7 matrix pattern is shown for illustration only.
  - F. This package contains Pb-free balls.

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DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>	Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>	Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Energy	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>	Space, Avionics & Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>	Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless-apps">www.ti.com/wireless-apps</a>