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3SK181

T-31-25

2046

N-Channel Enhancement
MOS Silicon FET(Dual Gate)

©2130A

High-Frequency General-Purpose Amp Applications

Applications
- FM tuners and VHF tuners

Features
- Enhancement type
- Easy AGC (Cut off at V_{G2S}= 0V)
- High power gain and low noise figure
- High forward transfer admittance

Absolute Maximum Ratings at Ta=25°C

			unit
Drain to Source Voltage	V_{DS}	15	V
Gate 1 to Source Voltage	V_{G1S}	±10	V
Gate 2 to Source Voltage	V_{G2S}	±10	V
Drain Current	I_D	30	mA
Power Dissipation	P_D	200	mW
Channel Temperature	T_{ch}	125	°C
Storage Temperature	Tstg	-55 to +125	°C

Electrical Characteristics at Ta=25°C

			min	typ	max	unit
Drain to Source Voltage	V_{DS}	V_{G1S}=0V, V_{G2S}=0V I_{DS}=100uA	15			V
Gate 1 to Source Breakdown Voltage	$V_{(BR)G1SS}$	I_{G1}=10uA, V_{DS}=0V V_{G2S}=0V	±10			V
Gate 2 to Source Breakdown Voltage	$V_{(BR)G2SS}$	I_{G2}=10uA, V_{DS}=0V V_{G1S}=0V	±10			V
Gate 1 to Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS}=10V, V_{G2S}=6V I_D=100uA	0	0.7	1.3	V
Gate 2 to Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS}=10V, V_{G1S}=3V I_D=100uA	0.1	0.9	1.6	V
Gate 1 Cutoff Current	I_{G1SS}	V_{G1S}=4V, V_{G2S}=V_{DS}=0V			50	nA
Gate 2 Cutoff Current	I_{G2SS}	V_{G2S}=8V, V_{G1S}=V_{DS}=0V			50	nA
Drain Current	I_{DSX}	V_{DS}=10V, V_{G1S}=1.5V V_{G2S}=6V	2.5*		24*	mA

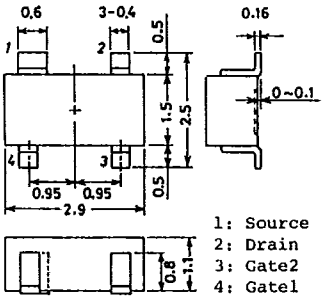
Continued on next page.

*: The 3SK181 is classified by I_{DSX} as follows (unit:mA):

2.5	4	6.0	5.0	5	12.0	10.0	6	24.0

(Note) Marking: EJ
I_{DSX} rank : 4,5,6

Case Outline 2046
(unit:mm)



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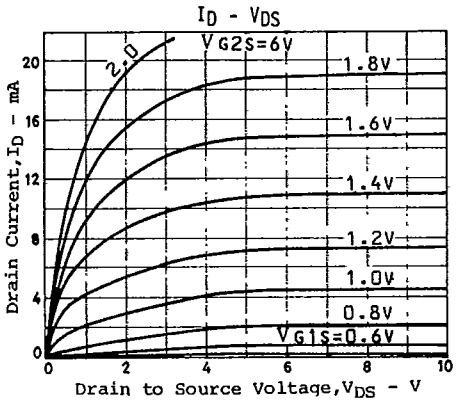
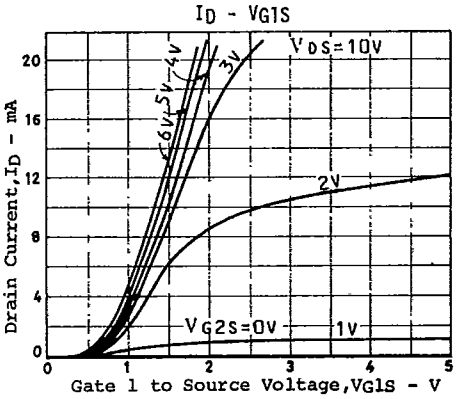
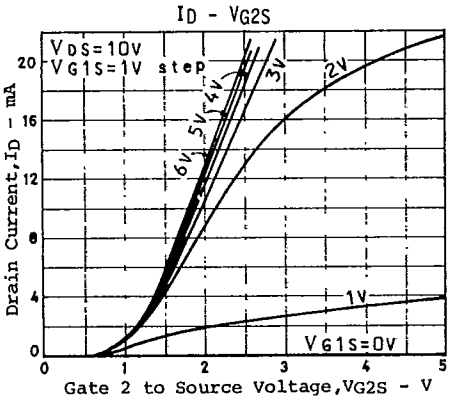
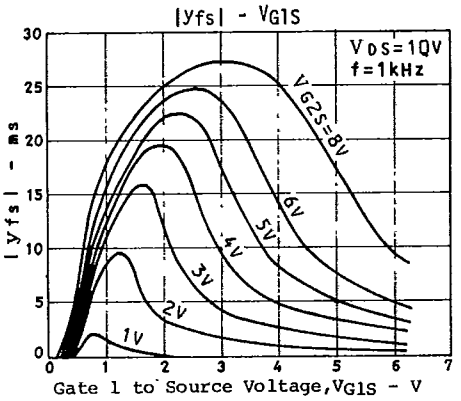
Continued from preceding page.

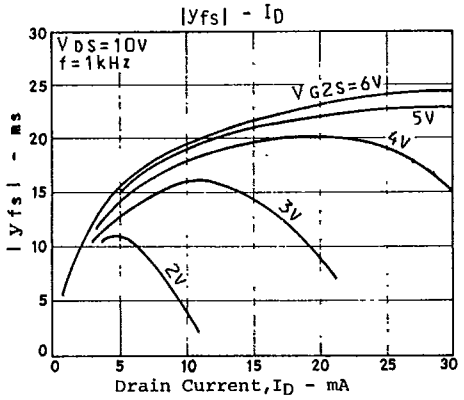
			min	typ	max	unit
Forward Transfer Admittance	|Yfs|	f=1kHz, I_D=10mA, V_{DS}=10V, V_{G2S}=6V		18		ms
Input Capacitance	C_{iss}	V_{DS}=10V, f=1MHZ, V_{G1S}=0V, V_{G2S}=6V		3.0		pF
Reverse Transfer Capacitance	C_{rss}			0.02	0.05	pF
Power Gain	PG	V_{DS}=10V, I_D=10mA	22	28		dB
Noise Figure	NF	f=100MHz, V_{G2S}=6V		1.8	3.0	dB

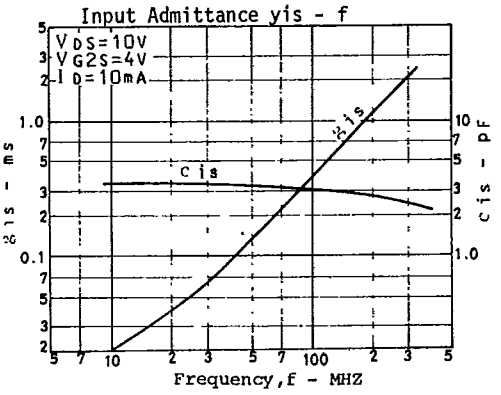












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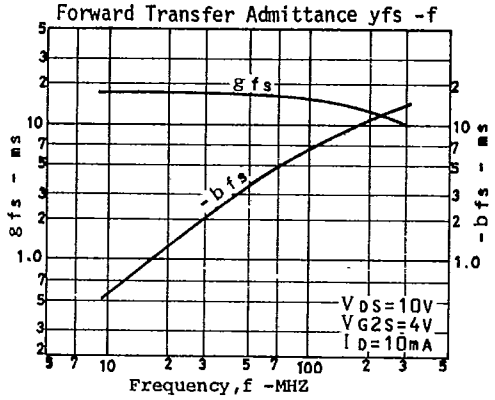
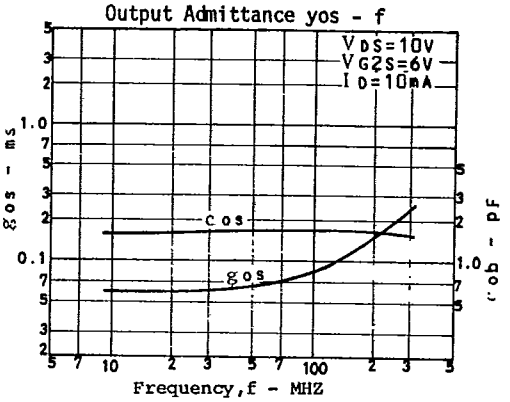
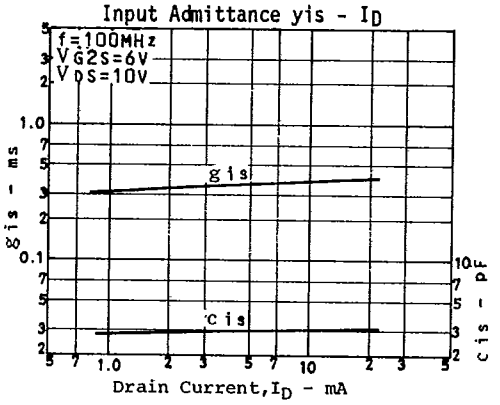
Forward Transfer Admittance yfs -f



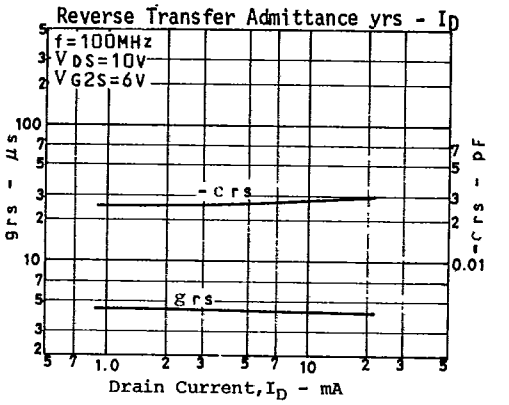
Output Admittance yos - f



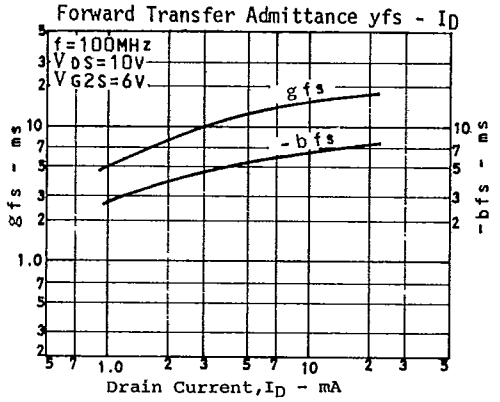
Input Admittance yis - ID



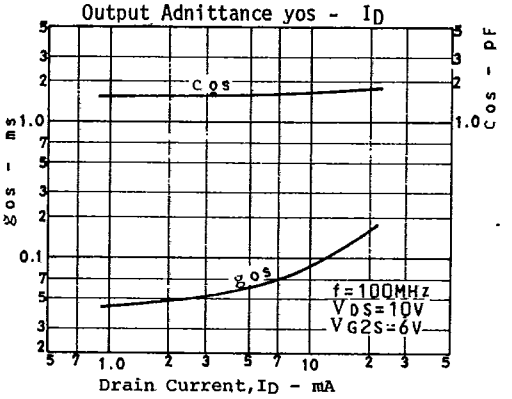
Reverse Transfer Admittance yrs - ID



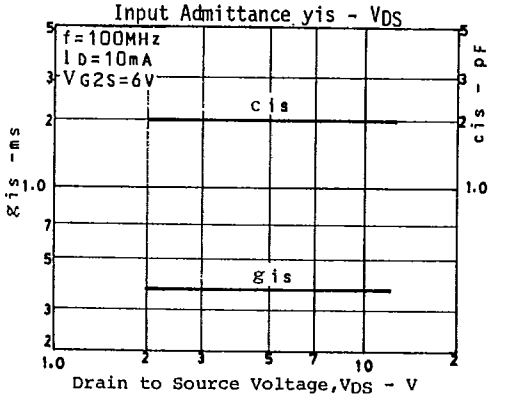
Forward Transfer Admittance yfs - ID



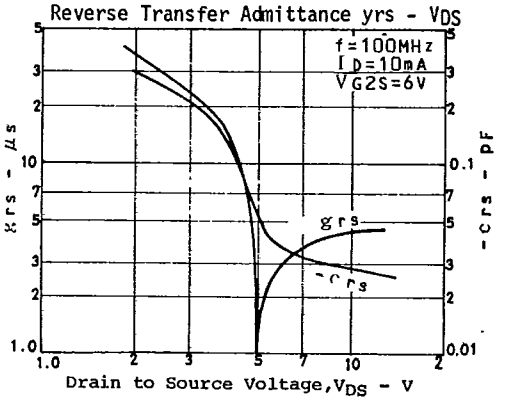
Output Admittance yos - ID



Input Admittance yis - VDS



Reverse Transfer Admittance yrs - VDS



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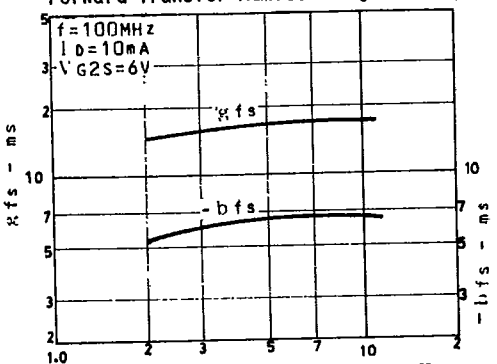
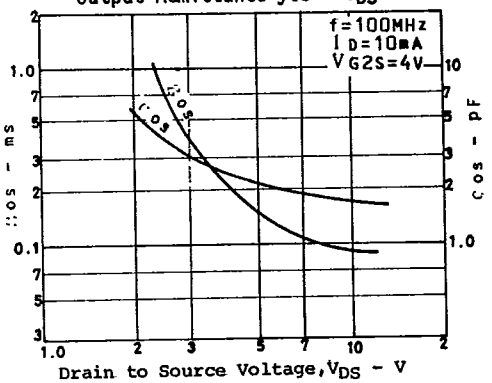
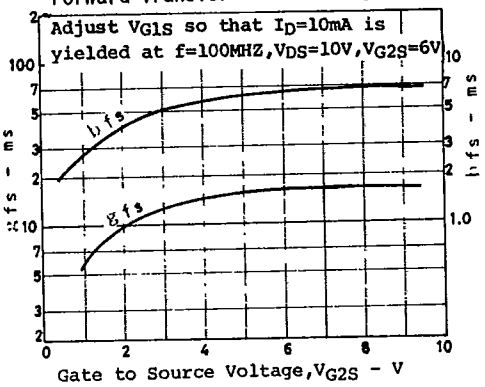
Forward Transfer Admittance yfs - VDS



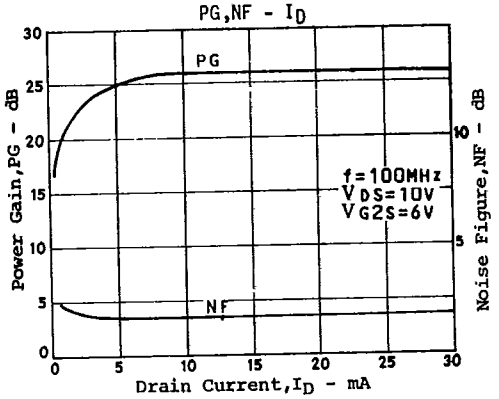
Output Admittance yos - VDS



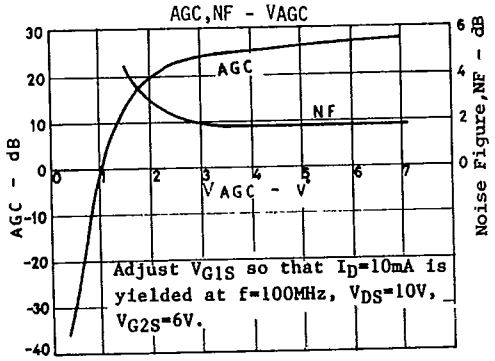
Forward Transfer Admittance yfs - VG2S



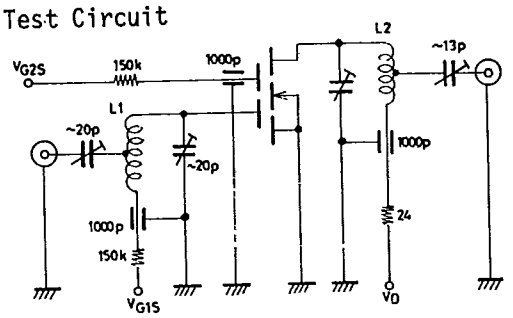
PG,NF - ID



AGC,NF - VAGC



PG,NF Test Circuit



L1: 1mmφ plated wire 10mmφ 4T, tap: 1T from gate side.
L2: 1mmφ plated wire 10mmφ 6T, tap: 1T from drain side.

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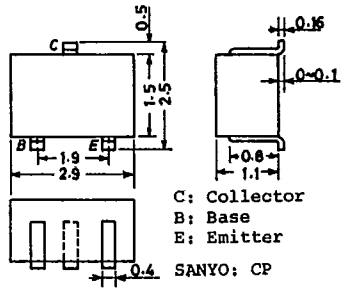
CASE OUTLINES OF SURFACE MOUNT TRANSISTORS

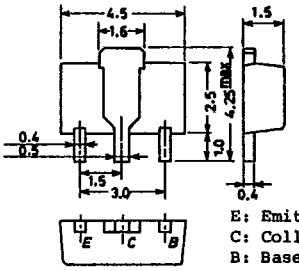
- All of Sanyo surface mount transistor case outlines are illustrated below.
- All dimensions are in mm, and dimensions which are not followed by min. or max. are represented by typical values.
- No marking is indicated.

Case Outline—[2018A] unit: mm



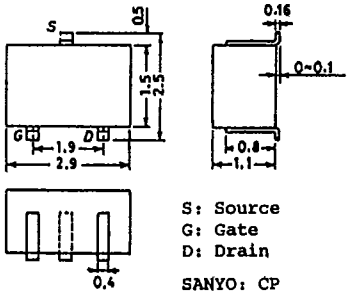
C: Collector
B: Base
E: Emitter
SANYO: CP

Case Outline—[2038] unit: mm



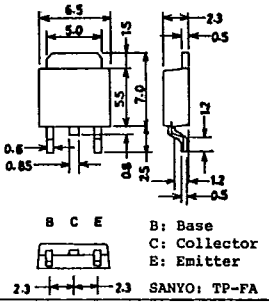
E: Emitter
C: Collector
B: Base
SANYO: PCP

Case Outline—[2024A] unit: mm



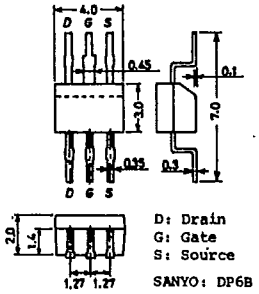
S: Source
G: Gate
D: Drain
SANYO: CP

Case Outline—[2044] unit: mm



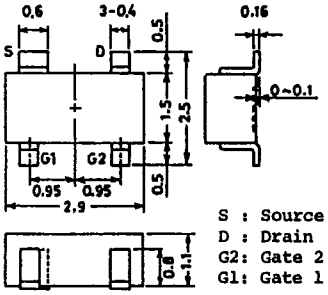
B: Base
C: Collector
E: Emitter
SANYO: TP-FA

Case Outline—[2028A] unit: mm



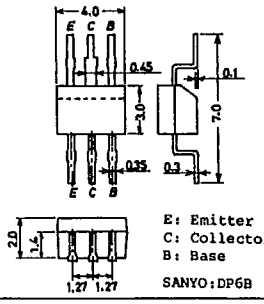
D: Drain
G: Gate
S: Source
SANYO: DP6B

Case Outline—[2046] unit: mm



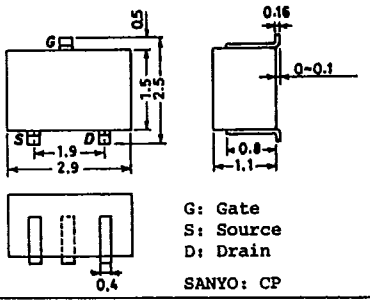
S : Source
D : Drain
G2: Gate 2
G1: Gate 1

Case Outline—[2030A] unit: mm



E: Emitter
C: Collector
B: Base
SANYO:DP6B

Case Outline—[2050] unit: mm



G: Gate
S: Source
D: Drain
SANYO: CP

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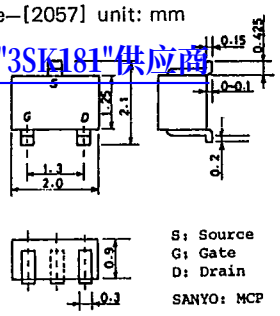
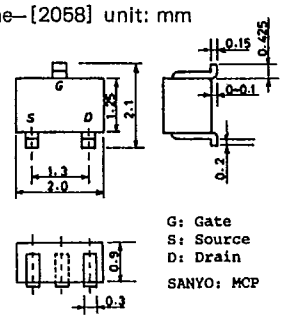
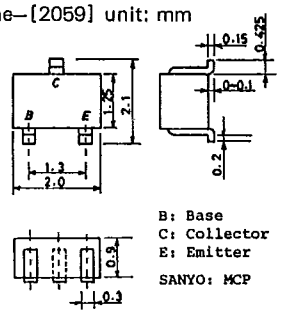
Case Outline—[2057] unit: mm



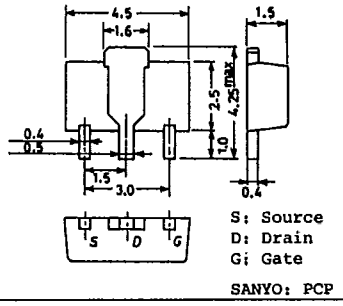
Case Outline—[2058] unit: mm



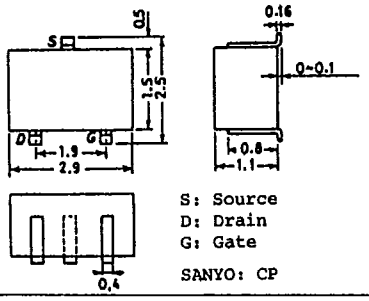
Case Outline—[2059] unit: mm



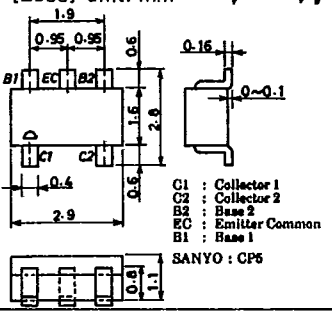
Case Outline—[2062] unit: mm



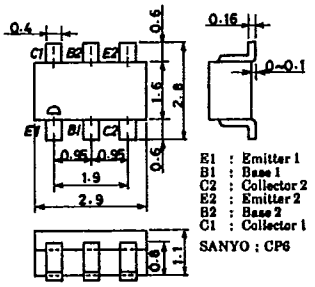
Case Outline—[2065] unit: mm



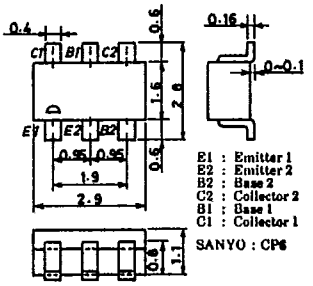
Case Outline—[2066] unit: mm



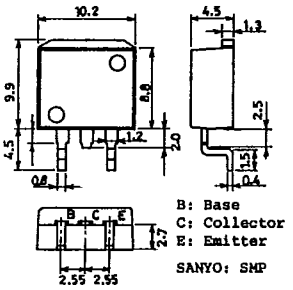
Case Outline—[2067] unit: mm



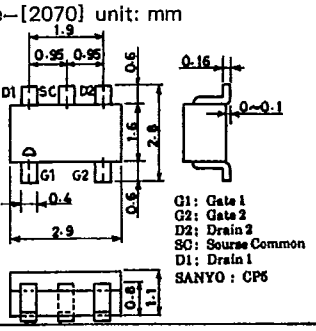
Case Outline—[2068] unit: mm



Case Outline—[2069] unit: mm



Case Outline—[2070] unit: mm



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Case Outline—[2071] unit: mm

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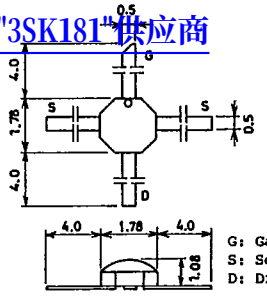
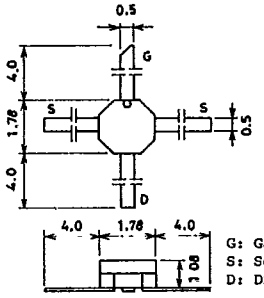
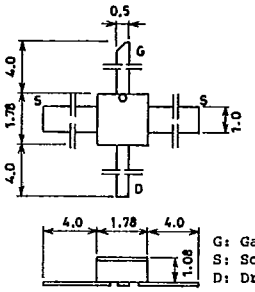


Case Outline—[2072] unit: mm



Case Outline—[2073] unit: mm