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PMIC N/A

STANDARDIZED MILITARY DRAWING

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DRAWING APPROVAL DATE
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REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, BIPOLAR, FIELD PROGRAMMABLE SEQUENCER (FPLS)

SIZE	CAGE CODE	
A	67268	5962-88507

SHEET 1 OF 18

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911
5962-E704

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-88507	01	L	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	PLS179	(20x45x12) field programmable logic sequencer

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
L	D-9 (24-lead, 0.300 row spacing) dual-in-line package

1.3 Absolute maximum ratings.

Supply voltage	7.0 V dc
Input voltage	10.0 V dc
Output voltage	5.5 V dc
Input current (minimum)	-30 mA
Input current (maximum)	30 mA
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 1/	1.2 W
Thermal resistance, junction-to-case (θ_{JC}): Case L	See MIL-M-38510, appendix C
Junction temperature (T_J)	+200°C
Output sink current	100 mA

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
Minimum high level input voltage (V_{IH})	2.2 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Logic diagram. The logic diagram shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Limits Min	Limits Max	Unit
Low level input voltage	V_{IL}	V_{CC} = 4.5 V	1,2,3		0.8	V
High level input voltage	V_{IH}	V_{CC} = 5.5 V	1,2,3	2.2		V
Input clamp voltage 2/	V_{IC}	V_{CC} = 4.5 V, I_I = -18 mA	1,2,3		-1.2	V
Low level input current	I_{IL}	V_{CC} = 5.5 V, V_I = 0.45 V	1,2,3		-100	µA
Low level input current (CLK input)	I_{IL}	V_{CC} = 5.5 V, V_I = 0.45 V	1,2,3		-250	µA
High level input current	I_{IH}	V_{CC} = 5.5 V, V_I = 5.5 V	1,2,3		40	µA
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, V_{IL} = 0.8 V, V_{IH} = 2 V, I_{OL} = 10 mA	1,2,3		0.5	V
High level output voltage	V_{OH}	V_{CC} = 4.5 V, V_{IL} = 0.8 V, V_{IH} = 2 V, I_{OH} = -2 mA	1,2,3	2.4		V
Output short-circuit current 2/ 3/	I_{OS}	V_{CC} = 4.5 V, V_O = 0 V	1,2,3	-15	-85	mA
DC supply current 4/	I_{CC}	V_{CC} = 5.5 V	1,2,3		210	mA
Three-state output current 5/ 6/	I_{OZ}	V_{CC} = 5.5 V, V_{OUT} = 5.5 V	1,2,3		80	µA
		V_{CC} = 5.5 V, V_{OUT} = 0.45 V			-140	µA
Functional tests		See 4.3.1d	7,8			
Propagation delay: Clock	t_{CKO}	V_{CC} = 5.0 V ±10%, R_1 = 470Ω, R_2 = 1 kΩ, C_L = 50 pF, See figures 4 and 5	9,10,11		25	ns
Output enable	t_{OE1}	To prevent spurious clocking, clock rise time (10%-90%) ≤ 10 ns	9,10,11		35	ns
Output disable 7/	t_{OD1}		9,10,11		35	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Output	t_{PD}	V_{CC} = 5.0 V ±10% R_1 = 470Ω, R_2 = 1 kΩ, C_L = 50 pF See figures 4 and 5 To prevent spurious clocking, clock rise time (10%-90%) ≤ 10 ns	9,10,11		40	ns
Output enable	t_{OE2}		9,10,11		40	ns
Output disable 7/	t_{OD2}		9,10,11		40	ns
Preset/reset	t_{PRO}		9,10,11		50	ns
Power-on preset	t_{PPR}		9,10,11		20	ns
Pulse width: Clock high 7/ 8/	t_{CKH}		9,10,11	25		ns
Clock low 8/	t_{CKL}		9,10,11	25		ns
Period 8/	t_{CKP}		9,10,11	65		ns
Preset/reset pulse 8/	t_{PRH}		9,10,11	45		ns
Setup time: Input 8/	t_{IS1}		9,10,11	40		ns
Input (through F_N) 8/	t_{IS2}		9,10,11	25		ns
Input (through complement array) 8/ 9/	t_{IS3}		9,10,11	65		ns
Hold time: Input 8/	t_{IH1}		9,10,11	0		ns
Input (through F_N) 8/	t_{IH2}		9,10,11	15		ns

See footnotes on next page.

1/ All voltage values are with respect to ground.

2/ Test one at a time.

3/ Duration of short circuit should not exceed 1 second.

4/ I_{CC} is measured with the $\overline{OE}$ input grounded, all other inputs at 4.5 V, and the outputs open.

5/ Measured with V_{IH} applied to $\overline{OE}$.

6/ Leakage values are a combination of input and output leakage.

7/ Measured at $V_T = V_{OL} + 0.5$ V.

8/ Limits are guaranteed with 12 product terms maximum connected to each sum term line.

9/ When using the complement array t_{VKP} = 75 ns (minimum).

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.9 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations; two processing options are provided for selection in the contract, using an altered item drawing.

3.9.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 4.3.1c and table II. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.9.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. All devices processed to an altered item drawing may be programmed either before or after burn-in at the manufacturer's discretion. The required electrical testing shall include, as a minimum, the final electrical tests for programmed devices as specified in table II herein.

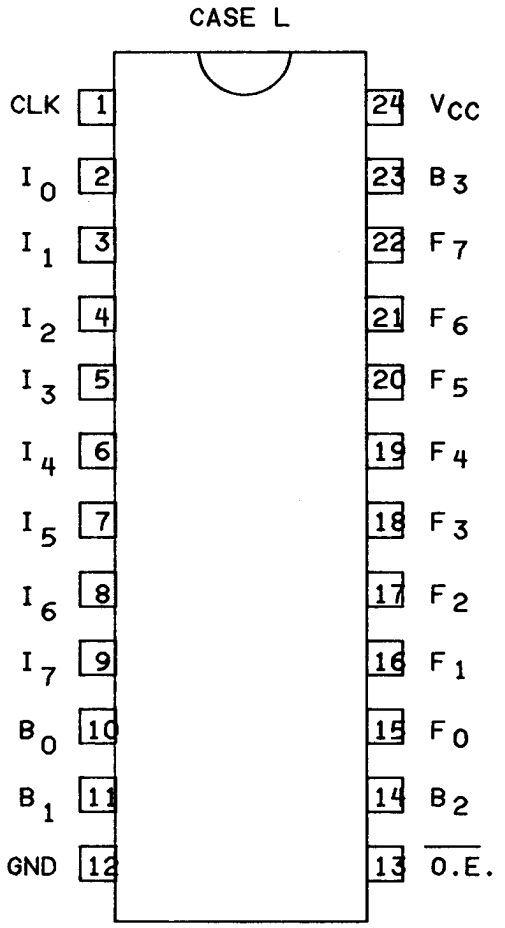

FIGURE 1. Terminal connections.

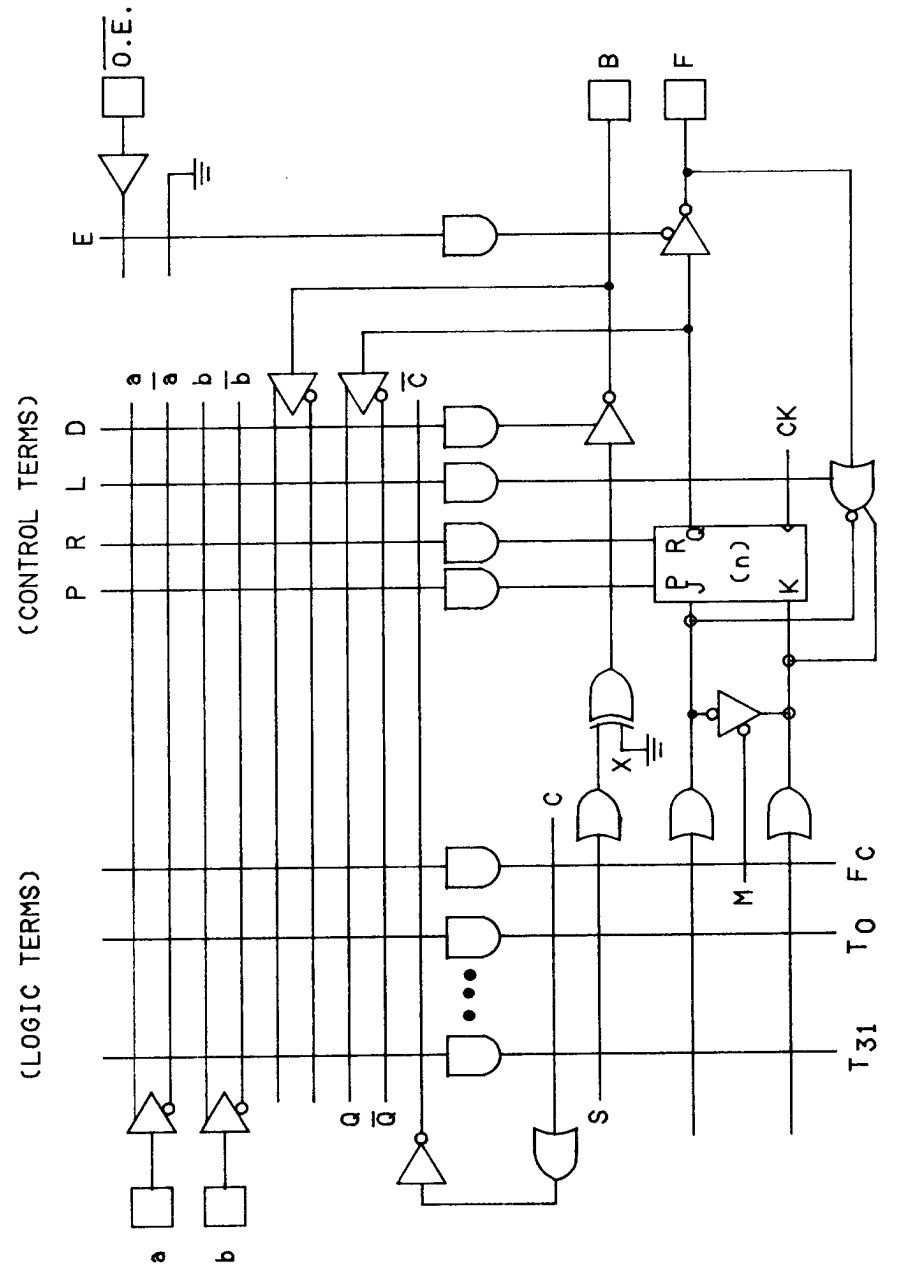

FIGURE 2. Logic diagram.

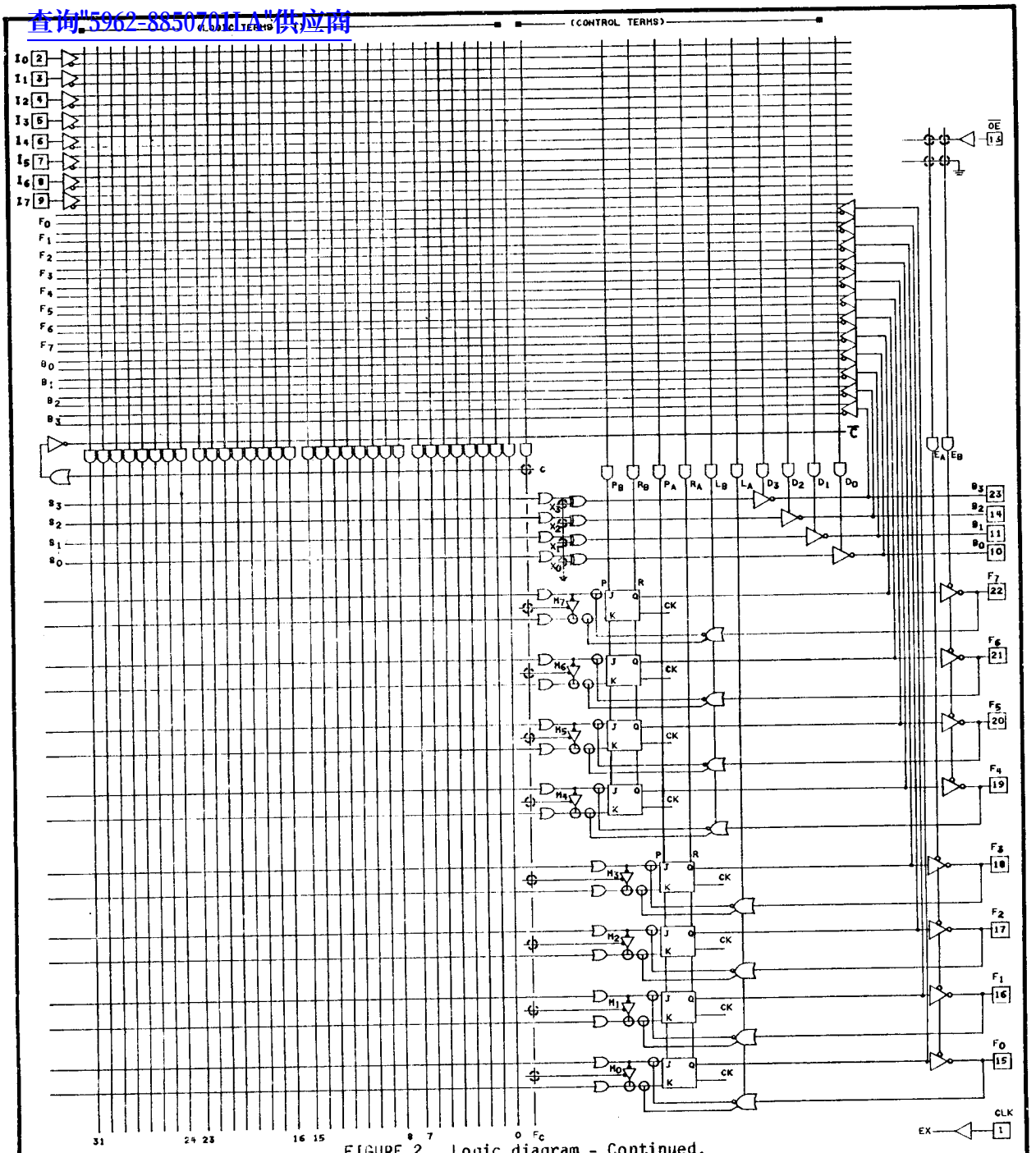

FIGURE 2. Logic diagram - Continued.

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NOTES:

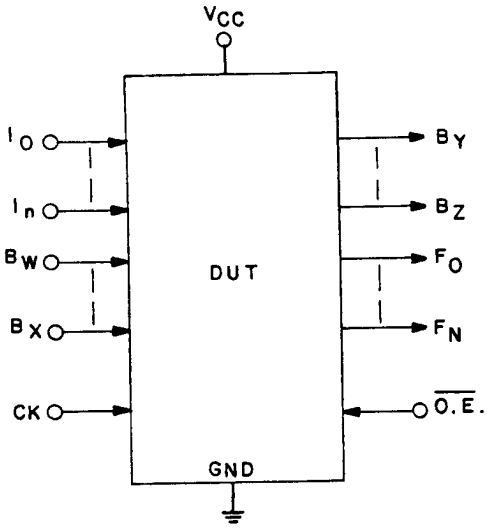
1. All OR gate inputs with a blown link float to logic "0".
2. All other gates and control inputs with a blown link float to logic "1".
3. ⊕ denotes WIRE-OR.
4. ◌ programming connection.

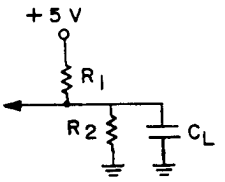
FIGURE 2. Logic diagram - Continued.

$\overline{OE}$	L	CK	P	R	J	K	Q	F
H								H/Hi-Z
L	X	X	L	X	X	X	L	H
L	X	X	H	L	X	X	H	L
L	X	X	L	H	X	X	L	H
L	L	↑	L	L	L	L	Q	$\overline{Q}$
L	L	↑	L	L	L	H	L	H
L	L	↑	L	L	H	L	H	L
L	L	↑	L	L	H	H	$\overline{Q}$	Q
H	H	↑	L	L	L	H	L	H*
H	H	↑	L	L	H	L	H	L*
+10 V	X	↑	X	X	L	H	L	H**
	X	↑	X	X	H	L	H	L**

NOTES:
1. Positive logic:
   $J/K = \overline{T_0} + T_1 + T_2 + \ldots + T_{32}$
   $T_n = \overline{C} \cdot (I_0 \cdot I_1 \cdot I_2 \ldots) \cdot (Q_0 \cdot Q_1 \ldots) \cdot (B_0 \cdot B_1 \ldots)$
2. ↑ denotes transition from low to high level.
3. X = Don't care.
4. * = Forced at F_n pin for loading J/K flip-flop in I/O mode. L must be enabled, and other active t_n disabled via steering input(s) I, B, or Q.
5. At P = R = H, Q = H. The final state of Q depends on which is released first.
6. ** = Forced at F_n pin to load J/K flip-flop independent of program code (diagnostic mode).

FIGURE 3. Truth table.



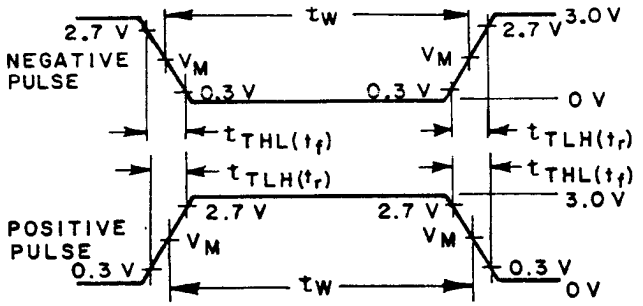


(INCLUDES SCOPE AND JIG CAPACITANCE)

NOTE: R_1 = 470Ω, R_2 = 1 kΩ, C_L = 50 pF.

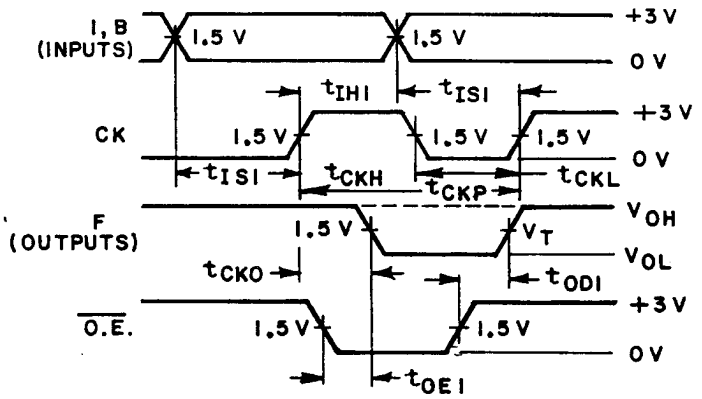
FIGURE 4. Test load circuit.

VOLTAGE WAVEFORMS

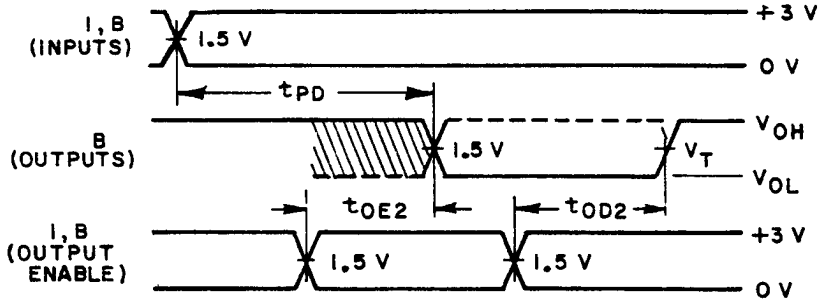


Input pulse characteristics				
V_M	Rep. rate	Pulse width	t_{TLH}	t_{THL}
1.5 V	1 MHz	500 ns	≤5 ns	≤5 ns

FIGURE 5. Timing waveforms.

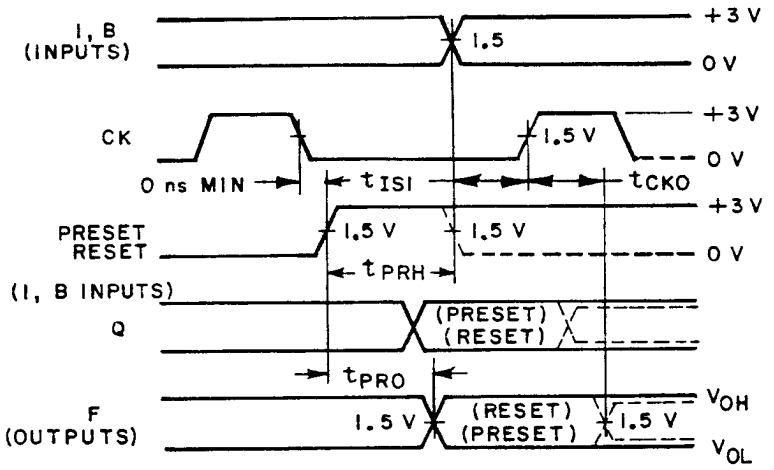


FLIP–FLOP OUTPUTS



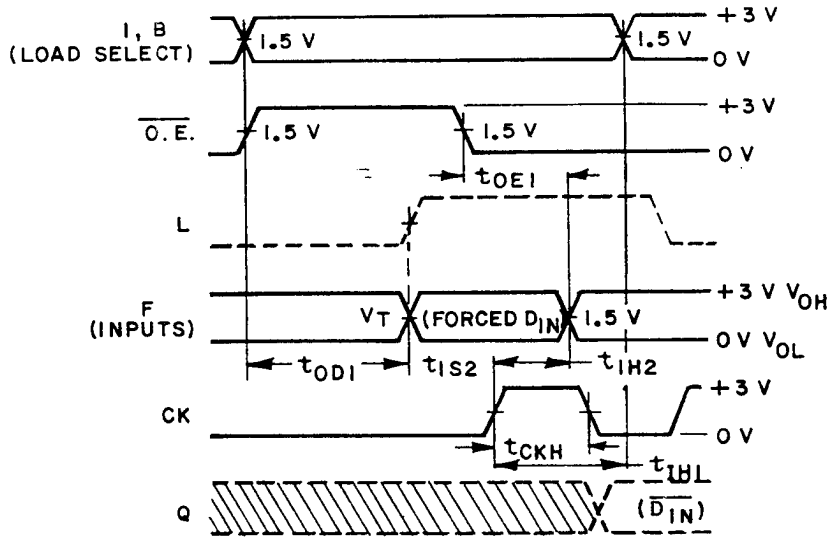
GATE OUTPUTS

FIGURE 5. Timing waveforms - Continued.



*Preset and reset functions override clock. However, F outputs may glitch with the first positive clock edge if t_{ISI} cannot be guaranteed by the user.

ASYNCHRONOUS PRESET/RESET



FLIP-FLOP INPUT MODE

FIGURE 5. Timing waveforms - Continued.

Memory timing definitions

t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{CKP}	Clock period.
t_{PRH}	Width of preset input pulse.
t_{IS1}	Required delay between beginning of valid input and positive transition of clock.
t_{IS2}	Required delay between beginning of valid input forced at flip-flop output pins, and positive transition of clock.
t_{IH1}	Required delay between positive transition of clock and end of valid input data.
t_{IH2}	Required delay between positive transition of clock and end of valid input data forced at flip-flop output pins.
t_{CKO}	Delay between positive transition of clock and when outputs become valid (with $\overline{O.E.}$ low).
t_{OE1}	Delay between beginning of output enable low and when outputs become valid.
t_{OD1}	Delay between beginning of output enable high and when outputs are in the off-state.
t_{PD}	Propagation delay between combinational inputs and outputs.
t_{OE2}	Delay between predefined output enable high, and when combinational outputs become valid.
t_{OD2}	Delay between predefined output enable low and when combinational outputs are in the off-state.
t_{PRO}	Delay between positive transition of predefined preset reset input, and when flip-flop outputs become valid.

FIGURE 5. Timing waveforms - Continued.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Unprogrammed devices shall be tested for programmability and ac performance compliance to the requirement of group A, subgroups 9, 10, and 11. Either of two techniques is acceptable:

(1) Testing the entire lot using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, and 11, group A testing in accordance with the sampling plan specified in MIL-STD-883, method 5005.

(2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming. If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable.

Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two total devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

d. Subgroups 7 and 8 must verify input to output logic combinations.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

4.4 Programming procedures. The programming procedures shall be as specified by the device manufacturer.

TABLE II. Electrical test requirements. 1/ 2/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004) for programmed devices	1*,2,3,7*,8,9
Final electrical test parameters (method 5004) for unprogrammed devices	1*,2,3,7*, 8,9
Group A test requirements (method 5005)	1,2,3,7,8,9,10, 11
Groups C and D end-point electrical parameters (method 5005)	1,2,3

* PDA applies to subgroups 1 and 7.
1/ Any or all subgroups may be combined when using high-speed testers.
2/ Subgroups 7 and 8 funtional test shall also verify that no fuses are blown for unprogrammed devices or that the altered item drawing pattern exists for programmed devices.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8850701LX	18324	PLS179/BLX	

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address	Fusible link
18324	Signetics, Incorporated 4130 South Market Court Sacramento, CA 95834	Ni-chrome

011678