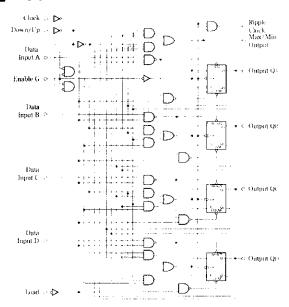
clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down. Level changes at the down/up input should be made only when the clock input is high. This counter is fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs. The clock, down/up, and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers, etc., required for long parallel words.

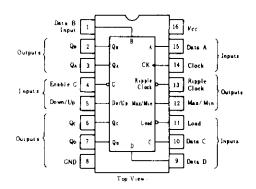
Two outputs have been made available to perform the cascading function; ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycles to the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists.

The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

BLOCK DIAGRAM



PIN ARRANGEMENT



RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Clock frequency	felock	0	-	20	MHz
Clock pulse width	tic (CK)	25		<u> </u>	ns
Load input pulse width	in Hond)	35			ns
Setup time	tou :	20		-	ns
Hold time	th	3	_		ns
Enable time	tenable ;	40			ns

■ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^{\circ}$)

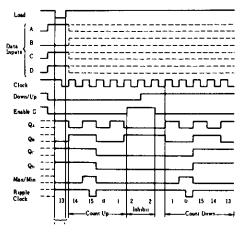
Ite	n	Symbol	Test Conditions		min	typ*	max	Unit
	-1	Vin			2.0	_		V
Input voltage		VIL				_	0.8	V
		Von	$V_{CC} = 4.75 \text{ V}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -400 \mu\text{A}$		2.7	_	_	V
Output voltage			$I_{OL} = 4 \text{mA}$	-	_	0.4	v	
	Vol	$V_{CC} = 4.75 \text{V}, V_{IH} = 2 \text{V}, V_{IL} = 0.8 \text{V}$	$I_{OL} = 8 \text{mA}$		_	0.5		
	Enable		7) = 0.011 7; 0.411				60	4
	Others	— Іін	$V_{CC} = 5.25 \text{V}, V_I = 2.7 \text{V}$		_	_	20	μΑ
	Enable					_	-1.2	4
Input current	Others	In	$V_{CC} = 5.25 \text{ V}, V_I = 0.4 \text{ V}$				-0.4	mA
	Enable					_	0.3	^
	Others	- Iı	$V_{CC}=5.25V, V_I=7V$			_	0.1	mA
Short-circuit out	put current	Ios	Vcc=5.25V		-20	-	-100	mA
Supply current**		Icc	Vcc=5.25V		_	20	35	m A
Input clamp volta		Vik	$V_{\rm CC} = 4.75 \text{V}, I_{IN} = -18 \text{mA}$				-1.5	V

^{*} VCC=5V, Ta=25°C

ESWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25^{\circ}C$)

Îtem	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	fmax				20	25	<u> </u>	MH
	tPLH	, ,	QA, QB, QC, QD	$C_L=15 ext{pF}$ $R_L=2 ext{k}\Omega$		22	33	ns
	tphL.	Load			_	33	50	
	tPLH	Data A ,B,C,D	QA, QB, QC, QD		_	20	32	ns
	tPHL				-	27	40	
	t _{PLH}	Clock Ripple Clock	Bil- Clk			13	20	ns
Propagation delay time	tPHL		Rippie Clock			16	24	
	tPLH	Clock	QA, QB, QC, QD			16	24	ns
	tPHL				·· –	24	36	
	tPLH	Clock	Max/Min			28	42	ns
	tPHL					37	52	
	tPLH	Down/Up	Ripple Clock		_	30	45	ns
	tphl			1		30	45	
	tplh	Down/Up Max/Min	h4 /34:		_	21	33	ns
	tphL			_	22	33	ns	
	tplH	F 11	Di- J. Cl. J.		_	21	33	ns
	tphL	Enable	Ripple Clock			22	33	

ECOUNT SEQUENCES



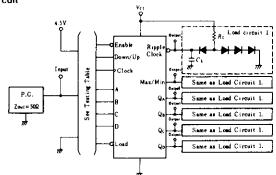
Illustrated below is the following sequence;

- 1. Load (preset) to binary thirteen.
- 2. Count up to fourteen, fifteen (maximum), zero, one, and two.
- 3. Inhibit
- Count down to one, zero (minimum), fifteen, fourteen, and thirteen.

^{**} I_{CC} is measured with all outputs open and all inputs grounded.

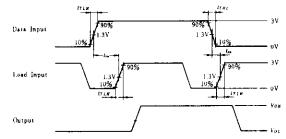
■TES查询G-ME+LGOO1"供应商

1) Test Circuit



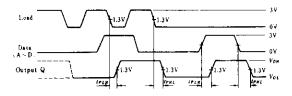
Notes) 1. C_L includes probe and jig capacitance. 2. All diodes are 1S2074 (H).

Waveform



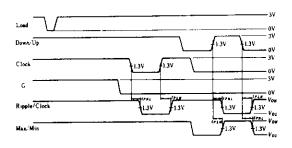
Input pulse: t_{TLH}, t_{THL} \le 10ns, PRR=1MHz, Duty cycle \le 50%

Waveform 1. Load→Q, Data→Q

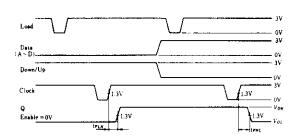


Note) Conditions on other inputs are irrelevant.

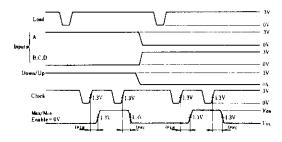
Waveform 2. G→Ripple CK, CK→Ripple CK, Down/Up→ Ripple CK, Down/Up→Max/Min

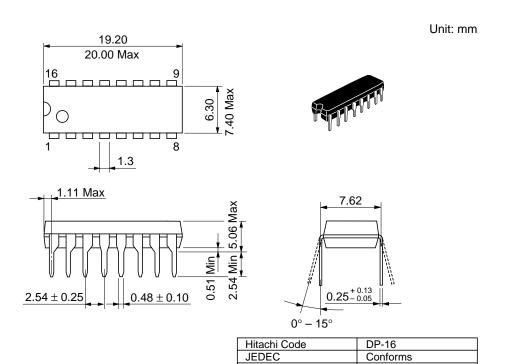


Waveform 3. Clock→Q



Waveform 4. Clock---Max/Min





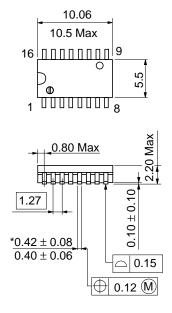
EIAJ

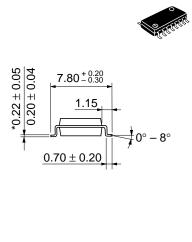
Weight (reference value) 1.07 g

Conforms

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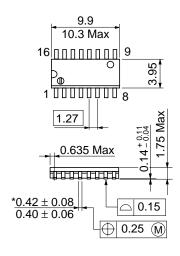


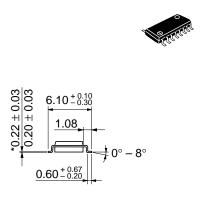
Hitachi Code	FP-16DA
JEDEC	
EIAJ	Conforms
Weight (reference value)	0.24 g

*Dimension including the plating thickness
Base material dimension

查询"HD74LS191"供应商

Unit: mm





Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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