Precision 8-Channel/Dual 4-Channel CMOS Analog Multiplexers

DESCRIPTION

The DG508B is an 8-channel single-ended analog multiplexer designed to connect one of eight inputs to a common output as determined by a 3-bit binary address (A0, A1, A2). The DG509B is a dual 4-channel differential analog multiplexer designed to connect one of four differential inputs to a common dual output as determined by its 2-bit binary address (A0, A1). Break-before-make switching action protects against momentary crosstalk between adjacent channels.

An on channel conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches off for stacking several devices. All control inputs, addresses (Ax) and enable (EN) are TTL compatible over the full specified operating temperature range.

The DG508B and DG509B are fabricated on an enhanced SG-II CMOS process that achieves improved performance on: reduced charge injection, lower device leakage, and minimized parasitic capacitance.

As the DG508, DG509 has a long history in the industry with many suppliers offering copies - and in some cases improved variations - with the best in class improvements, the Vishay Siliconix new version of the DG508B, DG509B are the superior alternatives to what is currently available.

Applications for the DG508B, DG509B include high speed and high precision data acquisition, audio signal switching and routing, ATE systems, and avionics. High performance and low power dissipation make them ideal for battery operated and remote instrumentation applications.

The DG508B and DG509B have the absolute maximum voltage rating extended to 44 V. Additionally, single supply operation is also allowed. An epitaxial layer prevents latch-up.

The DG508B and DG509B are both available in 16-lead SOIC, TSSOP, and PDIP package options with extended temperature range of - 40 °C to + 125 °C.

For more information, refer to Vishay Siliconix DG508B, DG509B evaluation board note.

FEATURES

Pb-free
RoHS COMPLIANT
HALOGEN FREE

- Operate with single or dual power supply
- V+ to V- analog signal swing range
- 44 V power supply maximum rating
- Extended operate temperature range:
  - 40 °C to + 125 °C
- Low leakage typically < 3 pA
- Low charge injection - Q_{INJ} = 2 pC
- Low power - I_{SUPPLY}: 10 µA
- TTL compatible logic
- > 250 mA latch up current per JESD78
- Available in SOIC16, TSSOP16, and PDIP16 packages
- Superior alternative to:
  - ADG508A, DG508A, HI-508
  - ADG509A, DG509A, HI-509
- Compliant to RoHS directive 2002/95/EC
- Halogen-free according to IEC 61249-2-21 definition

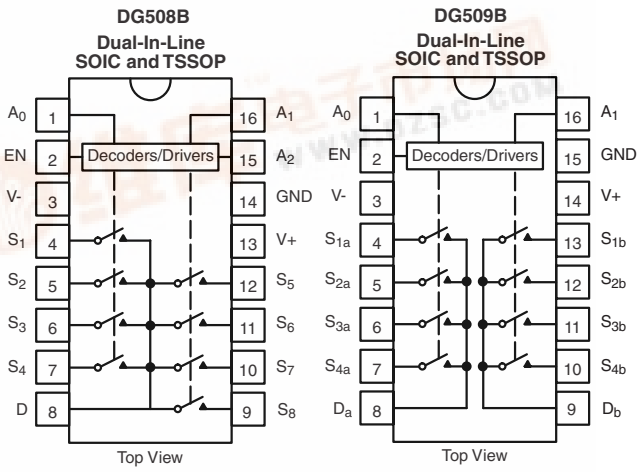
BENEFITS

- Reduced switching errors
- Reduced glitching
- Improved data throughput
- Reduced power consumption
- Increased ruggedness
- Wide supply ranges (± 5 V to ± 20 V)

APPLICATIONS

- Data acquisition systems
- Audio and video signal routing
- ATE systems
- Medical instrumentation

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLES AND ORDERING INFORMATION

TRUTH TABLE DG508B

A_2	A_1	A_0	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

TRUTH TABLE DG509B

A_1	A_0	EN	On Switch
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Logic "0" = $V_{IL} \leq 0.8$ V
Logic "1" = $V_{IH} \geq 2.0$ V
X = Do not care

ORDERING INFORMATION DG508B

Temp. Range	Package	Part Number
- 40 °C to 125 °C[a]	16-Pin SOIC	DG508BEY-T1-E3
	16-Pin TSSOP	DG508BEQ-T1-E3
	16-Pin PDIP	DG508BEJ-E3

ORDERING INFORMATION DG509B

Temp. Range	Package	Part Number
- 40 °C to 125 °C[a]	16-Pin SOIC	DG509BEY-T1-E3
	16-Pin TSSOP	DG509BEQ-T1-E3
	16-Pin PDIP	DG509BEJ-E3

Notes:
a. - 40 °C to 85 °C datasheet limits apply.

ABSOLUTE MAXIMUM RATINGS

Parameter		Limit	Unit
Voltages Referenced to V-	V+	44	V
	GND	25	
Digital Inputs[a], V_S, V_D		(V-) - 2 to (V+) + 2 or 20 mA, whichever occurs first	
Current (Any terminal)		30	mA
Peak Current, S or D (Pulsed at 1 ms, 10 % duty cycle max.)		100	
Storage Temperature	(EY, EQ, EJ suffix)	- 65 to 150	°C
Power Dissipation (Packages)[b]	16-Pin Narrow SOIC[c]	640	mW
	16-Pin TSSOP[d]	450	
	16-Pin PDIP[e]	501	
Thermal Resistance (θ_{J-A})[b]	16-Pin Narrow SOIC[c]	125	°C/W
	16-Pin TSSOP[d]	178	
	16-Pin PDIP[e]	159.6	

Notes:
a. Signals on S_X, D_X or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads soldered or welded to PC board.
c. Derate 8.0 mW/°C above 70 °C.
d. Derate 5.6 mW/°C above 70 °C.
e. Derate 6.3 mW/°C above 70 °C

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = - 15 V (± 10 %) V_{AX}, V_{EN} = 2.0 V, 0.8 V[a]		Temp.[b]	Typ.[c]	- 40 °C to 125 °C Min.[d]	- 40 °C to 125 °C Max.[d]	- 40 °C to 85 °C Min.[d]	- 40 °C to 85 °C Max.[d]	Unit
Analog Switch										
Analog Signal Range[e]	V_{ANALOG}			Full		- 15	15	- 15	15	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_D = ± 10 V, I_S = - 1 mA		Room	180		380		380	Ω
				Full			480		450	
$R_{DS(on)}$ Matching	$\Delta R_{DS(on)}$	V_D = ± 10 V		Room	10					
Source Off Leakage Current	$I_{S(off)}$	V_D = ± 10 V, V_S = ∓ 10 V, V_{EN} = 0 V		Room		- 1	1	- 1	1	nA
				Full		- 50	50	- 50	50	
Drain Off Leakage Current	$I_{D(off)}$		DG508B	Room		- 1	1	- 1	1	
				Full		- 100	100	- 100	100	
			DG509B	Room		- 1	1	- 1	1	
				Full		- 50	50	- 50	50	
Drain On Leakage Current	$I_{D(on)}$	$V_S = V_D$ = ∓ 10 sequence each switch on	DG508B	Room		- 1	1	- 1	1	
				Full		- 100	100	- 100	100	
			DG509B	Room		- 1	1	- 1	1	
				Full		- 50	50	- 50	50	
Digital Control										
Logic High Input Voltage	V_{INH}			Full		2.0		2.0		V
Logic Low Input Voltage	V_{INL}			Full			0.8		0.8	
Logic High Input Current	I_{IH}	V_{AX}, V_{EN} = 2.0 V		Full		- 1	1	- 1	1	µA
Logic Low Input Current	I_{IL}	V_{AX}, V_{EN} = 0.8 V		Full		- 1	1	- 1	1	
Logic Input Capacitance[e]	C_{in}	f = 1 MHz		Room	4					pF
Dynamic Characteristics										
Transition Time	t_{TRANS}	VS_1 = + 10 V/- 10 V, VS_8 = - 10 V/+ 10 V, R_L = 1 MΩ, C_L = 35 pF		Room	145		300		300	ns
				Full			400		400	
Break-Before-Make Interval	t_{OPEN}	$VS_1 = VS_8$ = 5.0 V, C_L = 35 pF, R_L = 1 kΩ		Room	37	15		15		
				Full		1		1		
Enable Turn-On Time	$t_{ON(EN)}$	VS_1 = 5 V, VS_2 to VS_8 = 0 V, R_L = 1 kΩ, C_L = 35 pF		Room	100		250		250	
				Full			340		340	
Enable Turn-Off Time	$t_{OFF(EN)}$			Room	90		240		240	
				Full			300		300	
Charge Injection[e]	Q_{INJ}	C_L = 1 nF, R_{GEN} = 0 Ω, V_{GEN} = 0 V		Full	2					pC
Off Isolation[e]	OIRR	C_L = 5 pF, R_L = 50 Ω, f = 1 MHz		Room	- 81					dB
Crosstalk[e]	XTALK			Room	- 88					
- 3 dB Bandwidth[e]	BW	R_L = 50 Ω		Room	250					MHz
Total Harmonic Distortion[e]	THD	R_L = 10 kΩ, 5 V_{rms} f = 20 Hz to 20 kHz		Room	0.04					%
Source Off Capacitance[e]	$C_{S(off)}$	f = 1 MHz		Room	3					pF
Drain Off Capacitance[e]	$C_{D(off)}$		DG508B	Room	13					
			DG509B	Room	8					
Drain On Capacitance[e]	$C_{D(on)}$		DG508B	Room	18					
			DG509B	Room	11					
Power Supply										
Positive Supply Current	I+	V_{AX}, V_{EN} = 0 V or V+		Room	0.01		0.5		0.5	mA
				Full			0.6		0.6	
Negative Supply Current	I-			Full		- 200		- 200		µA

SPECIFICATIONS Single Supply 12 V										
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V- = 0 V (± 10 %) V_{AX}, V_{EN} = 2.0 V, 0.8 V[a]		Temp.[b]	Typ.[c]	- 40 °C to 125 °C Min.[d]	- 40 °C to 125 °C Max.[d]	- 40 °C to 85 °C Min.[d]	- 40 °C to 85 °C Max.[d]	Unit
Analog Switch										
Analog Signal Range[e]	V_{ANALOG}			Full		0	12	0	12	V
On-Resistance	$R_{DS(on)}$	V_D = 10 V/0 V, I_S = 1 mA		Room	265		500		500	Ω
				Full			650		600	
$R_{DS(on)}$ Matching	$\Delta R_{DS(on)}$			Room	10					
Switch Off Leakage Current	$I_{S(off)}$	V+ = 12 V, V- = 0 V, V_D = 0 V/10 V, V_S = 10 V/0 V		Room		- 1	1	- 1	1	nA
				Full		- 50	- 50	- 50	50	
	$I_{D(off)}$		DG508B	Room		- 1	1	- 1	1	
				Full		- 100	100	- 100	100	
	$I_{D(off)}$		DG509B	Room		- 1	1	- 1	1	
				Full		- 50	50	- 50	50	
Channel On Leakage Current	$I_{D(on)}$	V+ = 12 V, V- = 0 V, V_S = V_D = 0 V/10 V	DG508B	Room		- 1	1	- 1	1	
				Full		- 100	100	- 100	100	
			DG509B	Room		- 1	1	- 1	1	
				Full		- 50	50	- 50	50	
Digital Control										
Logic High Input Voltage	V_{INH}			Full		2.0		2.0		V
Logic Low Input Voltage	V_{INL}			Full			0.8		0.8	
Logic High Input Current	I_{IH}	V_{AX}, V_{EN} = 2.0 V		Full		- 1	1	- 1	1	µA
Logic Low Input Current	I_{IL}	V_{AX}, V_{EN} = 0.8 V		Full		- 1	1	- 1	1	
Logic Input Capacitance[e]	C_{in}	f = 1 MHz		Room	4					pF
Dynamic Characteristics										
Transition Time	t_{TRANS}	VS_1 = 10 V/0 V, VS_8 = 0 V/10 V, R_L = 1 MΩ, C_L = 35 pF		Room	165		400		400	ns
				Full			550		500	
Break-Before-Make Interval	t_{OPEN}	VS_1 = VS_8 = 5 V, C_L = 35 pF, R_L = 1 kΩ		Room	37	15		15		
				Full		1		1		
Enable Turn-On Time	$t_{ON(EN)}$	VS_1 = 5 V, VS_2 to VS_8 = 0 V, R_L = 1 kΩ, C_L = 35 pF		Room	125		300		300	
				Full			550		425	
Enable Turn-Off Time	$t_{OFF(EN)}$			Room	75		250		250	
				Full			350		300	
Charge Injection[e]	Q_{INJ}	C_L = 1 nF, R_{GEN} = 0 Ω, V_{GEN} = 0 V		Full	2.5					pC
Off Isolation[e]	OIRR	C_L = 5 pF, R_L = 50 Ω, f = 1 MHz		Room	- 80					dB
Crosstalk[e]	X_{TALK}			Room	- 88					
- 3 dB Bandwidth[e]	BW	R_L = 50 Ω		Room	200					MHz
Total Harmonic Distortion[e]	THD	R_L = 10 kΩ, 5 V_{RMS}, f = 20 Hz to 20 kHz		Room	0.26					%

SPECIFICATIONS Single Supply 12 V										
		Test Conditions Unless Otherwise Specified V+ = 12 V, V- = 0 V (± 10 %) V_{AX}, V_{EN} = 2.0 V, 0.8 V[a]				- 40 °C to 125 °C		- 40 °C to 85 °C		
Parameter	**Symbol**			**Temp.[b]**	**Typ.[c]**	**Min.[d]**	**Max.[d]**	**Min.[d]**	**Max.[d]**	**Unit**
Source Off Capacitance[e]	$C_{S(off)}$	f = 1 MHz		Room	2					pF
Drain Off Capacitance[e]	$C_{D(off)}$		DG508B		13					
			DG509B		8					
Channel On Capacitance[e]	$C_{D(on)}$		DG508B		17					
			DG509B		12					
Power Supply										
Power Supply Current	I+	V_{AX}, V_{EN} = 0 V, or V+		Room	0.01		0.5		0.5	mA
				Full			0.6		0.6	

Notes:
a. V_{AX}, V_{EN} = input voltage perform proper function.
b. Room = 25 °C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. $\Delta R_{DS(on)} = R_{DS(on)}$ max. - $R_{DS(on)}$ min.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SCHEMATIC DIAGRAM Typical Channel

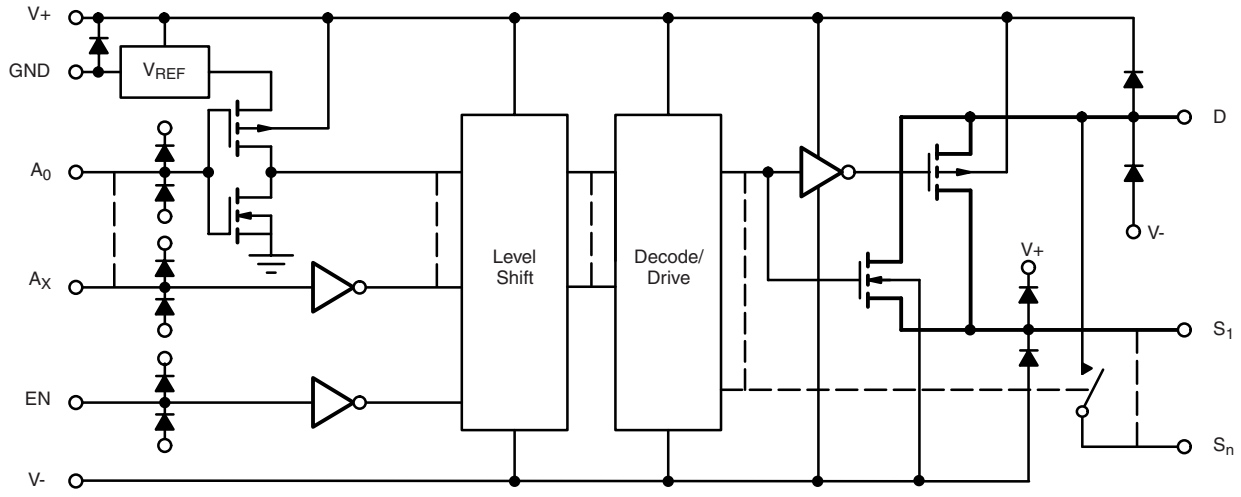
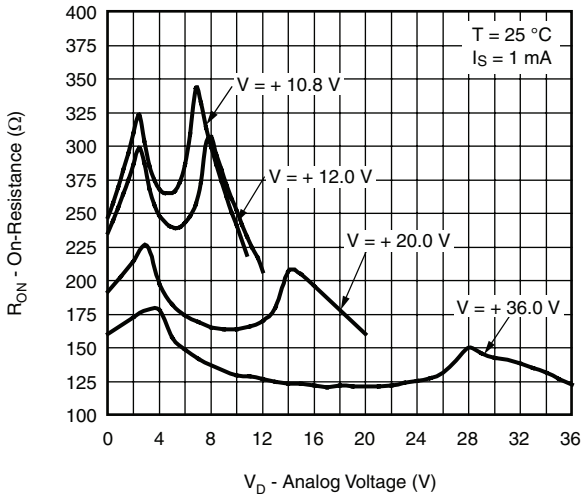
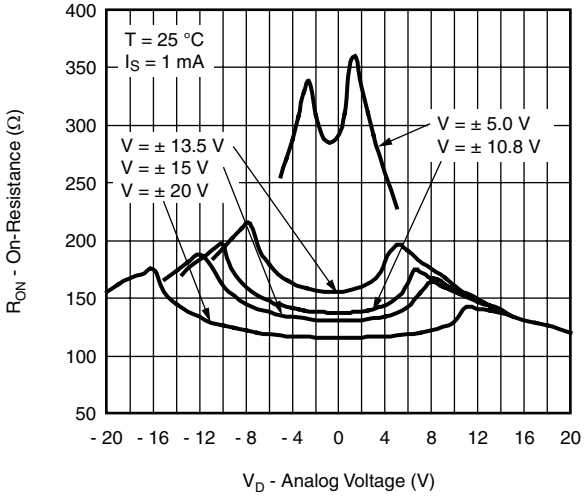


Figure 1.

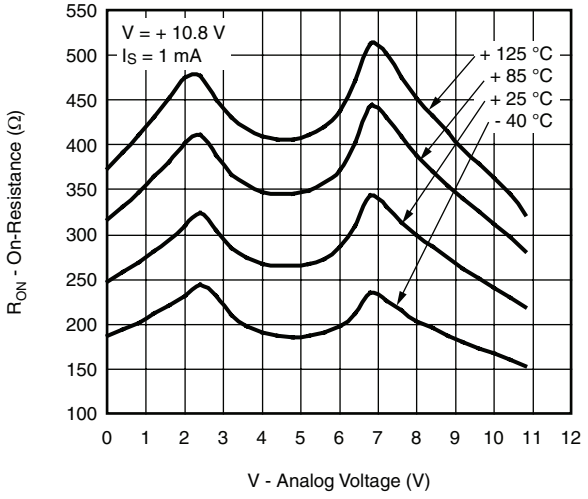
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



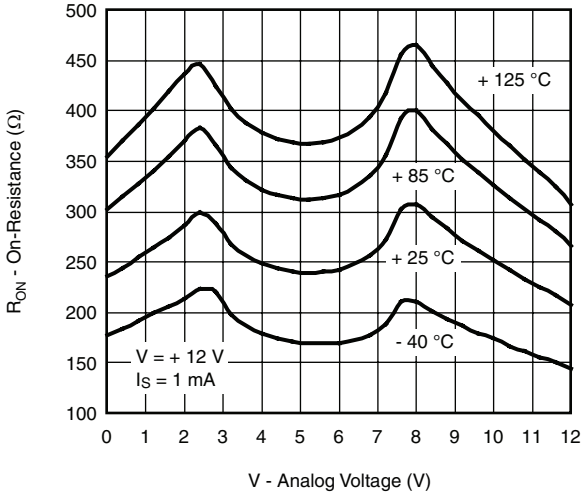
On-Resistance vs. V_D and Single Supply Voltage



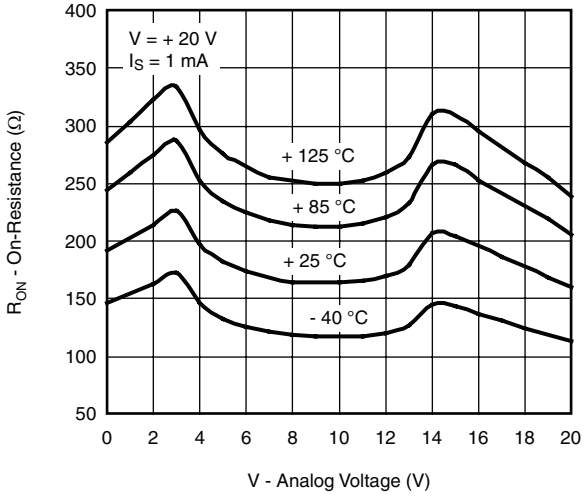
On-Resistance vs. V_D and Dual Supply Voltage



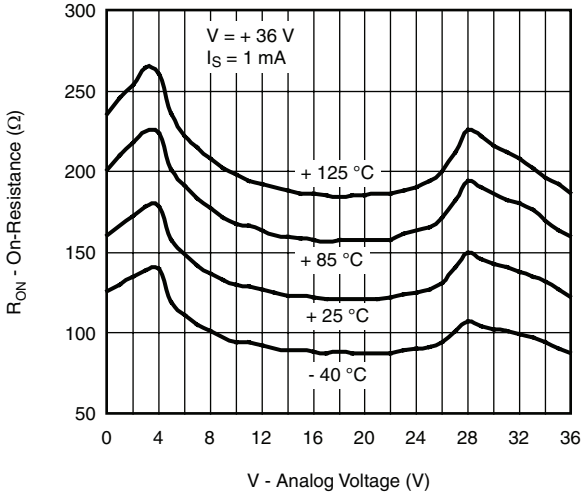
On-Resistance vs. Analog Voltage and Temperature



On-Resistance vs. Analog Voltage and Temperature

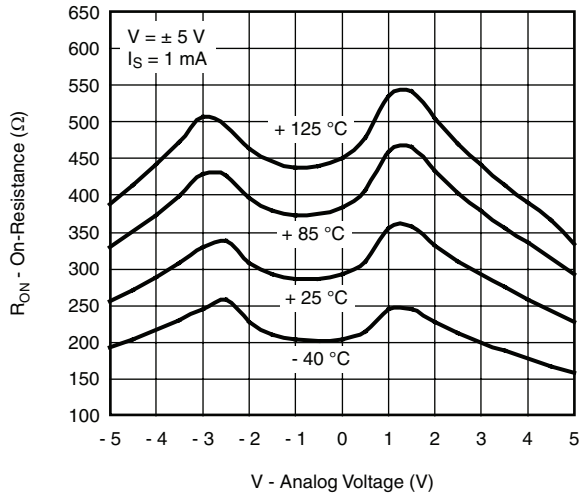


On-Resistance vs. Analog Voltage and Temperature

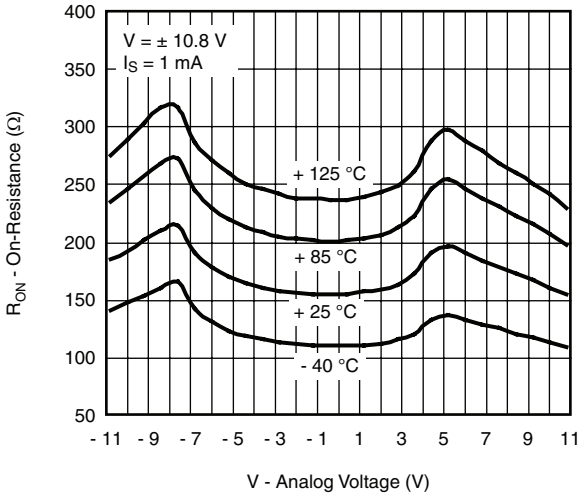


On-Resistance vs. Analog Voltage and Temperature

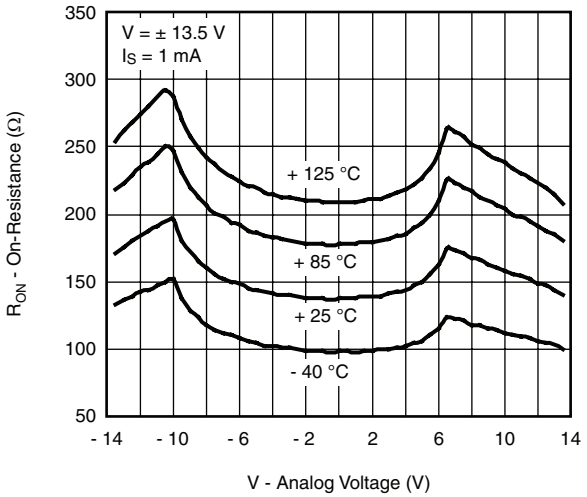
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



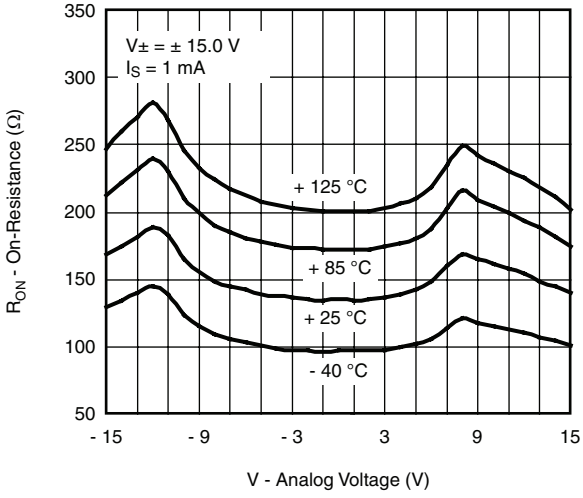
On-Resistance vs. Analog Voltage and Temperature



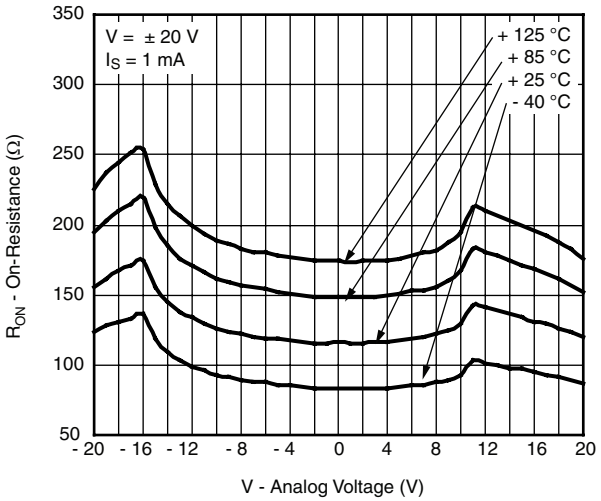
On-Resistance vs. Analog Voltage and Temperature



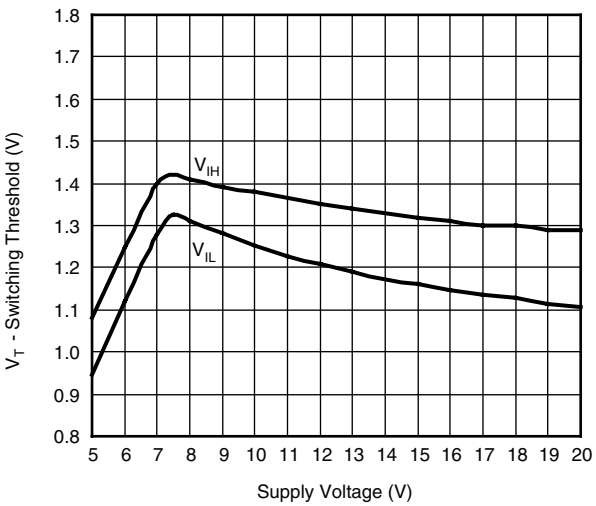
On-Resistance vs. Analog Voltage and Temperature



On-Resistance vs. Analog Voltage and Temperature

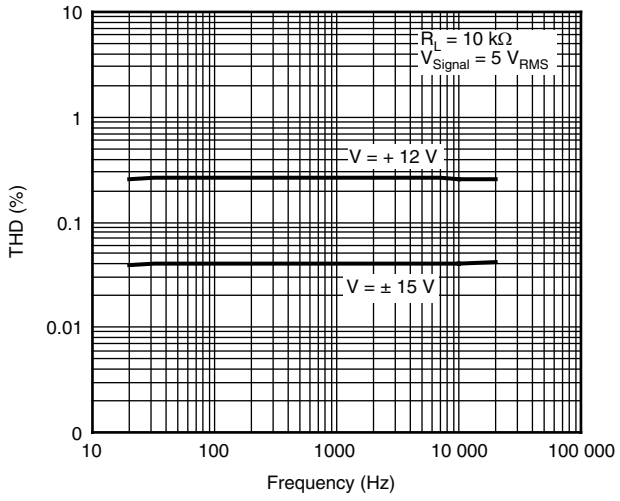


On-Resistance vs. Analog Voltage and Temperature

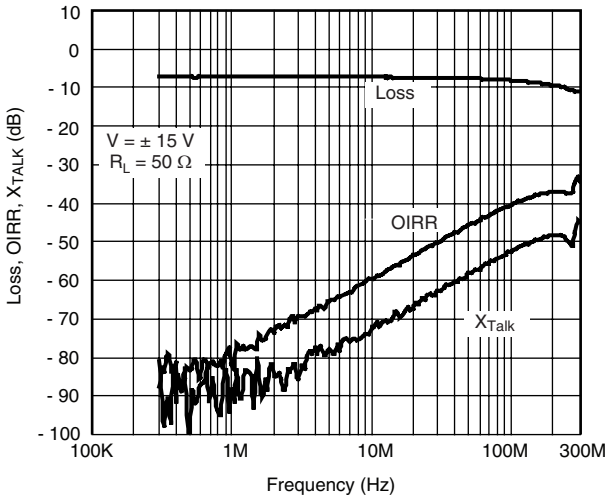


Switching Threshold vs. Supply Voltage

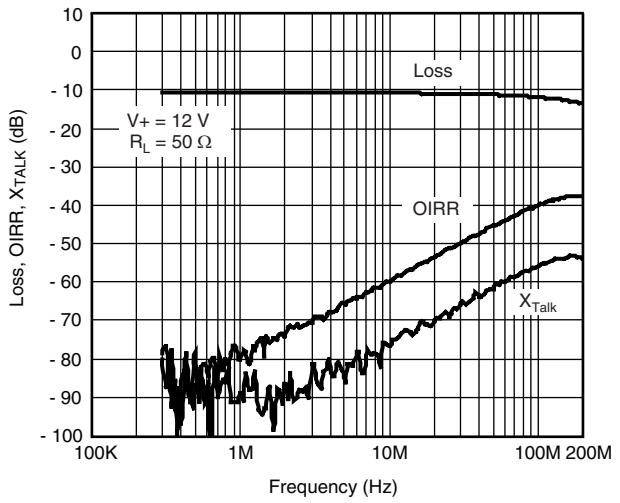
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



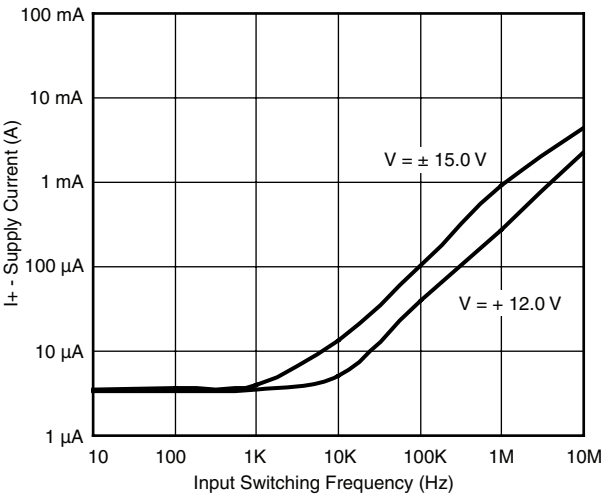
THD vs. Frequency



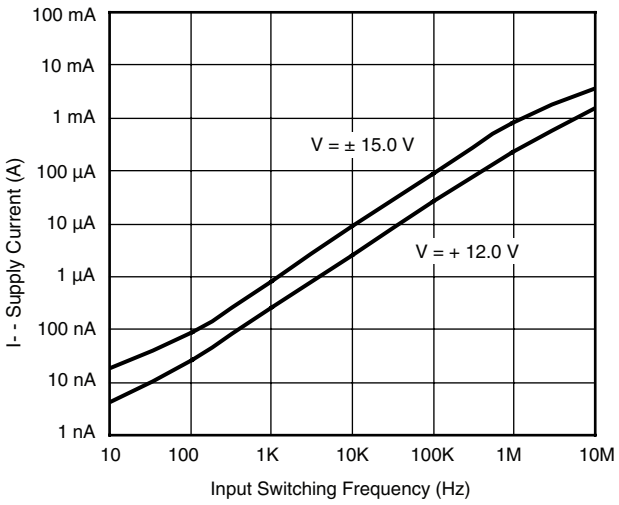
Insertion Loss, Off-Isolation, Crosstalk vs. Frequency



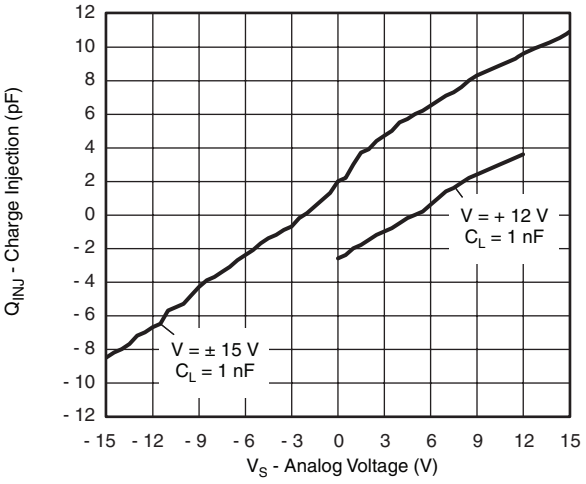
Insertion Loss, Off-Isolation, Crosstalk vs. Frequency



Supply Current vs. Input Switching Frequency

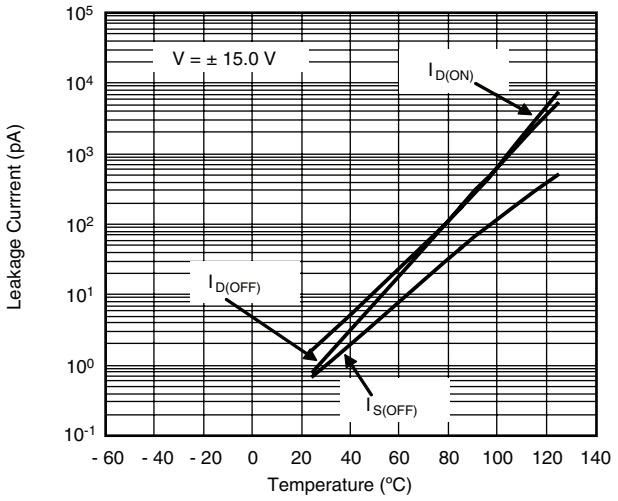


Supply Current vs. Input Switching Frequency

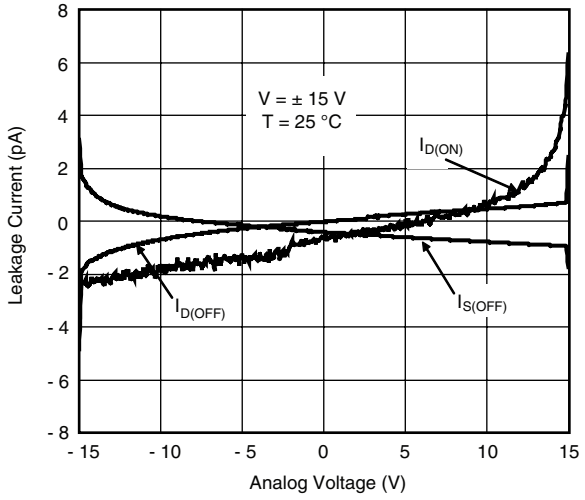


Charge Injection vs. Analog Voltage

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

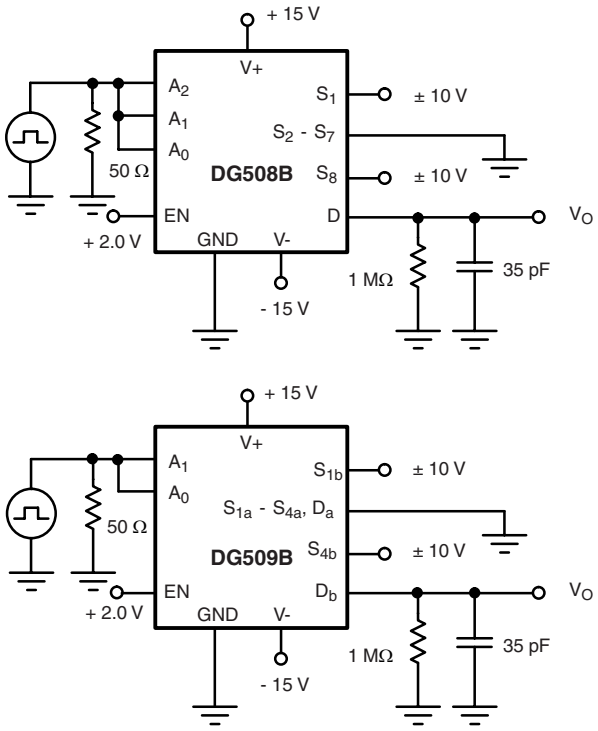


Leakage Current vs. Temperature



Leakage Current vs. Analog Voltage

TEST CIRCUITS



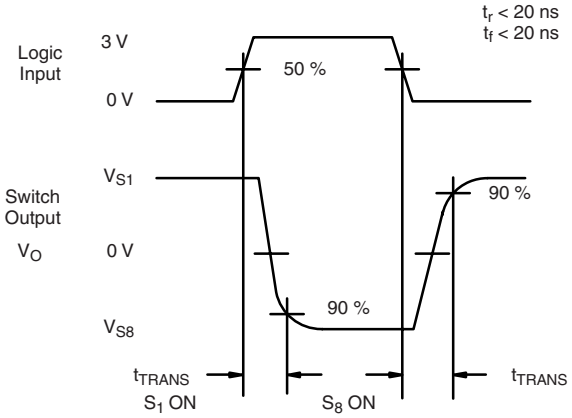


Figure 2. Transition Time

TEST CIRCUITS

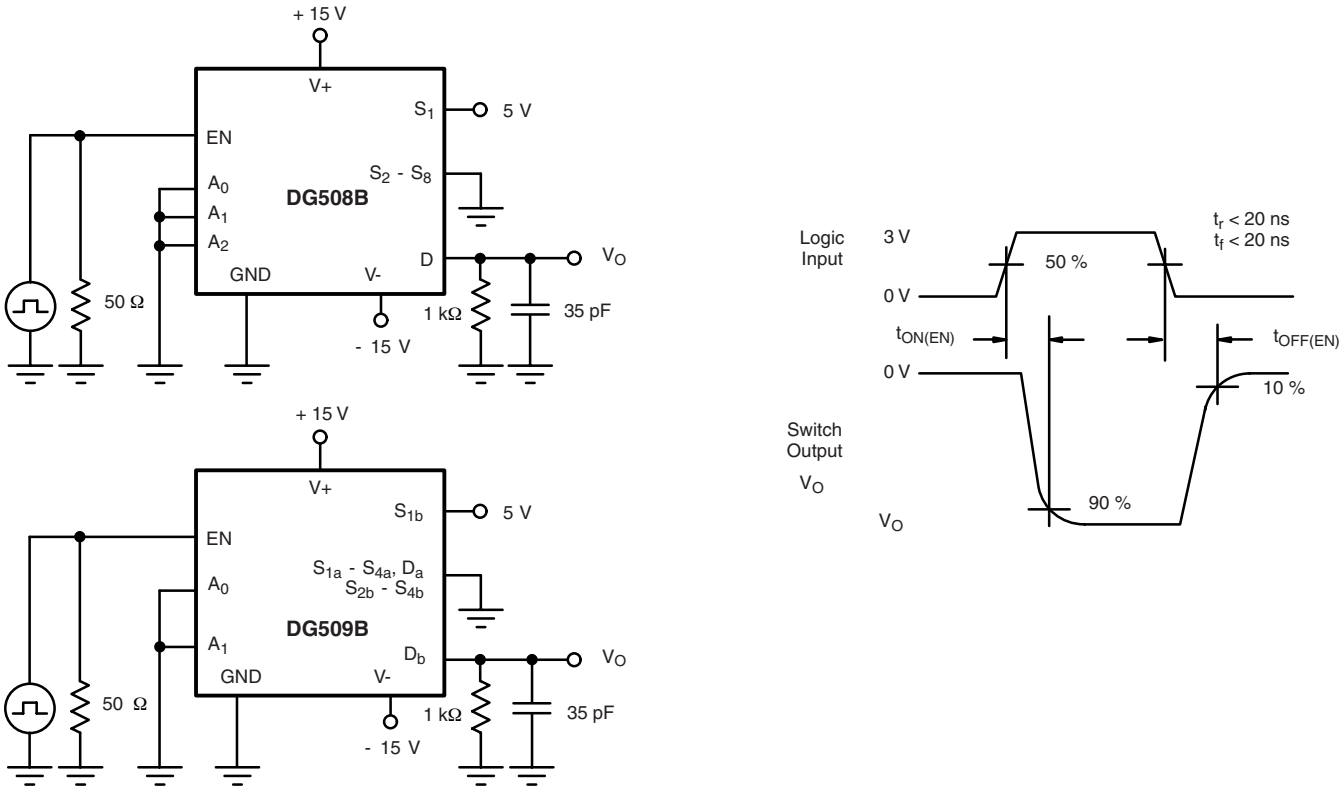


Figure 3. Enable Switching Time

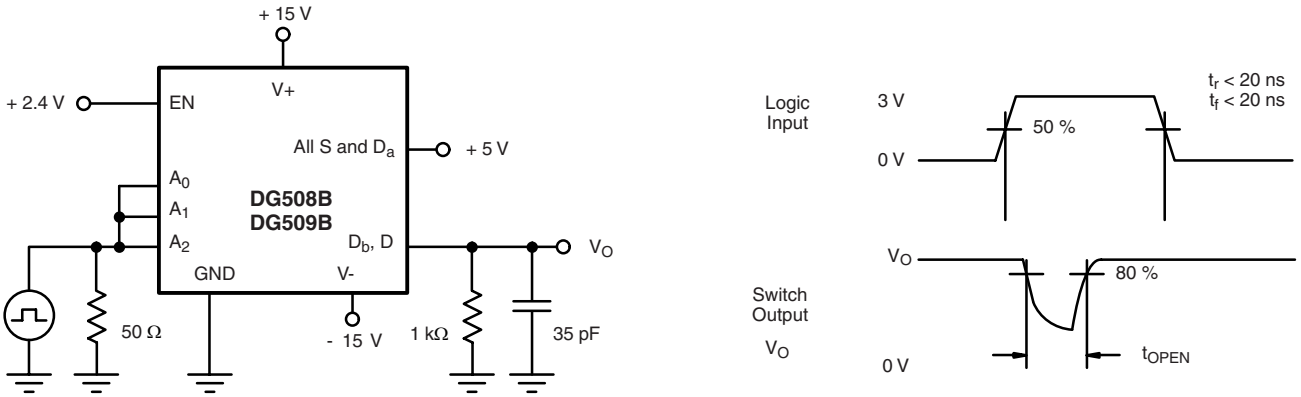


Figure 4. Break-Before-Make Interval

TEST CIRCUITS

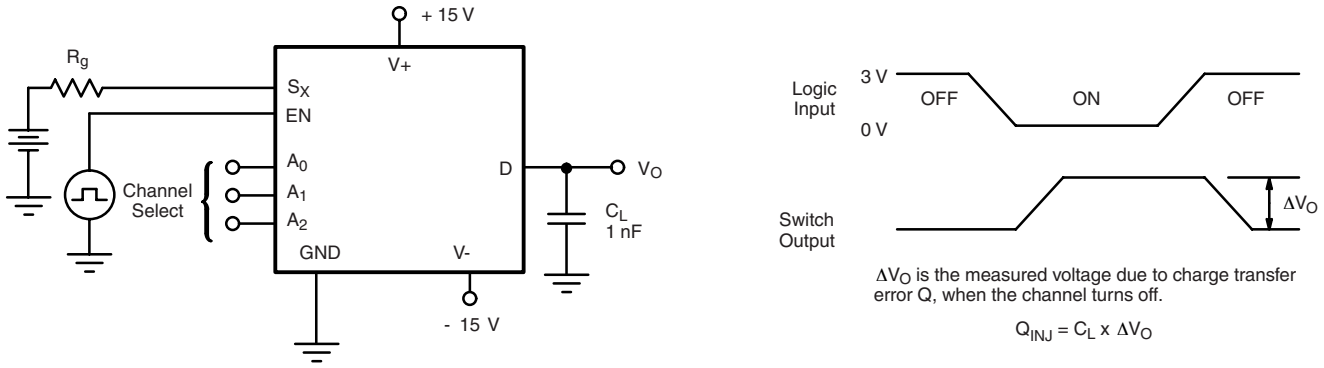


Figure 5. Charge Injection

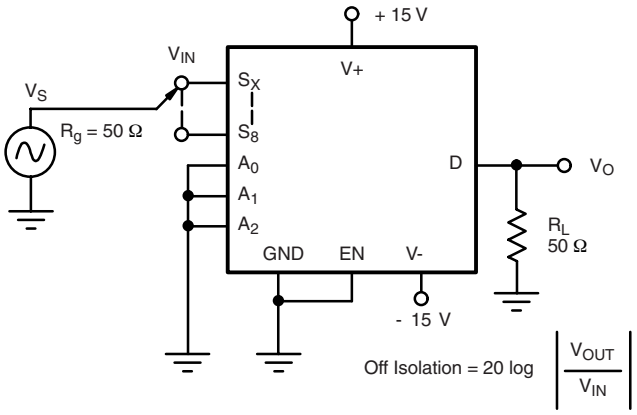


Figure 6. Off Isolation

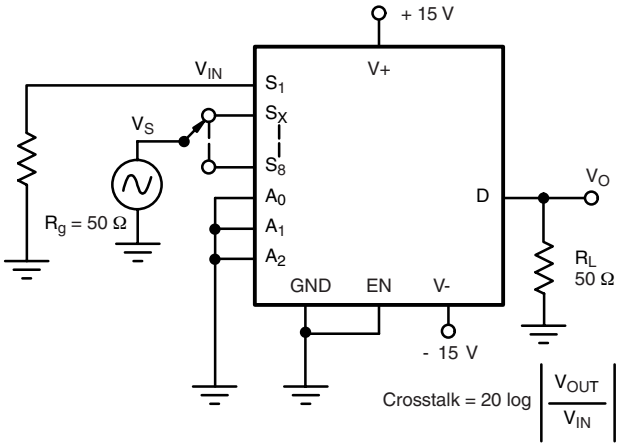


Figure 7. Crosstalk

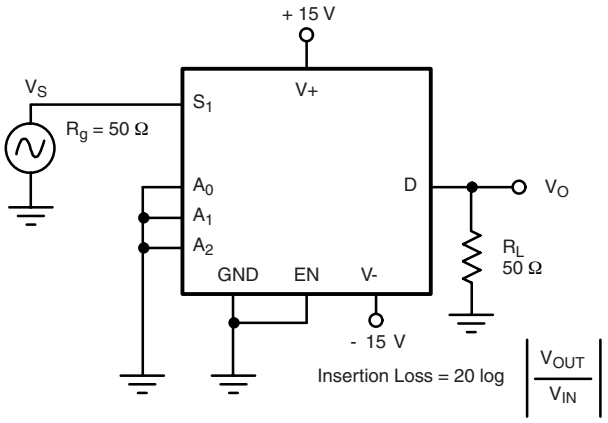


Figure 8. Insertion Loss

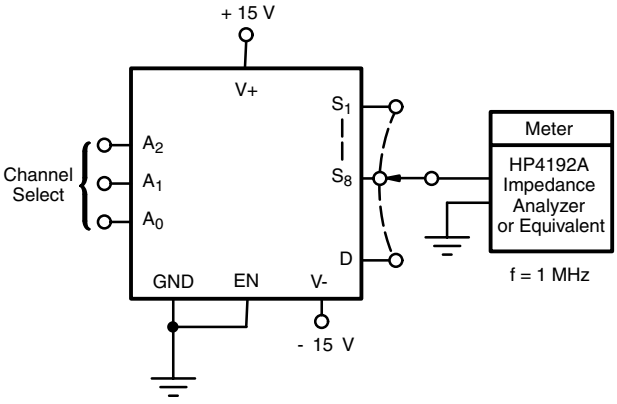


Figure 9. Source Drain Capacitance

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