M2118 FAMILY
16,384 x 1 BIT DYNAMIC RAM

MILITARY

	M2118-4	M2118-7
Maximum Access Time (ns)	120	150
Read, Write Cycle (ns)	270	320
Read-Modify Cycle (ns)	320	410

- **Single +5V Supply, ±10% Tolerance**
- **HMOS Technology**
- **Low Power: 150 mW Max. Operating**
  11 mW Max. Standby
- **Low V_{DD} Current Transients**
- **All Inputs, Including Clocks, TTL Compatible**
- **$\overline{CAS}$ Controlled Output is Three-State, TTL Compatible**
- **$\overline{RAS}$ Only Refresh**
- **128 Refresh Cycles Required Every 2ms**
- **Allows Negative Overshoot V_{IL} min = −2V**
- **Military Temperature Range −55° to +85°C (T_C)**
- **Not Recommended for New Designs**

The Intel® M2118 is a 16,384 word by 1-bit Dynamic MOS RAM designed to operate from a single +5V power supply. The M2118 is fabricated using HMOS—a production proven process for high performance, high reliability, and high storage density.

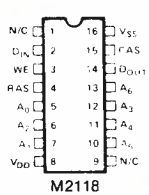
The M2118 uses a single transistor dynamic storage cell and advanced dynamic circuitry to achieve high speed with low power dissipation. The circuit design minimizes the current transients typical of dynamic RAM operation. These low current transients contribute to the high noise immunity of the M2118 in a system environment.

Multiplexing the 14 address bits into the 7 address input pins allows the M2118 to be packaged in the industry standard 16-pin DIP. The two 7-bit address words are latched into the M2118 by the two TTL clocks, Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). Non-critical timing requirements for $\overline{RAS}$ and $\overline{CAS}$ allow use of the address multiplexing technique while maintaining high performance.

The M2118 three-state output is controlled by $\overline{CAS}$, independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is latched on the output by holding $\overline{CAS}$ low. The data out pin is returned to the high impedance state by returning $\overline{CAS}$ to a high state.

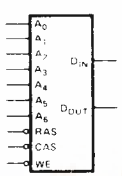
The single transistor storage cell requires refreshing for data retention. Refreshing is accomplished by performing $\overline{RAS}$-only refresh cycles, or normal read or write cycles on the 128 address combinations of A_0 through A_6 during a 2ms period. A write cycle will refresh stored data on all bits of the selected row except the bit which is addressed.

PIN CONFIGURATION



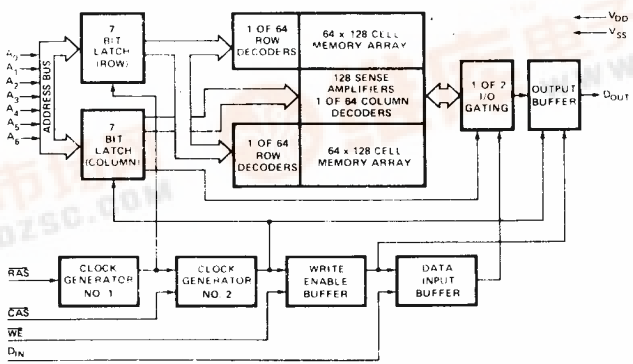
M2118

LOGIC SYMBOL



A_0-A_6	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{WE}$	WRITE ENABLE
$\overline{RAS}$	ROW ADDRESS STROBE
V_{DD}	POWER (+5V)
V_{SS}	GROUND

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Case Temperature Under Bias ..... −65°C to +95°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin Relative to V_{SS} 7.5V
Data Out Current 50mA
Power Dissipation 1.0W

*COMMENT:
Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS [1]

T_C[4] = −55°C to +85°C, V_{DD} = 5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits Min	Typ [2]	Max	Unit	Test Conditions	Notes
$\|I_{LI}\|$	Input Load Current (any input)		0.1	10	µA	V_{IN}=V_{SS} to V_{DD}	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State		0.1	10	µA	Chip Deselected: $\overline{CAS}$ at V_{IH}, V_{OUT} = 0 to 5.5V	
I_{DD1}	V_{DD} Supply Current, Standby		1.2	2	mA	$\overline{CAS}$ and $\overline{RAS}$ at V_{IH}	
I_{DD2}	V_{DD} Supply Current, Operating		21	25	mA	M2118-4, t_{RC} = t_{RCMIN}	3
			19	23	mA	M2118-7, t_{RC} = t_{RCMIN}	3
I_{DD3}	V_{DD} Supply Current; $\overline{RAS}$-Only Cycle		14	16	mA	M2118-4, t_{RC} = t_{RCMIN}	3
			12	14	mA	M2118-7, t_{RC} = t_{RCMIN}	3
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled		2	4	mA	$\overline{CAS}$ at V_{IL}, $\overline{RAS}$ at V_{IH}	3
V_{IL}	Input Low Voltage (all inputs)	-2.0		0.8	V		
V_{IH}	Input High Voltage (all inputs)	2.4		7.0	V		
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.2mA	
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -5mA	

NOTES:
1. All voltages referenced to V_{SS}.
2. Typical values are for T_A = 25°C and nominal supply voltages.
3. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DDMAX} is measured with the output open.
4. Case temperatures are "instant on."

CAPACITANCE [1]

T_C[2] = 25°C, V_{DD} = 5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Typ	Max	Unit
C_{I1}	Address, Data In	3	5	pF
C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, Data Out	4	7	pF

NOTES:
1. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation:
$C = \frac{I\Delta t}{\Delta V}$ with ΔV equal to 3 volts and power supplies at nominal levels.
2. Case temperatures are "instant on."

A.C. CHARACTERISTICS [1,2,3]

T_C[10] = −55°C to +85°C, V_{DD} = 5V ±10%, V_{SS} = 0V, unless otherwise noted. 1.

READ, WRITE, READ-MODIFY-WRITE AND REFRESH CYCLES

Symbol	Parameter	M2118-4 Min.	M2118-4 Max.	M2118-7 Min.	M2118-7 Max.	Unit	Notes
t_{RAC}	Access Time From $\overline{RAS}$		120		150	ns	4,5
t_{CAC}	Access Time From $\overline{CAS}$		65		80	ns	4,5,6
t_{REF}	Time Between Refresh		2		2	ms	
t_{RP}	$\overline{RAS}$ Precharge Time	120		135		ns	
t_{CPN}	$\overline{CAS}$ Precharge Time(non-page cycles)	55		70		ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0		0		ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	55	25	70	ns	7
t_{RSH}	$\overline{RAS}$ Hold Time	85		105		ns	
t_{CSH}	$\overline{CAS}$ Hold Time	120		165		ns	
t_{ASR}	Row Address Set-Up Time	0		0		ns	
t_{RAH}	Row Address Hold Time	15		15		ns	
t_{ASC}	Column Address Set-Up Time	0		0		ns	
t_{CAH}	Column Address Hold Time	15		20		ns	
t_{AR}	Column Address Hold Time, to $\overline{RAS}$	70		90		ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{OFF}	Output Buffer Turn Off Delay	0	50	0	60	ns	

READ AND REFRESH CYCLES

t_{RC}	Random Read Cycle Time	270		320		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	140	10000	175	10000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	65	10000	95	10000	ns	
t_{RCS}	Read Command Set-Up Time	0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		ns	

WRITE CYCLE

t_{RC}	Random Write Cycle Time	270		320		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	140	10000	175	10000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	65	10000	95	10000	ns	
t_{WCS}	Write Command Set-Up Time	0		0		ns	9
t_{WCH}	Write Command Hold Time	30		45		ns	
t_{WCR}	Write Command Hold Time, to $\overline{RAS}$	85		115		ns	
t_{WP}	Write Command Pulse Width	30		50		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	65		110		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	50		100		ns	
t_{DS}	Data-In Set-Up Time	0		0		ns	
t_{DH}	Data-In Hold Time	30		45		ns	
t_{DHR}	Data-In Hold Time, to $\overline{RAS}$	85		115		ns	

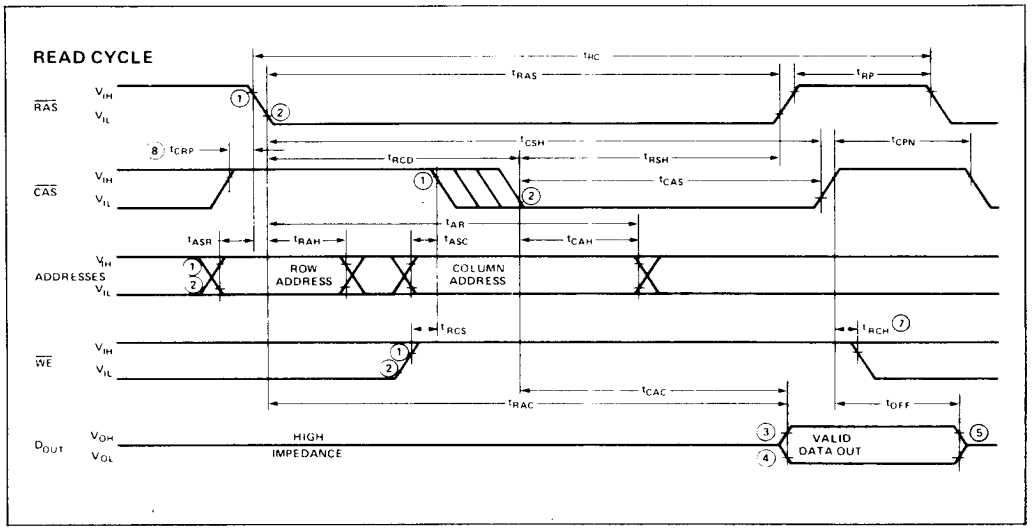
READ-MODIFY-WRITE CYCLE

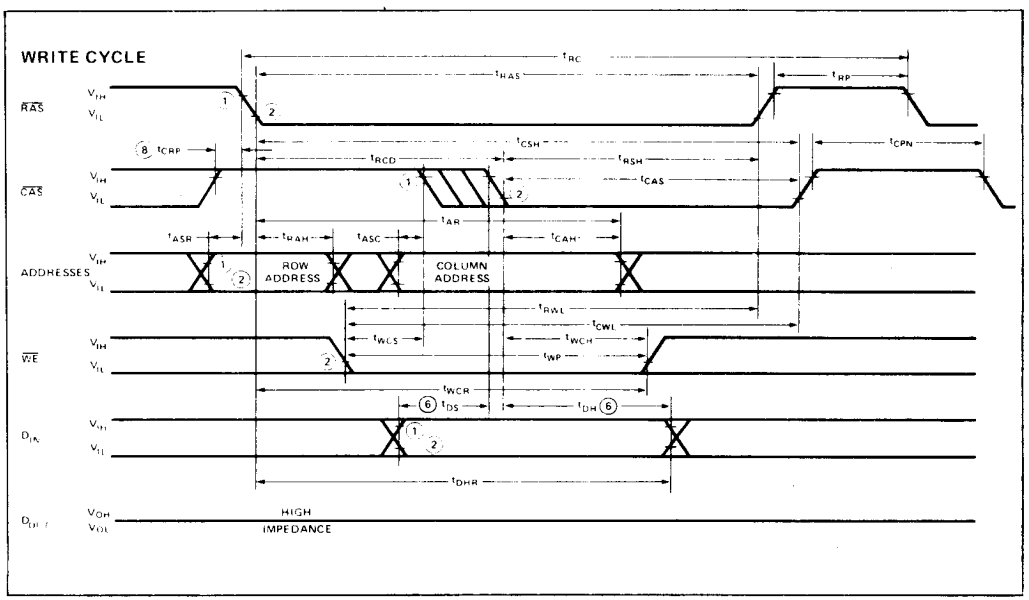
t_{RWC}	Read-Modify-Write Cycle Time	320		410		ns	
t_{RRW}	RMW Cycle $\overline{RAS}$ Pulse Width	190	10000	265	10000	ns	
t_{CRW}	RMW Cycle $\overline{CAS}$ Pulse Width	120	10000	185	10000	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	120		150		ns	9
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	65		80		ns	9

NOTES:

1. All voltages referenced to V_{SS}.
2. Eight cycles are required after power up or prolonged periods (greater than 2ms) of $\overline{RAS}$ inactivity before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
3. A.C. Characteristics assume t_T = 5ns.
4. Assume that $t_{RCD} \leq t_{RCD}$(max). If t_{RCD} is greater than t_{RCD} (max.) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
5. Load = 2 TTL loads and 100pF
6. Assumes $t_{RCD} \geq t_{RCD}$ (max.).
7. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is less than t_{RCD} (max.) access time is t_{RAC}. If t_{RCD} is greater than t_{RCD} (max.) access time is $t_{RCD} + t_{CAC}$.
8. t_T is measured between V_{IH} (min.) and V_{IL} (max.).
9. t_{WCS}, t_{CWD} and t_{RWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (min.) the cycle is an early write cycle and the data out pin will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} \geq t_{RWD}$ (min.), the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
10. Case temperatures are "instant on."

WAVEFORMS

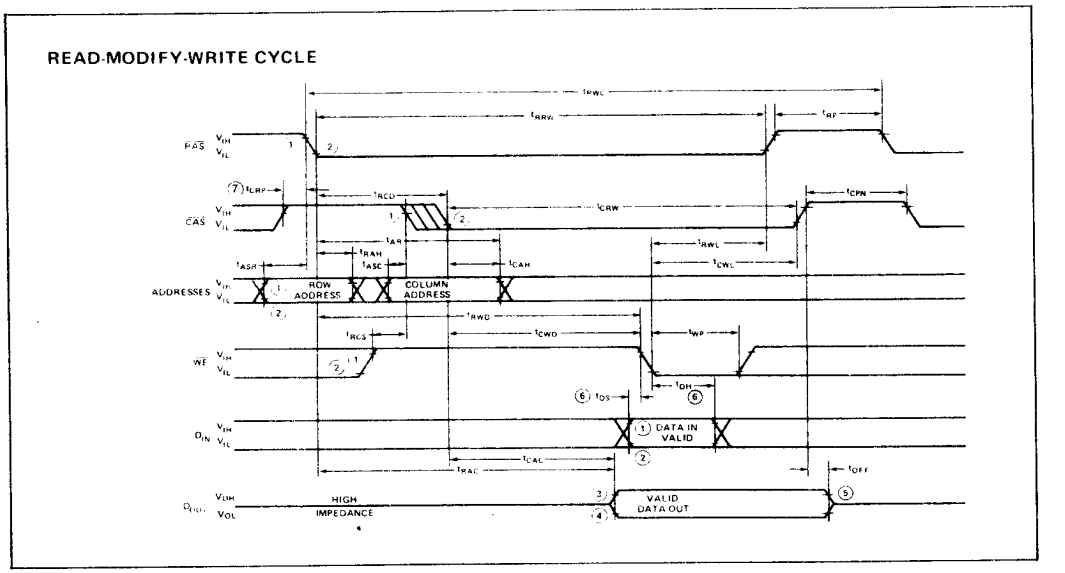




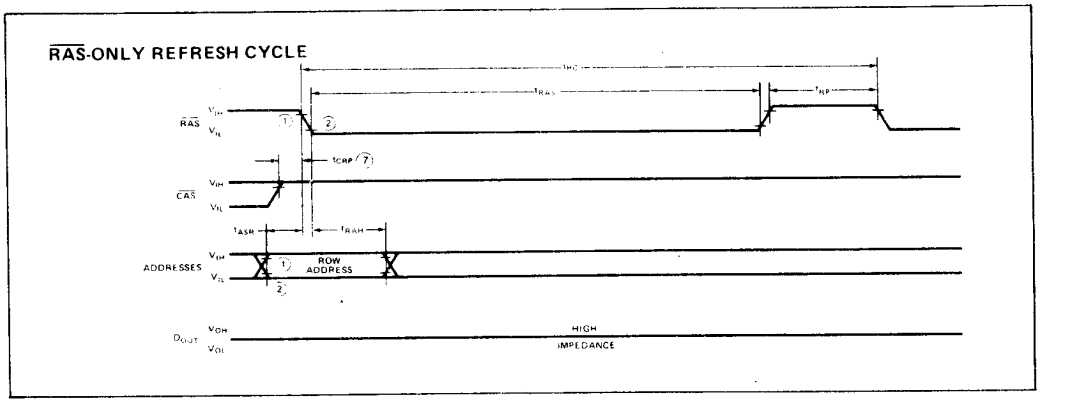
NOTES: 1,2 $V_{IH\ MIN}$ AND $V_{IL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF INPUT SIGNALS
3,4 $V_{OH\ MIN}$ AND $V_{OL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF D_{OUT}
5 t_{OFF} IS MEASURED TO $|I_{OUT}| \leq |I_{LO}|$
6 t_{DS} AND t_{DH} ARE REFERENCED TO $\overline{CAS}$ OR $\overline{WE}$, WHICHEVER OCCURS LAST
7 t_{RCH} IS REFERENCED TO THE TRAILING EDGE OF $\overline{CAS}$ OR $\overline{RAS}$, WHICHEVER OCCURS FIRST
8 t_{CRP} REQUIREMENT IS ONLY APPLICABLE FOR $\overline{RAS}$/$\overline{CAS}$ CYCLES PRECEEDED BY A $\overline{CAS}$ ONLY CYCLE (i.e., FOR SYSTEMS WHERE $\overline{CAS}$ HAS NOT BEEN DECODED WITH $\overline{RAS}$)

WAVEFORMS

READ-MODIFY-WRITE CYCLE



RAS-ONLY REFRESH CYCLE



NOTES: 1,2. $V_{IH\ MIN}$ AND $V_{IL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF INPUT SIGNALS.
3,4. $V_{OH\ MIN}$ AND $V_{OL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF D_{OUT}.
5. t_{OFF} IS MEASURED TO $I_{OUT} \leq |1|$.
6. t_{OS} AND t_{DH} ARE REFERENCED TO $\overline{CAS}$ OR $\overline{WE}$, WHICHEVER OCCURS LAST.
7. t_{CRP} REQUIREMENT IS ONLY APPLICABLE FOR $\overline{RAS}$/$\overline{CAS}$ CYCLES PRECEEDED BY A $\overline{CAS}$-ONLY CYCLE (i.e., FOR SYSTEMS WHERE $\overline{CAS}$ HAS NOT BEEN DECODED WITH $\overline{RAS}$).