24-BIT 192-kHz SAMPLING ENHANCED MULTI-LEVEL DELTA-SIGMA AUDIO DIGITAL-TO-ANALOG CONVERTER

Check for Samples: PCM1754-Q1

FEATURES

- Qualified for Automotive Applications
- 24-Bit Resolution
- Analog Performance (V_{CC} = 5 V)
  - Dynamic Range: 106 dB
  - SNR: 106 dB, Typical
  - THD+N: 0.002%, Typical
  - Full-Scale Output: 4 V_{PP}, Typical
- 4×/8× Oversampling Digital Filter
  - Stop-Band Attenuation: -50 dB
  - Pass-Band Ripple: ±0.04 dB
- Sampling Frequency: 5 kHz to 200 kHz
- System Clock: 128 f_S, 192 f_S, 256 f_S, 384 f_S, 512 f_S, 768 f_S, 1152 f_S with Auto Detect
- Hardware Control (PCM1754)
  - I^2S and 16-Bit Word, Right-Justified
  - 44.1 kHz Digital De-Emphasis
  - Soft Mute
  - Zero Flag for L-, R-Channel Common Output
- Power Supply: 5-V Single Supply
- Small 16-Lead SSOP Package, Lead-Free

APPLICATIONS

- A/V Receivers
- DVD Movie Players
- DVD Add-On Cards for High-End PCs
- DVD Audio Players
- HDTV Receivers
- Car Audio Systems
- Other Applications Requiring 24-Bit Audio

DESCRIPTION

The PCM1754 is a CMOS, monolithic, integrated circuit, which includes stereo digital-to-analog converters and support circuitry in a small 16-lead SSOP package. The data converters use TI's enhanced multilevel delta-sigma architecture, which employs 4th-order noise shaping and 8-level amplitude quantization to achieve excellent dynamic performance and improved tolerance to clock jitter. The PCM1754 accepts industry standard audio data formats with 16- to 24-bit data, providing easy interfacing to audio DSP and decoder chips. Sampling rates up to 200 kHz are supported. A full set of user-programmable functions is accessible through a three-wire serial control port, which supports register write functions.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 105°C	SSOP - DBQ	Reel of 2000	PCM1754TDBQRQ1	P1754Q

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

Supply voltage: V_{CC}	-0.3 V to 6.5 V
Ground voltage differences: AGND, DGND	±0.1 V
Input voltage	-0.3 V to 6.5 V
Input current (any pins except supplies)	±10 mA
Ambient temperature under bias	-40°C to 105°C
Storage temperature	-55°C to 150°C
Junction temperature	150°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

All specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 44.1 kHz, system clock = 384 f_S, and 24-bit data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution			24		Bits
DATA FORMAT						
	Audio-data interface format			I^2S, standard		
	Audio-data bit length			16-24-bit (I^2S), 16-bit (standard)		
	Audio data format			MSB first, 2s complement		
f_S	Sampling frequency		5		200	kHz
	System clock frequency			128 f_S, 192 f_S, 256 f_S, 384 f_S, 512 f_S, 768 f_S, 1152 f_S		
DIGITAL INPUT/OUTPUT						
	Logic family			TTL compatible		
V_{IH}	Input logic level		2			VDC
V_{IL}					0.8	VDC
I_{IH}(1)	Input logic current	$V_{IN} = V_{CC}$			10	µA
I_{IL}(1)		V_{IN} = 0 V			-10	µA
I_{IH}(2)		$V_{IN} = V_{CC}$		65	100	µA
I_{IL}(2)		V_{IN} = 0 V			-10	µA
V_{OH}(3)	Output logic level	I_{OH} = -1 mA	2.4			VDC
V_{OL}(3)		I_{OL} = 1 mA			0.4	VDC

(1) Pins 16, 1, 2, 3: SCK, BCK, DATA, LRCK
(2) Pins 12-15: TEST, DEMP, MUTE, FMT
(3) Pin 11: ZEROA

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 44.1 kHz, system clock = 384 f_S, and 24-bit data (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE(4)(5)					
THD+N at VOUT = 0 dB	f_S = 44.1 kHz		0.00%	0.01%	
	f_S = 96 kHz		0.00%		
	f_S = 192 kHz		0.00%		
THD+N at VOUT = -60 dB	f_S = 44.1 kHz		0.65%		
	f_S = 96 kHz		0.80%		
	f_S = 192 kHz		0.95%		
Dynamic range	EIAJ, A-weighted, f_S = 44.1 kHz	100	106		dB
	A-weighted, f_S = 96 kHz		104		
	A-weighted, f_S = 192 kHz		102		
Signal-to-noise ratio	EIAJ, A-weighted, f_S = 44.1 kHz	100	106		dB
	A-weighted, f_S = 96 kHz		104		
	A-weighted, f_S = 192 kHz		102		
Channel separation	f_S = 44.1 kHz	97	103		dB
	f_S = 96 kHz		101		
	f_S = 192 kHz		100		
Level linearity error	VOUT = -90 dB		±0.5		dB
DC ACCURACY					
Gain error			±1	±6	% of FSR
Gain mismatch, channel-to-channel			±1	±3	% of FSR
Bipolar zero error	VOUT = 0.5 V_{CC} at BPZ		±30	±60	mV
ANALOG OUTPUT					
Output voltage	Full scale (0 dB)	80% of V_{CC}			V_{PP}
Center voltage		50% of V_{CC}			VDC
Load impedance	AC-coupled load	5			kΩ
DIGITAL FILTER PERFORMANCE					
FILTER CHARACTERISTICS (SHARP ROLLOFF)					
Pass band	±0.04 dB			0.454 f_S	
Stop band		0.546 fs			
Pass-band ripple				±0.04	dB
Stop-band attenuation	Stop band = 0.546 f_S	-50			dB

(4) Analog performance specifications are measured using the System Two™ Cascade audio measurement system by Audio Precision™ in the averaging mode.
(5) Conditions in 192-kHz operation are system clock = 128 f_S and oversampling rate = 64 f_S of register 18.

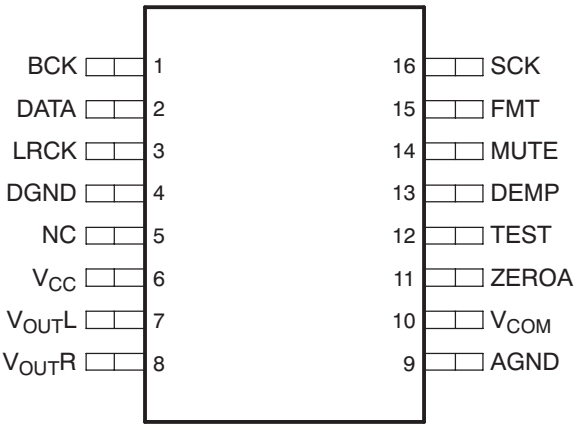
ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 44.1 kHz, system clock = 384 f_S, and 24-bit data (unless otherwise noted)

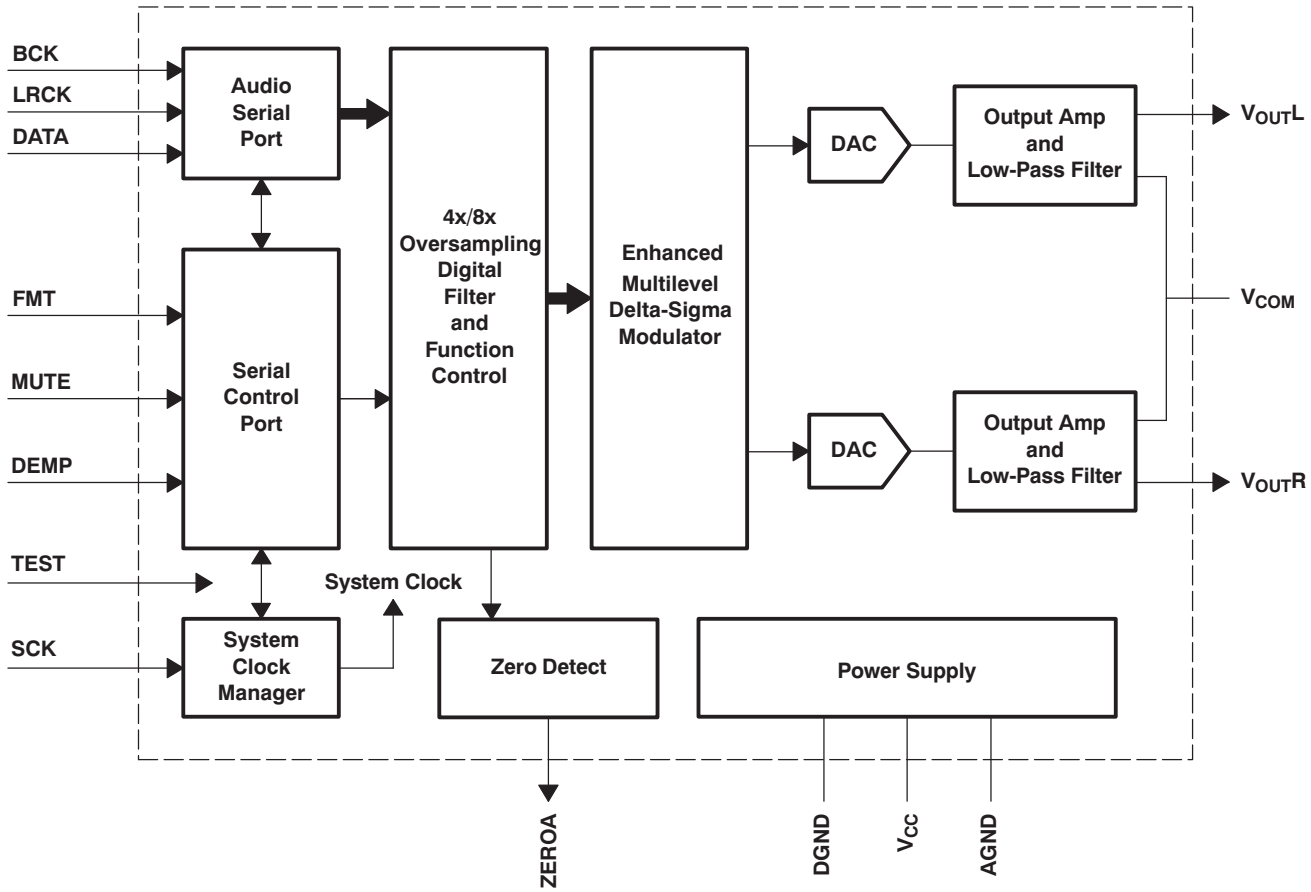
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG FILTER PERFORMANCE						
	Frequency response	At 20 kHz		-0.03		dB
		At 44 kHz		-0.20		
POWER SUPPLY REQUIREMENTS(6)						
V_{CC}	Voltage range		4.5	5	5.5	VDC
I_{CC}	Supply current	f_S = 44.1 kHz		16	21	mA
		f_S = 96 kHz		25		
		f_S = 192 kHz		30		
	Power dissipation	f_S = 44.1 kHz		80	105	mW
		f_S = 96 kHz		125		
		f_S = 192 kHz		150		
TEMPERATURE RANGE						
	Operation temperature		-40		105	°C
θ_{JA}	Thermal resistance	16-pin SSOP		115		°C/W

(6) Conditions in 192-kHz operation are system clock = 128 f_S and oversampling rate = 64 f_S of register 18.

DBQ PACKAGE
(TOP VIEW)



FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

NAME	NO.	I/O	DESCRIPTION
AGND	9	–	Analog ground
BCK	1	I	Audio–data bit–clock input
DATA	2	I	Audio–data digital input
DEMP	13	I	De–emphasis control(1)
DGND	4	–	Digital ground
FMT	15	I	Data format select(1)
LRCK	3	I	L–channel and R–channel audio data latch enable input
MUTE	14	I	Analog mixing control(1)
NC	5	–	No connection
SCK	16	I	System clock input
TEST	12	I	Test pin. Ground or open(1)
V_{CC}	6	–	Analog power supply, 5 V
V_{COM}	10	–	Common voltage decoupling
$V_{OUT}L$	7	O	Analog output for L–channel
$V_{OUT}R$	8	O	Analog output for R–channel
ZEROA	11	O	Zero flag output for L/R channels

(1) Schmitt-trigger input with internal pulldown

TYPICAL PERFORMANCE CURVES

All specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 44.1 kHz, system clock = 384 f_S, and 24-bit data, (unless otherwise noted)

DIGITAL FILTER (DE-EMPHASIS OFF)

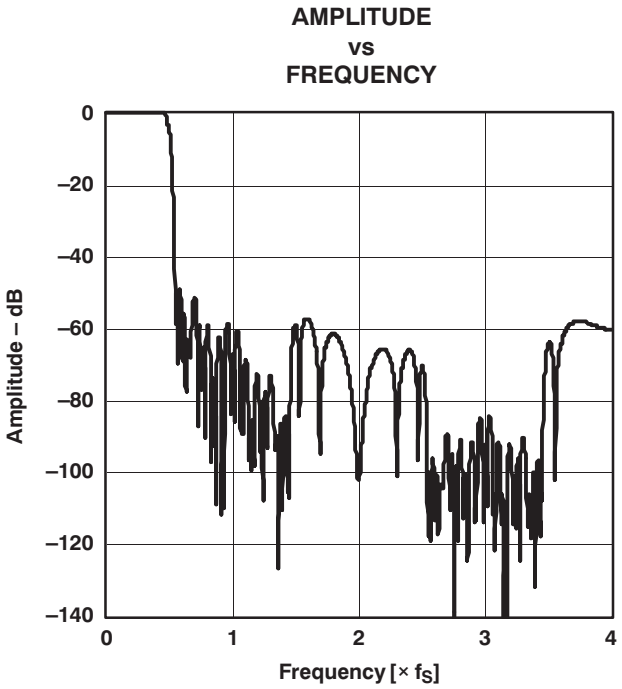


Figure 1. Frequency Response, Sharp Rolloff

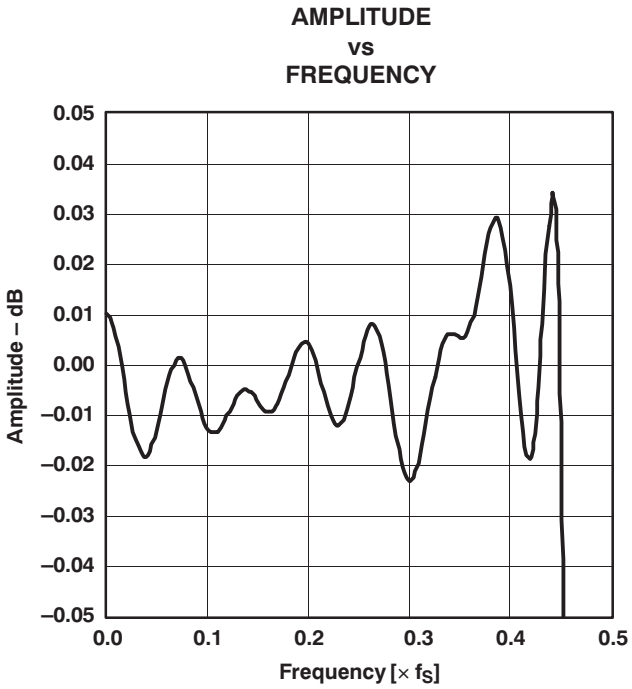


Figure 2. Pass-Band Ripple, Sharp Rolloff

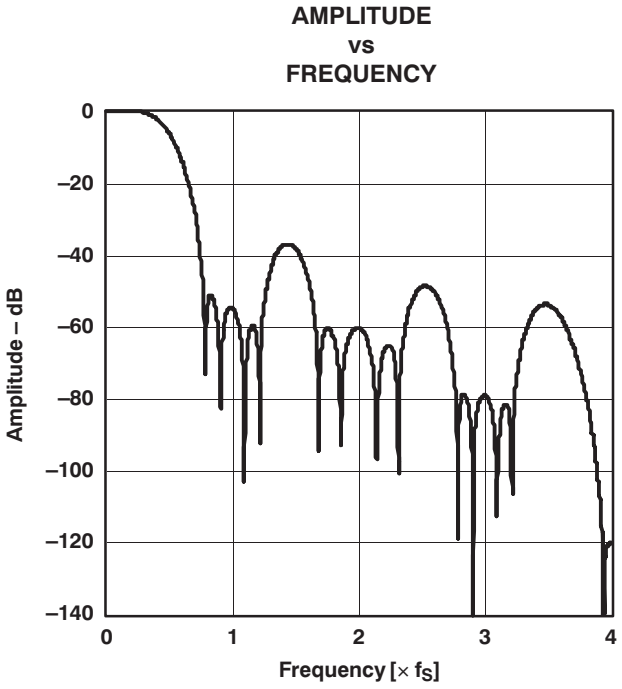


Figure 3. Frequency Response, Slow Rolloff

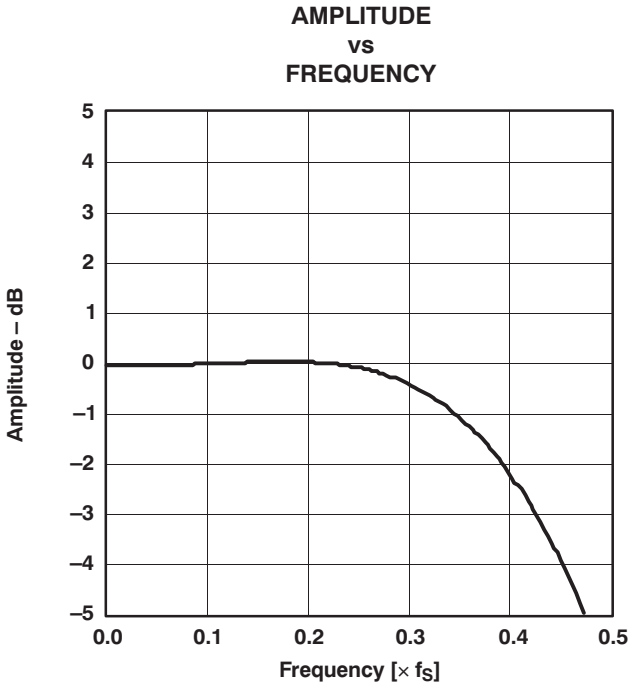


Figure 4. Transition Characteristics, Slow Rolloff

TYPICAL PERFORMANCE CURVES (continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 44.1 kHz, system clock = 384 f_S, and 24-bit data, (unless otherwise noted)

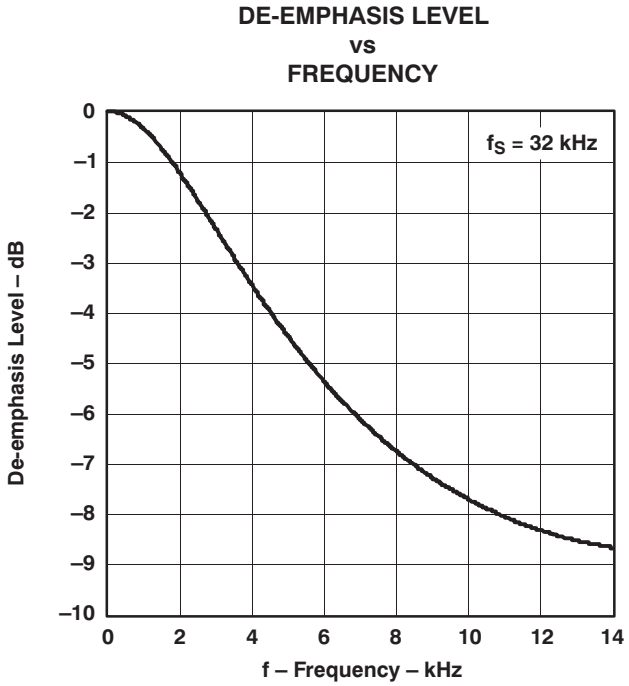


Figure 5.

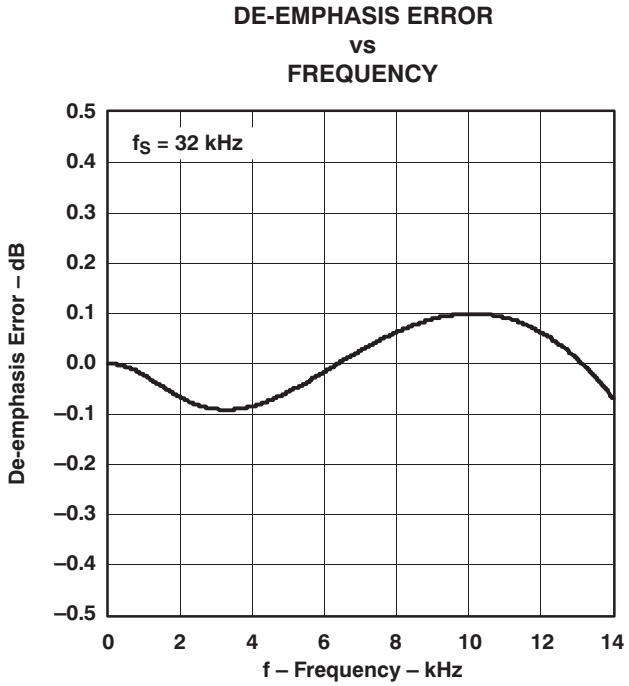


Figure 6.

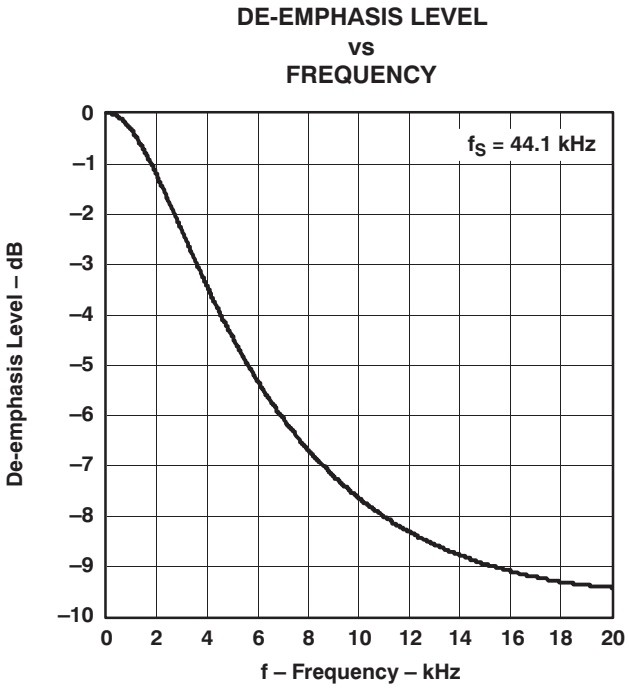


Figure 7.

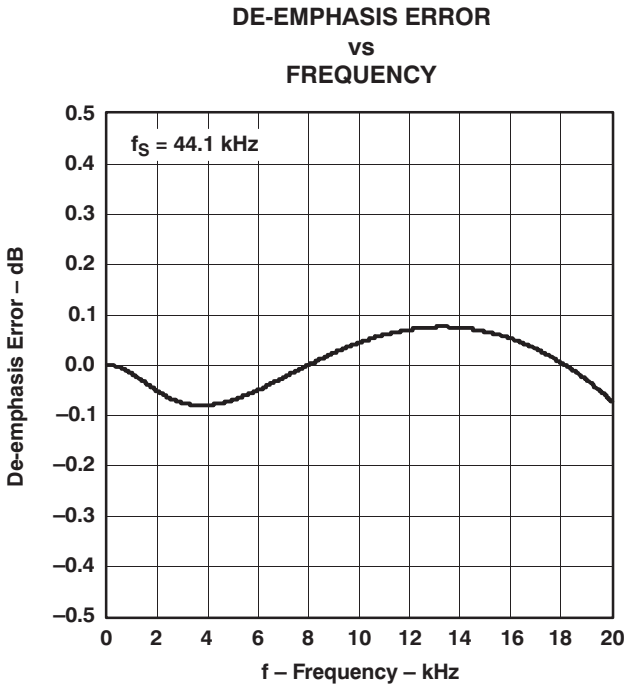


Figure 8.

TYPICAL PERFORMANCE CURVES (continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 44.1 kHz, system clock = 384 f_S, and 24-bit data, (unless otherwise noted)

DE-EMPHASIS LEVEL vs FREQUENCY

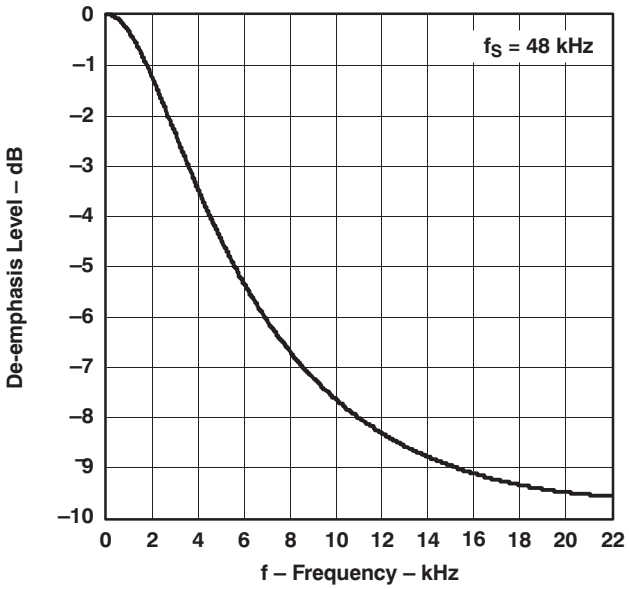


Figure 9.

DE-EMPHASIS ERROR vs FREQUENCY

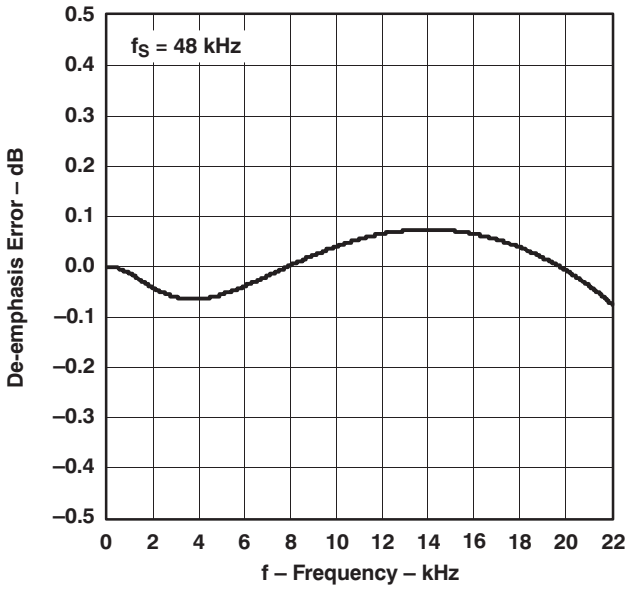


Figure 10.

TYPICAL PERFORMANCE CURVES (continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 44.1 kHz, system clock = 384 f_S, and 24-bit data, (unless otherwise noted)

ANALOG DYNAMIC PERFORMANCE (SUPPLY VOLTAGE CHARACTERISTICS)

TOTAL HARMONIC DISTORTION + NOISE vs SUPPLY VOLTAGE

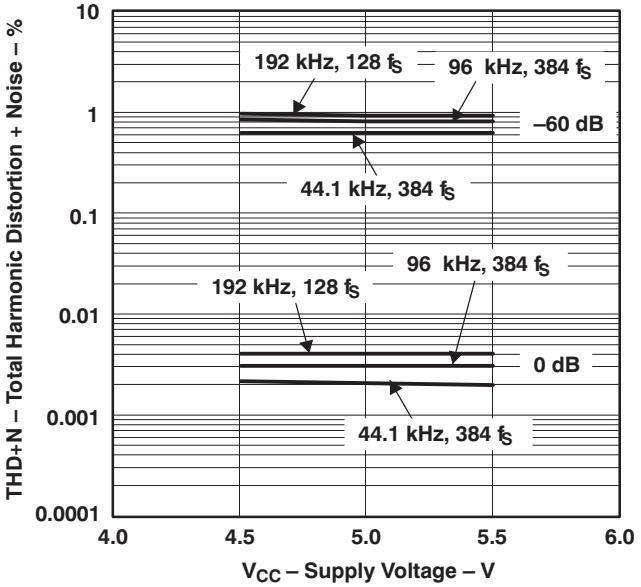


Figure 11.

DYNAMIC RANGE vs SUPPLY VOLTAGE

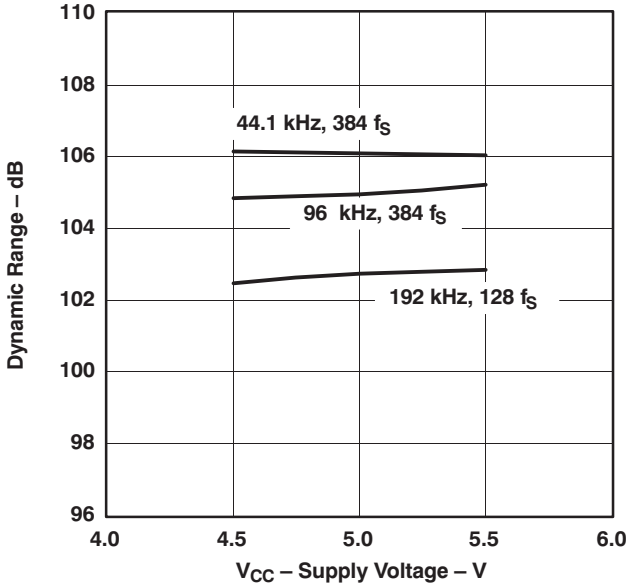


Figure 12.

SIGNAL-to-NOISE RATIO vs SUPPLY VOLTAGE

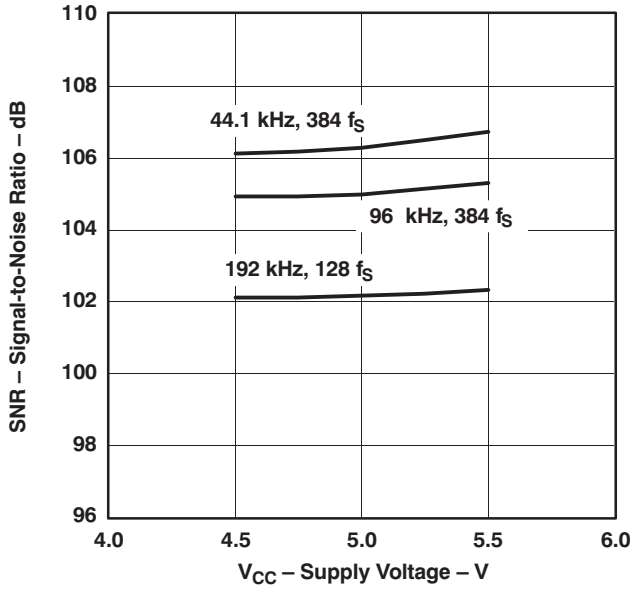


Figure 13.

CHANNEL SEPARATION vs SUPPLY VOLTAGE

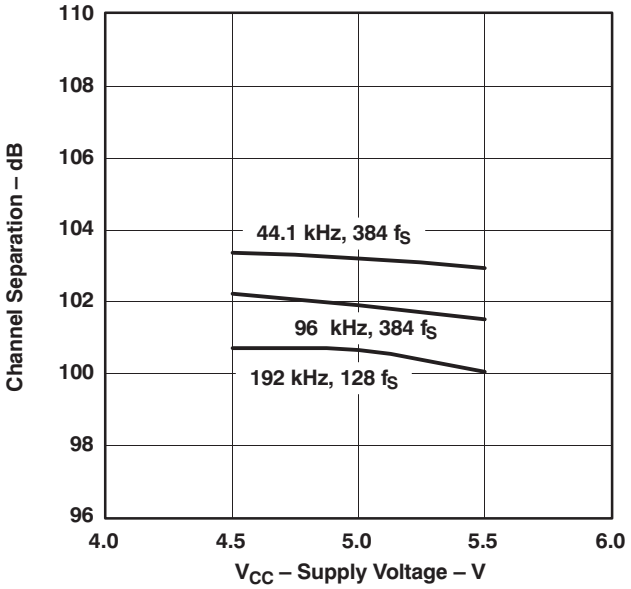


Figure 14.

TYPICAL PERFORMANCE CURVES (continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 44.1 kHz, system clock = 384 f_S, and 24-bit data, (unless otherwise noted)

ANALOG DYNAMIC PERFORMANCE (TEMPERATURE CHARACTERISTICS)

TOTAL HARMONIC DISTORTION + NOISE vs FREE-AIR TEMPERATURE

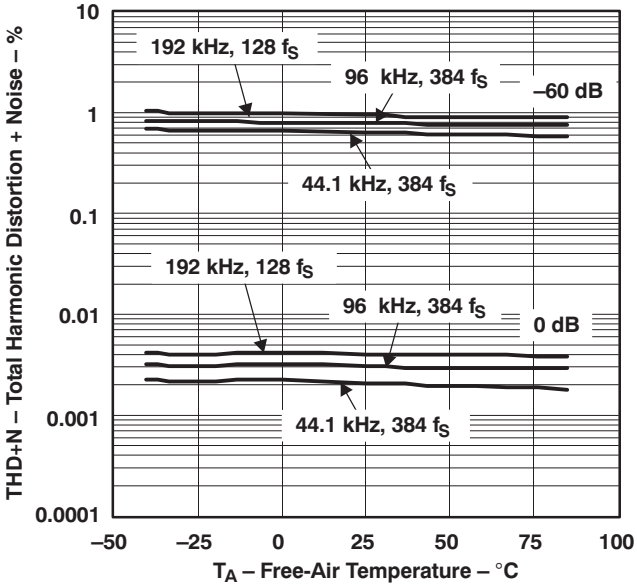


Figure 15.

DYNAMIC RANGE vs FREE-AIR TEMPERATURE

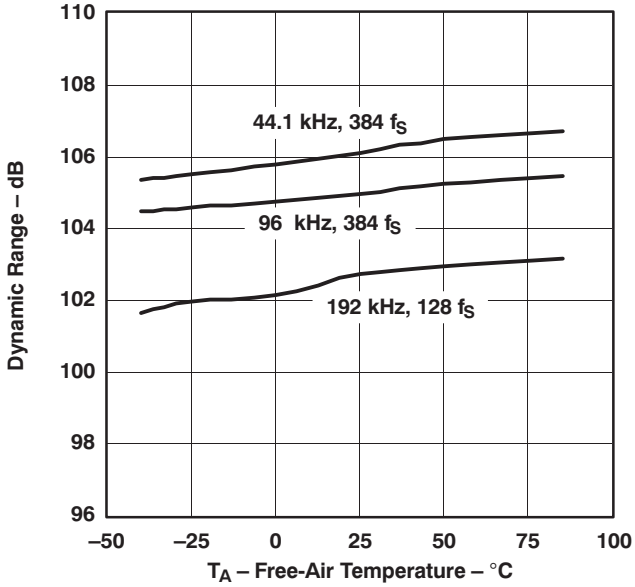


Figure 16.

SIGNAL-to-NOISE RATIO vs FREE-AIR TEMPERATURE

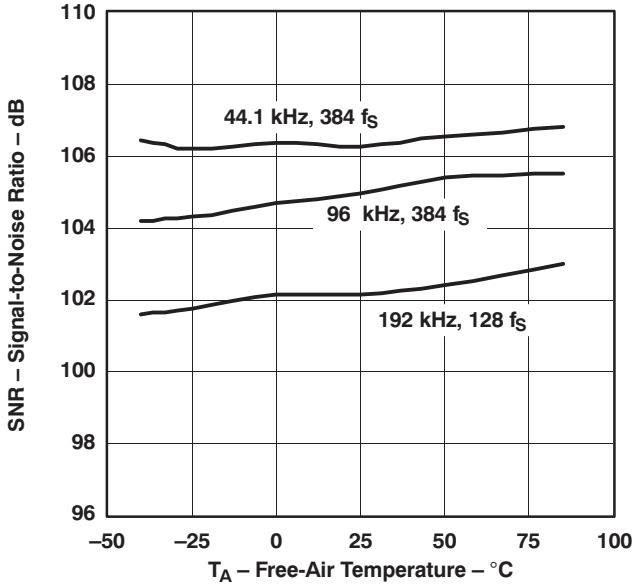


Figure 17.

CHANNEL SEPARATION vs FREE-AIR TEMPERATURE

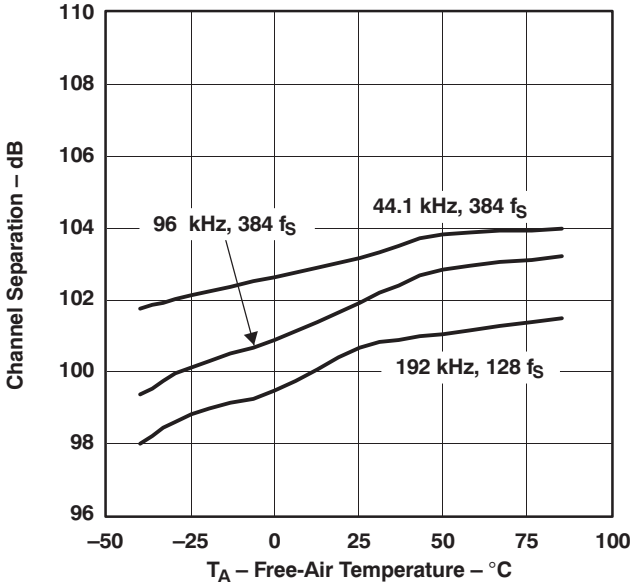


Figure 18.

SYSTEM CLOCK AND RESET FUNCTIONS

System Clock Input

The PCM1754 requires a system clock for operating the digital interpolation filters and multilevel delta-sigma modulators. The system clock is applied at the SCK input (pin 16). Table 1 shows examples of system clock frequencies for common audio sampling rates.

Figure 19 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase-jitter and noise. TI's PLL170x family of multiclock generators is an excellent choice for providing the PCM1754 system clock.

Table 1. System Clock Rates for Common Audio Sampling Frequencies

SAMPLING FREQUENCY	SYSTEM CLOCK FREQUENCY (f_{SCLK}) (MHz)						
	128 f_S	192 f_S	256 f_S	384 f_S	512 f_S	768 f_S	1152 f_S
8 kHz	1.024	1.536	2.048	3.072	4.096	6.144	9.216
16 kHz	2.048	3.072	4.096	6.144	8.192	12.288	18.432
32 kHz	4.096	6.144	8.192	12.288	16.384	24.576	36.864
44.1 kHz	5.6448	8.4672	11.2896	16.9344	22.5792	33.8688	(1)
48 kHz	6.144	9.216	12.288	18.432	24.576	36.864	(1)
88.2 kHz	11.2896	16.9344	22.5792	33.8688	45.1584	(1)	(1)
96 kHz	12.288	18.432	24.576	36.864	49.152	(1)	(1)
192 kHz	24.576	36.864	(1)	(1)	(1)	(1)	(1)

(1) This system clock rate is not supported for the given sampling frequency.

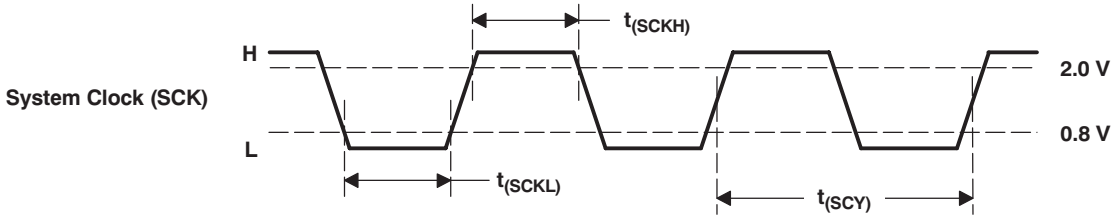


Figure 19. System Clock Input Timing

Table 2. System Clock Input Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
System clock pulse duration, high	$t_{(SCKH)}$	7			ns
System clock pulse duration, low	$t_{(SCKL)}$	7			ns
System clock pulse cycle time	$t_{(SCY)}$		(1)		ns

(1) 1/128 f_S, 1/256 f_S, 1/384 f_S, 1/512 f_S, 1/768 f_S, or 1/1152 f_S

Power-On Reset Functions

The PCM1754 includes a power-on reset function. Figure 20 shows the operation of this function. With the system clock active and V_{CC} > 3 V (typical, 2.2 V to 3.7 V), the power-on reset function is enabled. The initialization sequence requires 1024 system clocks from the time V_{CC} > 3 V (typical, 2.2 V to 3.7 V).

During the reset period (1024 system clocks), the analog output is forced to the bipolar zero level, or $V_{CC}/2$. After the reset period, an internal register is initialized in the next $1/f_S$ period and if SCK, BCK, and LRCK are provided continuously, the PCM1754 provides proper analog output with unit group delay against the input data.

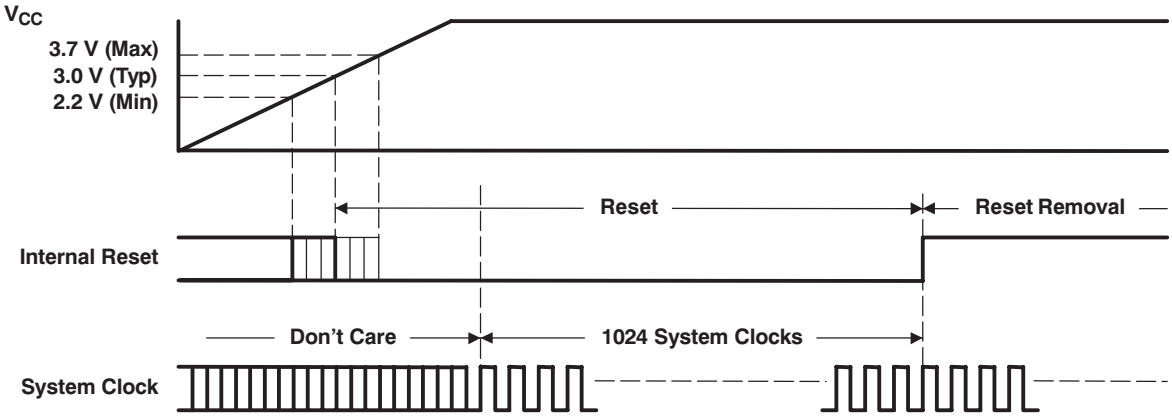


Figure 20. Power-On Reset Timing

AUDIO SERIAL INTERFACE

The audio serial interface for the PCM1754 consists of a 3-wire synchronous serial port. It includes LRCK (pin 3), BCK (pin 1), and DATA (pin 2). BCK is the serial audio bit clock, and it is used to clock the serial data present on DATA into the serial shift register of the audio interface. Serial data is clocked into the PCM1754 on the rising edge of BCK. LRCK is the serial audio left/right word clock. It is used to latch serial data into the internal registers of the serial audio interface.

Both LRCK and BCK should be synchronous to the system clock. Ideally, it is recommended that LRCK and BCK be derived from the system clock input, SCK. LRCK is operated at the sampling frequency, f_S. BCK can be operated at 32, 48, or 64 times the sampling frequency for standard (right-justified) format, and 32 times the sampling frequency of BCK is limited to 16-bit right-justified format only. BCK can be operated at 48 or 64 times the sampling frequency for the I^2S and left-justified formats. 48 times the sampling frequency of BCK is limited to 192/384/768 f_S SCKI.

Internal operation of the PCM1754 is synchronized with LRCK. Accordingly, internal operation is held when the sampling rate clock of LRCK is changed or when SCK and/or BCK is interrupted for a 3-bit clock cycle or longer. If SCK, BCK, and LRCK are provided continuously after this held condition, the internal operation is re-synchronized automatically in a period of less than $3/f_S$. External resetting is not required.

Audio Data Formats and Timing

The PCM1754 supports I²S and 16-bit-word right-justified audio data formats. The data formats are shown in Figure 22. Data formats are selected using the FMT pin on the PCM1754. The default data format is 24-bit left-justified. All formats require binary 2s-complement MSB-first audio data. Figure 21 shows a detailed timing diagram for the serial audio interface.

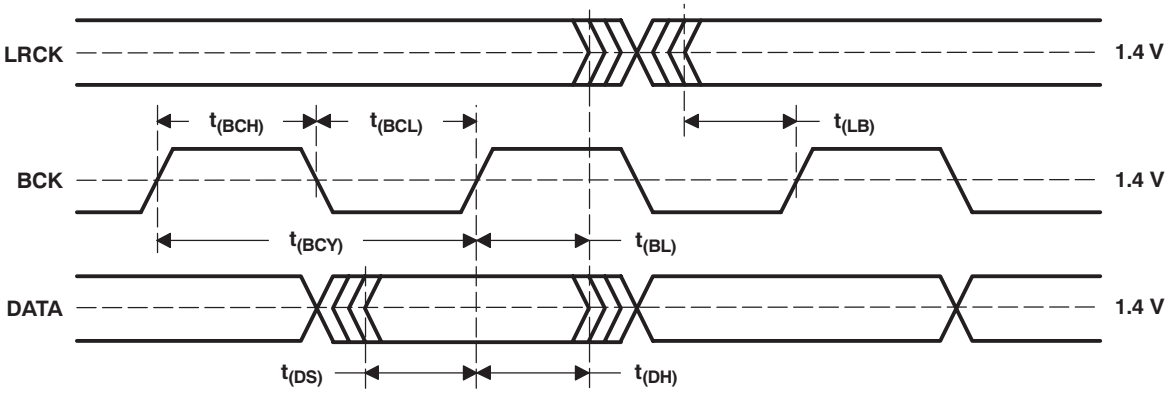


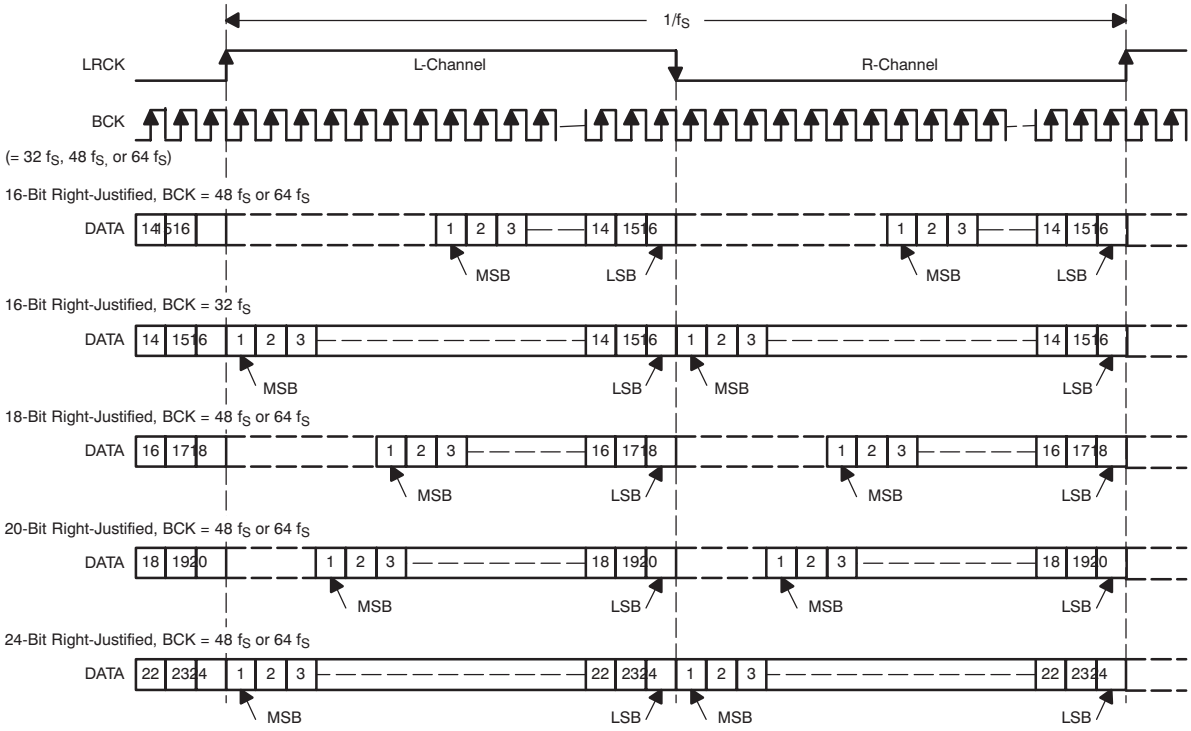
Figure 21. Audio Interface Timing

Table 3. Audio Interface Timing

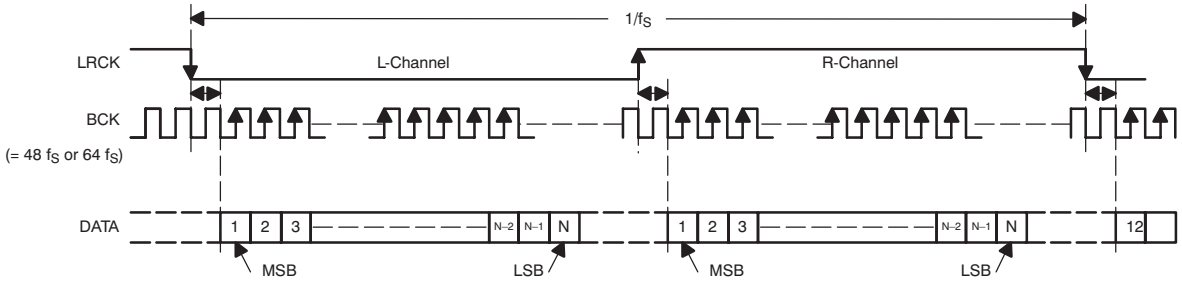
PARAMETER	SYMBOL	MIN	MAX	UNIT
BCK pulse cycle time	$t_{(BCY)}$	1/(32 f_S), 1/(48 f_S), 1/(64 f_S)(1)		
BCK high–level time	$t_{(BCH)}$	35		ns
BCK low–level time	$t_{(BCL)}$	35		ns
BCK rising edge to LRCK edge	$t_{(BL)}$	10		ns
LRCK falling edge to BCK rising edge	$t_{(LB)}$	10		ns
DATA setup time	$t_{(DS)}$	10		ns
DATA hold time	$t_{(DH)}$	10		ns

(1) f_S is the sampling frequency (e.g., 44.1 kHz, 48 kHz, 96 kHz, etc.).

(1) Standard Data Format; L-Channel = HIGH, R-Channel = LOW



(2) I²S Data Format; L-Channel = LOW, R-Channel = HIGH



(3) Left-Justified Data Format; L-Channel = HIGH, R-Channel = LOW

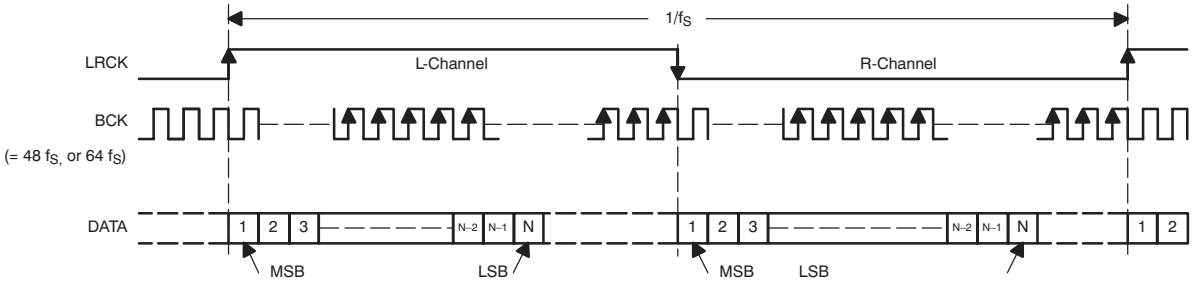


Figure 22. Audio Data Input Formats

ZERO FLAG

The PCM1754 has a ZERO flag pin, ZEROA (pin 11). ZEROA is the L-channel and R-channel common zero flag pin. If the data for L-channel and R-channel remains at a 0 level for 1024 sampling periods (or LRCK clock periods), ZEROA is set to a logic 1 state.

HARDWARE CONTROL

The digital functions of the PCM1754 are capable of hardware control. Table 4 shows selectable formats, Table 5 shows de-emphasis control, and Table 6 shows mute control.

Table 4. Data Format Select

FMT (PIN 15)	DATA FORMAT
LOW	16– to 24–bit, I^2S format
HIGH	16–bit right–justified

Table 5. De-Emphasis Control

DEMP (PIN 13)	DE–EMPHASIS FUNCTION
LOW	44.1 kHz de–emphasis OFF
HIGH	44.1 kHz de–emphasis ON

Table 6. Mute Control

MUTE (PIN 14)	MUTE
LOW	Mute OFF
HIGH	Mute ON

OVERSAMPLING RATE CONTROL

The PCM1754 automatically controls the oversampling rate of the delta-sigma D/A converters with the system clock rate. The oversampling rate is set to 64× oversampling with every system clock and sampling frequency.

ANALOG OUTPUTS

The PCM1754 includes two independent output channels, $V_{OUT}L$ and $V_{OUT}R$. These are unbalanced outputs, each capable of driving 4 V_{PP} typical into a 5-kΩ ac-coupled load. The internal output amplifiers for $V_{OUT}L$ and $V_{OUT}R$ are biased to the dc common-mode (or bipolar zero) voltage, equal to 0.5 V_{CC}.

The output amplifiers include an RC continuous-time filter, which helps to reduce the out-of-band noise energy present at the DAC outputs due to the noise shaping characteristics of the PCM1754 delta-sigma D/A converters. The frequency response of this filter is shown in Figure 23. By itself, this filter is not enough to attenuate the out-of-band noise to an acceptable level for many applications. An external low-pass filter is required to provide sufficient out-of-band noise rejection. Further discussion of DAC post-filter circuits is provided in the Applications Information section of this data sheet.

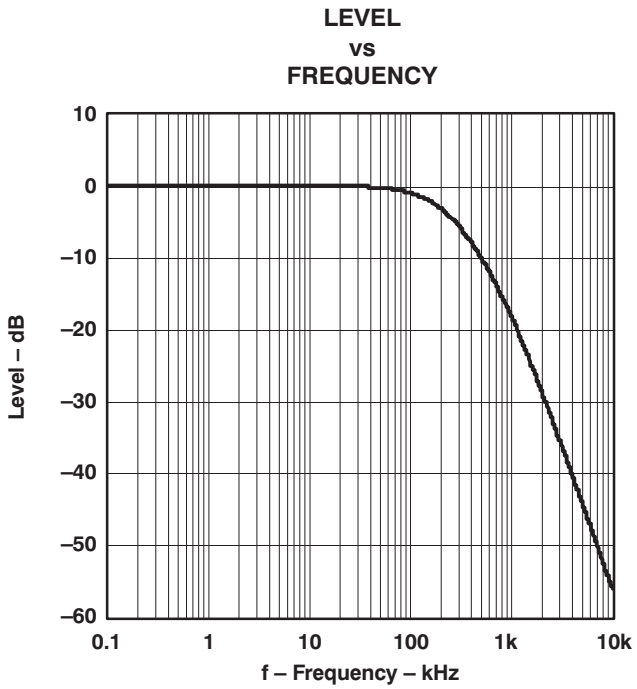
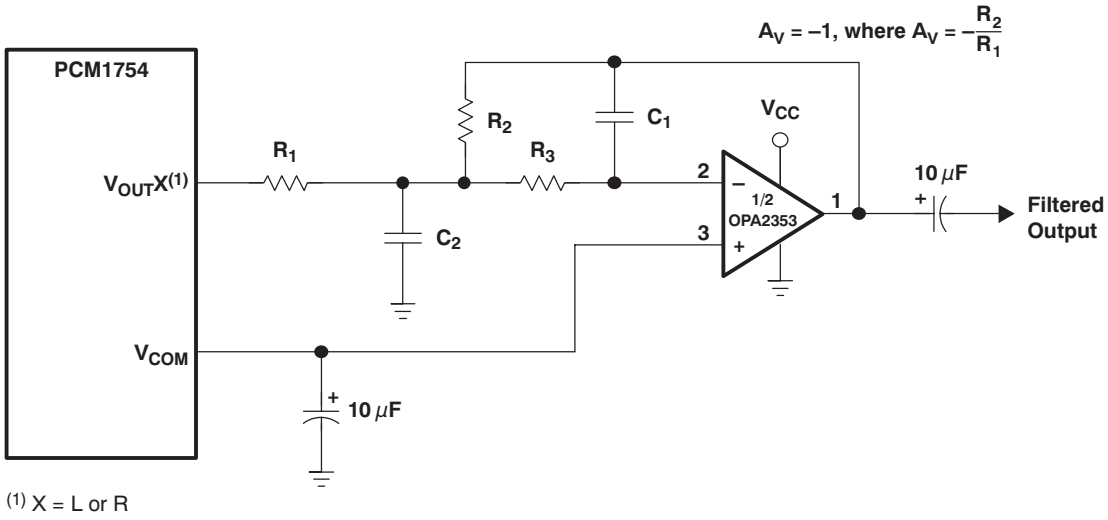


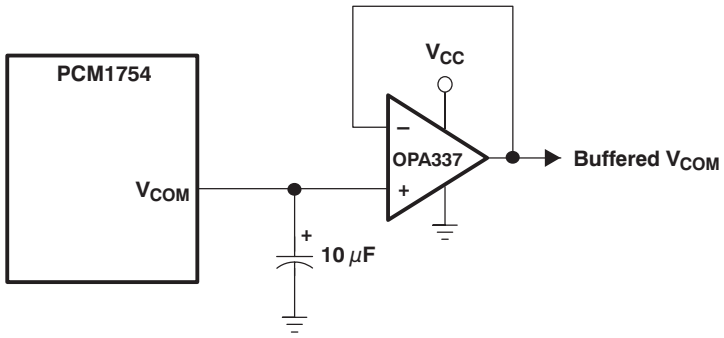
Figure 23. Output Filter Frequency Response

V_{COM} Output

One unbuffered common-mode voltage output pin, V_{COM} (pin 10) is brought out for decoupling purposes. This pin is nominally biased to a dc voltage level equal to 0.5 V_{CC}. This pin can be used to bias external circuits. Figure 24 shows an example of using the V_{COM} pin for external biasing applications.



(a) Using V_{COM} to Bias a Single-Supply Filter Stage



(b) Using a Voltage Follower to Buffer V_{COM} When Biasing Multiple Nodes

Figure 24. Biasing External Circuits Using the V_{COM} Pin

APPLICATION INFORMATION

CONNECTION DIAGRAMS

A basic connection diagram is shown in Figure 25, with the necessary power supply bypassing and decoupling components. TI recommends using the component values shown in Figure 25 for all designs.

The use of series resistors (22 Ω to 100 Ω) is recommended for the SCK, LRCK, BCK, and DATA inputs. The series resistor combines with the stray PCB and device input capacitance to form a low-pass filter, which reduces high-frequency noise emissions and helps to dampen glitches and ringing present on clock and data lines.

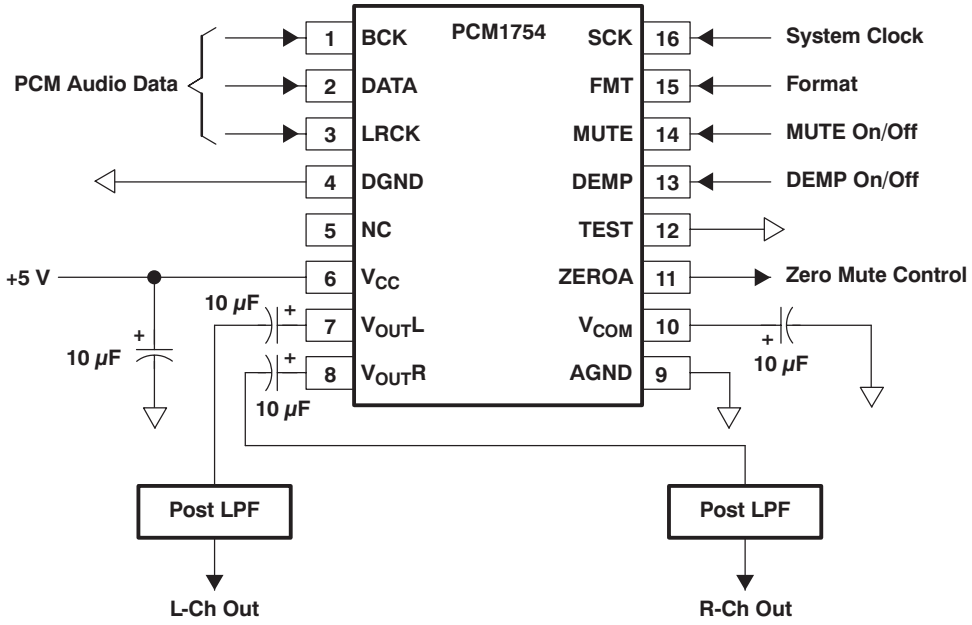


Figure 25. Basic Connection Diagram

POWER SUPPLIES AND GROUNDING

The PCM1754 requires 5 V for V_{CC}.

Proper power supply bypassing is shown in Figure 25. The 10-µF capacitors should be tantalum or aluminum electrolytic.

D/A OUTPUT FILTER CIRCUITS

Delta-sigma D/A converters use noise-shaping techniques to improve in-band signal-to-noise ratio (SNR) performance at the expense of generating increased out-of-band noise above the Nyquist frequency, or $f_S/2$. The out-of-band noise must be low-pass filtered in order to provide the optimal converter performance. This is accomplished by a combination of on-chip and external low-pass filtering.

Figure 24(a) and Figure 26 show the recommended external low-pass active filter circuits for single- and dual-supply applications. These circuits are 2nd-order Butterworth filters using the multiple feedback (MFB) circuit arrangement, which reduces sensitivity to passive component variations over frequency and temperature. For more information regarding MFB active filter design, see Burr-Brown applications bulletin (SBAA055), available from the TI Web site at http://www.ti.com.

Because the overall system performance is defined by the quality of the D/A converters and their associated analog output circuitry, high-quality audio operational amplifiers are recommended for the active filters. TI's OPA2353 and OPA2134 dual operational amplifiers are shown in Figure 24(a) and Figure 26, and are recommended for use with the PCM1754.

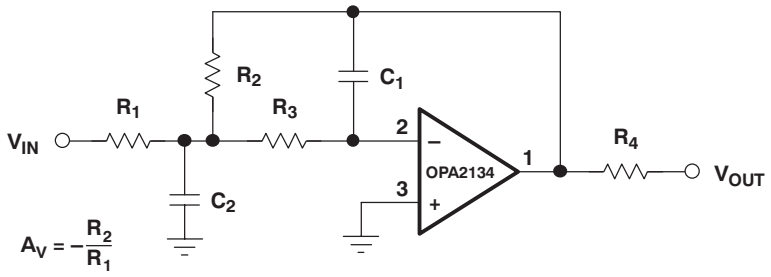


Figure 26. Dual-Supply Filter Circuit

PCB LAYOUT GUIDELINES

A typical PCB floor plan for the PCM1754 is shown in Figure 27. A ground plane is recommended, with the analog and digital sections being isolated from one another using a split or cut in the circuit board. The PCM1754 should be oriented with the digital I/O pins facing the ground plane split/cut to allow for short, direct connections to the digital audio interface and control signals originating from the digital section of the board.

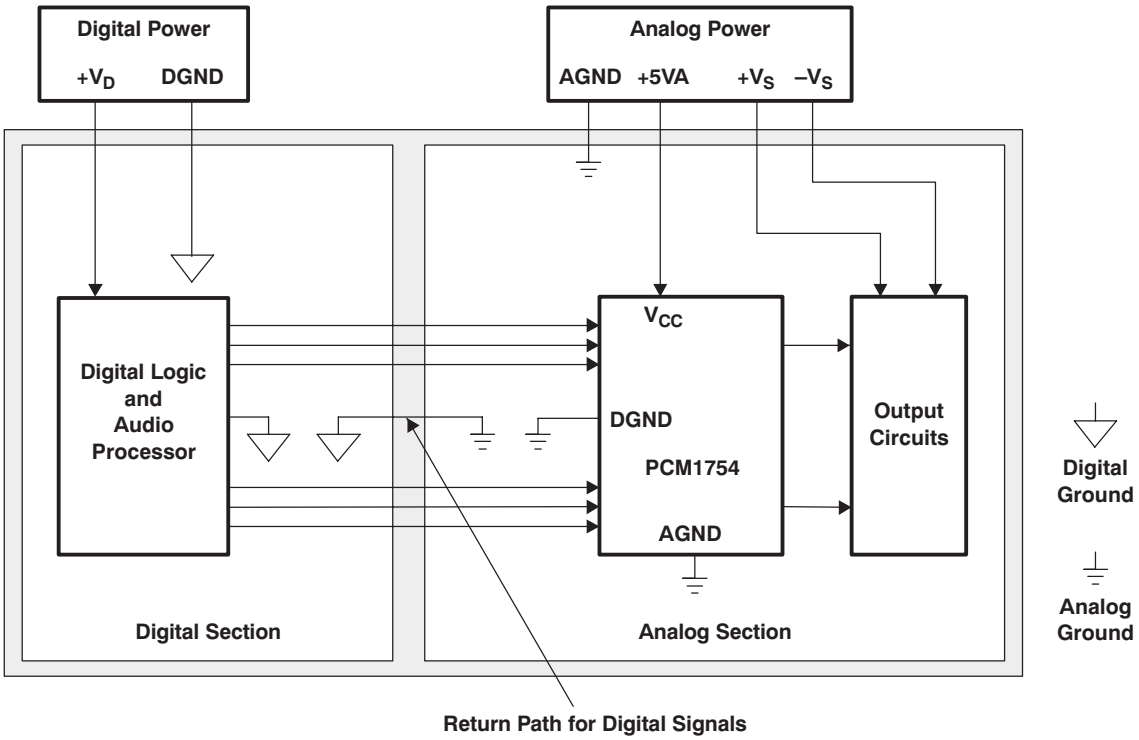


Figure 27. Recommended PCB Layout

Separate power supplies are recommended for the digital and analog sections of the board. This prevents the switching noise present on the digital supply from contaminating the analog power supply and degrading the dynamic performance of the PCM1754. In cases where a common 5-V supply must be used for the analog and digital sections, an inductance (RF choke, ferrite bead) should be placed between the analog and digital 5-V supply connections to avoid coupling of the digital switching noise into the analog circuitry. Figure 28 shows the recommended approach for single-supply applications.

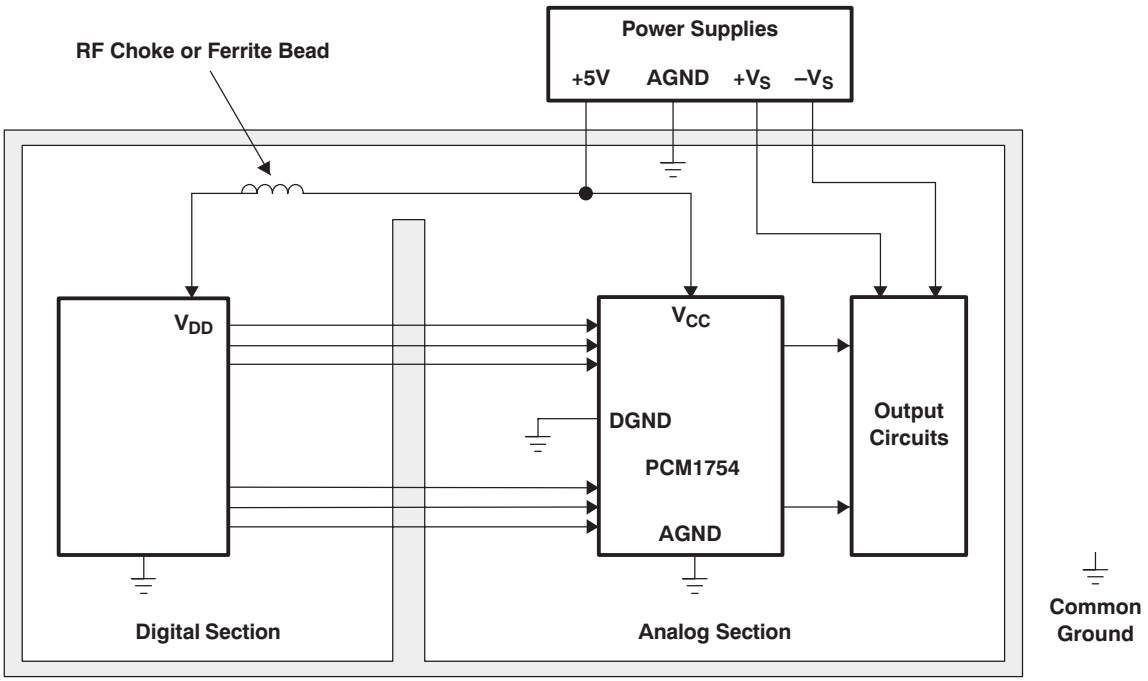


Figure 28. Single-Supply PCB Layout

THEORY OF OPERATION

The delta-sigma section of the PCM1754 is based on an 8-level amplitude quantizer and a 4th-order noise shaper. This section converts the oversampled input data to 8-level delta-sigma format. A block diagram of the 8-level delta-sigma modulator is shown in Figure 29. This 8-level delta-sigma modulator has the advantage of stability and clock jitter sensitivity over the typical one-bit (2-level) delta-sigma modulator.

The combined oversampling rate of the delta-sigma modulator and the interpolation filter is 64 f_S.

The theoretical quantization noise performance of the 8-level delta-sigma modulator is shown in Figure 30 and Figure 31. The enhanced multilevel delta-sigma architecture also has advantages for input clock jitter sensitivity due to the multilevel quantizer, with the simulated jitter sensitivity shown in Figure 32.

KEY PERFORMANCE PARAMETERS AND MEASUREMENT

This section provides information on how to measure key dynamic performance parameters for the PCM1754. In all cases, an Audio Precision System Two Cascade audio measurement system or equivalent is used to perform the testing.

Total Harmonic Distortion + Noise

Total harmonic distortion + noise (THD+N) is a significant figure of merit for audio D/A converters because it takes into account both harmonic distortion and all noise sources within a specified measurement bandwidth. The average value of the distortion and noise is referred to as THD+N.

For the PCM1754, THD+N is measured with a full-scale, 1-kHz digital sine wave as the test stimulus at the input of the DAC (see Figure 33). The digital generator is set to 24-bit audio word length and a sampling frequency of 44.1 kHz or 96 kHz. The digital generator output is taken from the unbalanced S/PDIF connector of the measurement system. The S/PDIF data is transmitted via a coaxial cable to the digital audio receiver on the DEM-DAI1753 demonstration board. The receiver is then configured to output 24-bit data in either I^2S or left-justified data format. The DAC audio interface format is programmed to match the receiver output format. The analog output is then taken from the DAC post filter and connected to the analog analyzer input of the measurement system. The analog input is band limited using filters resident in the analyzer. The resulting THD+N is measured by the analyzer and displayed by the measurement system.

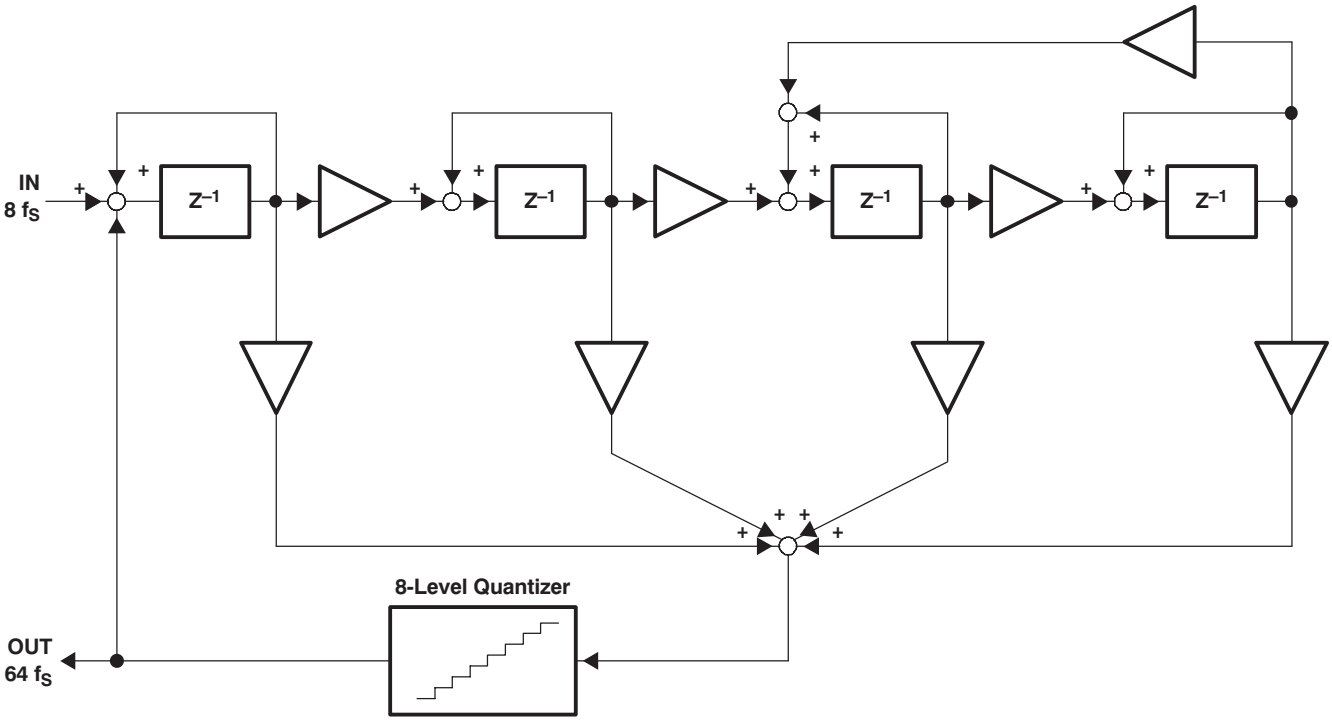


Figure 29. Eight-Level Delta-Sigma Modulator

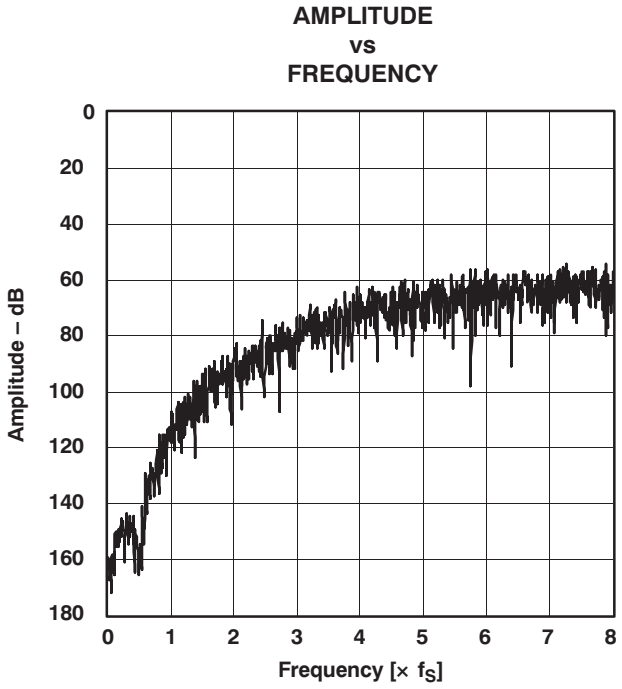


Figure 30. Quantization Noise Spectrum (×64 Oversampling)

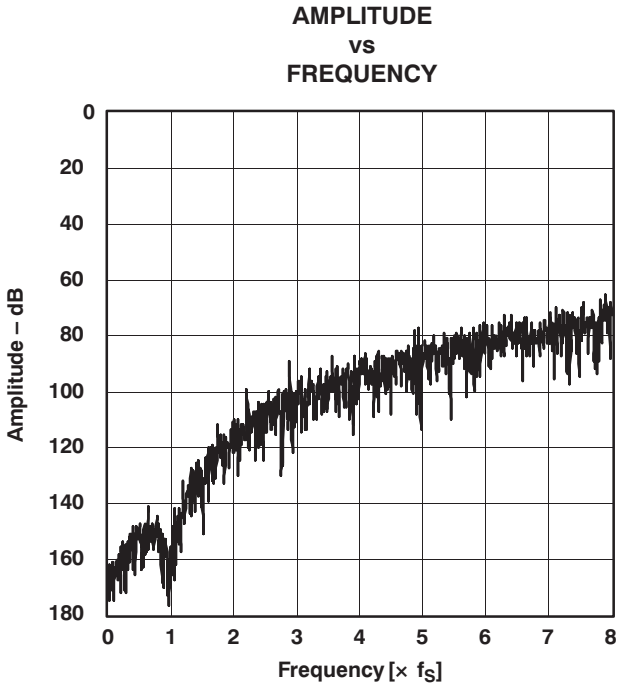


Figure 31. Quantization Noise Spectrum (×128 Oversampling)

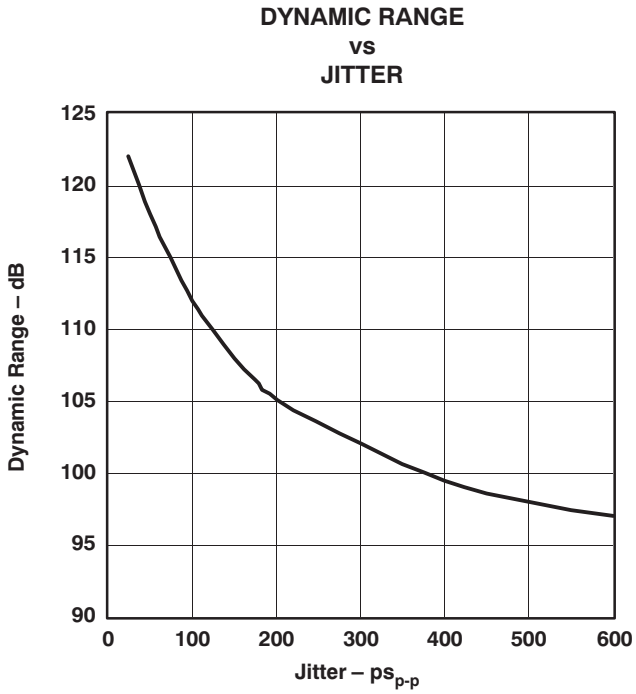


Figure 32. Jitter Dependence (×64 Oversampling)

Dynamic Range

Dynamic range is specified as A-weighted THD+N measured with a –60-dB full-scale, 1-kHz digital sine wave stimulus at the input of the D/A converter. This measurement is designed to give a good indicator of how the DAC performs given a low-level input signal.

The measurement setup for the dynamic range measurement is shown in Figure 34, and is similar to the THD+N test setup discussed previously. The differences include the band limit filter selection, the additional A-weighting filter, and the –60-dB full-scale input level.

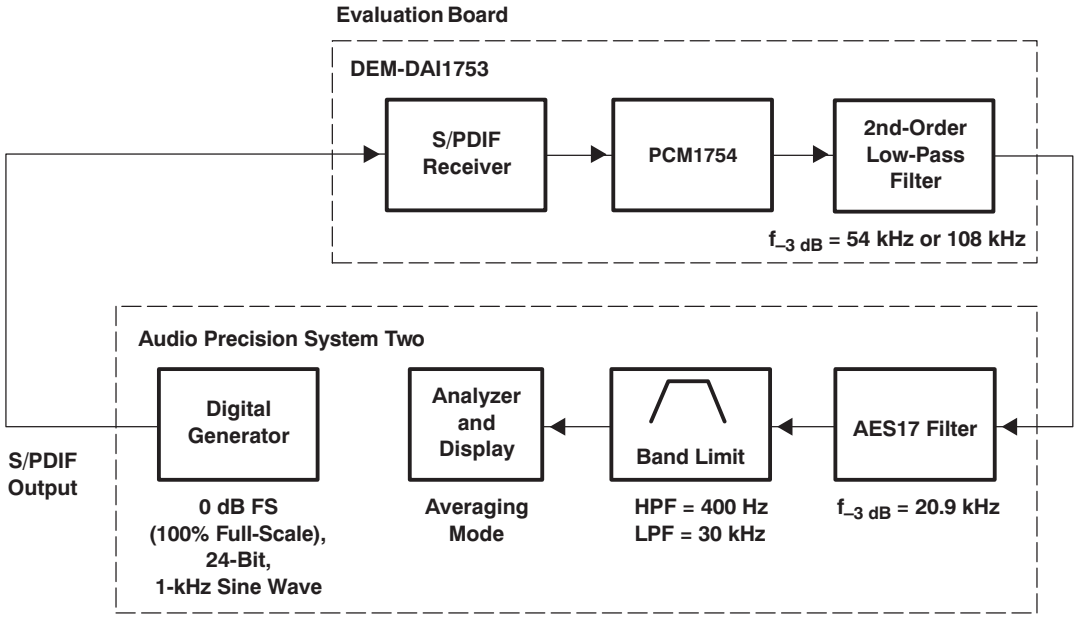


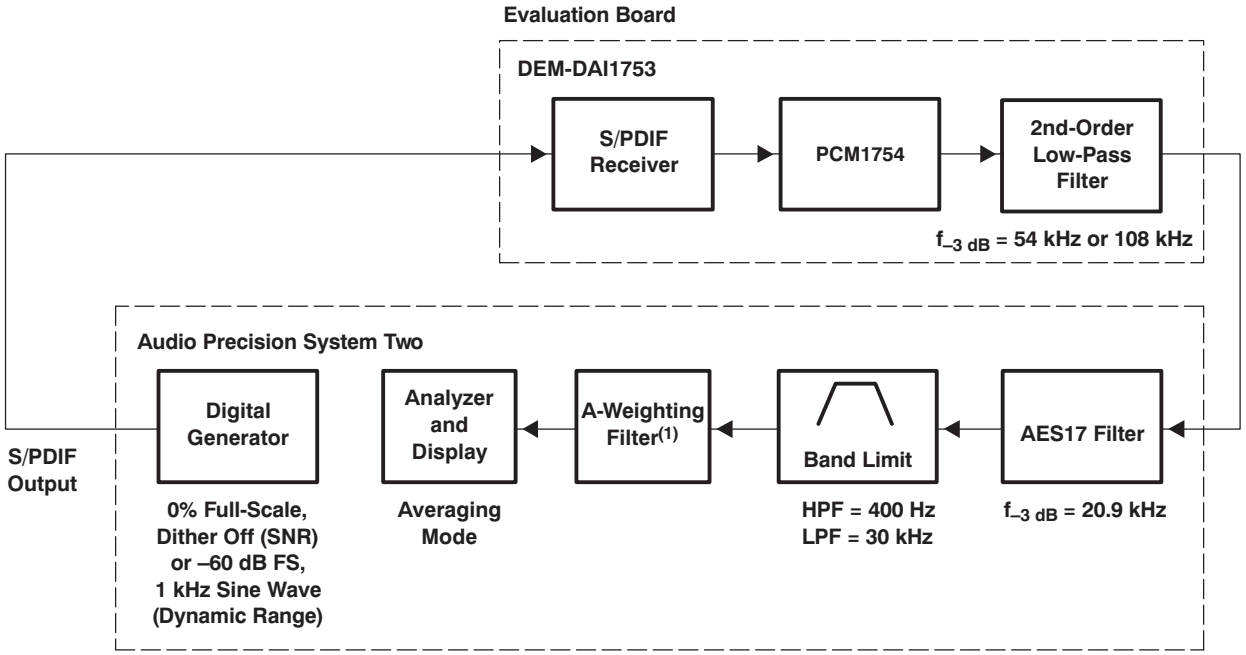
Figure 33. Test Setup for THD+N Measurement

Idle Channel Signal-to-Noise Ratio (SNR)

The SNR test provides a measure of the noise floor of the D/A converter. The input to the D/A is all-0s data, and the dither function of the digital generator must be disabled to ensure an all-0s data stream at the input of the D/A converter.

The measurement setup for SNR is identical to that used for dynamic range, with the exception of the input signal level.

(See the note provided in Figure 34).



(1) Results without A-Weighting are approximately 3 dB worse.

Figure 34. Test Setup for Dynamic Range and SNR Measurement

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
PCM1754TDBQRQ1	ACTIVE	SSOP/ QSOP	DBQ	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

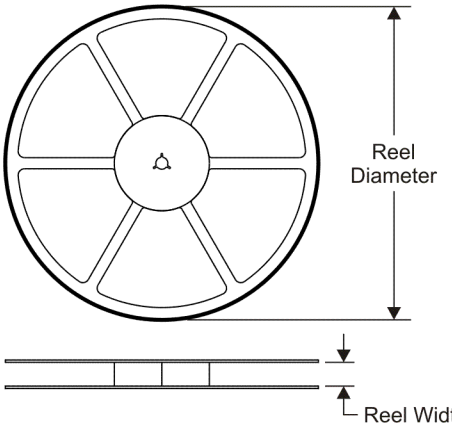
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

OTHER QUALIFIED VERSIONS OF PCM1754-Q1 :
- Catalog: PCM1754

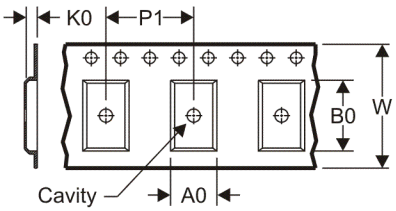
NOTE: Qualified Version Definitions:
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

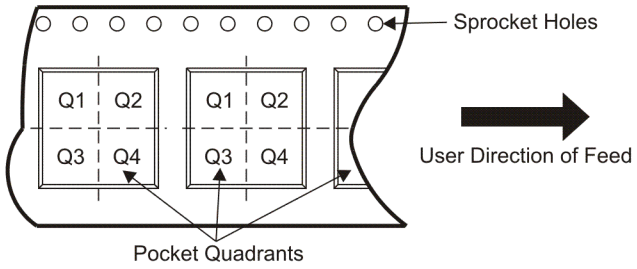


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

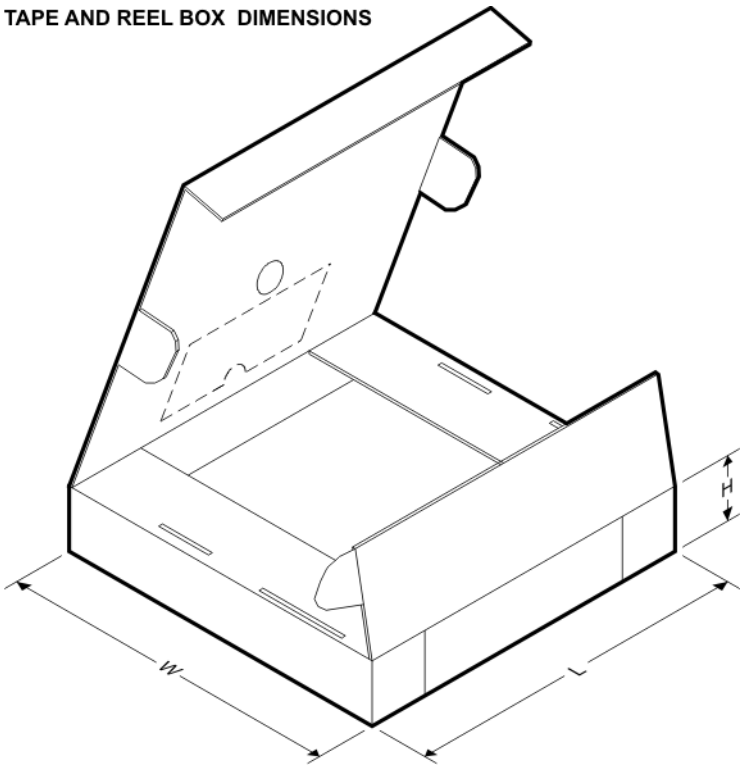
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM1754TDBQRQ1	SSOP/ QSOP	DBQ	16	2000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

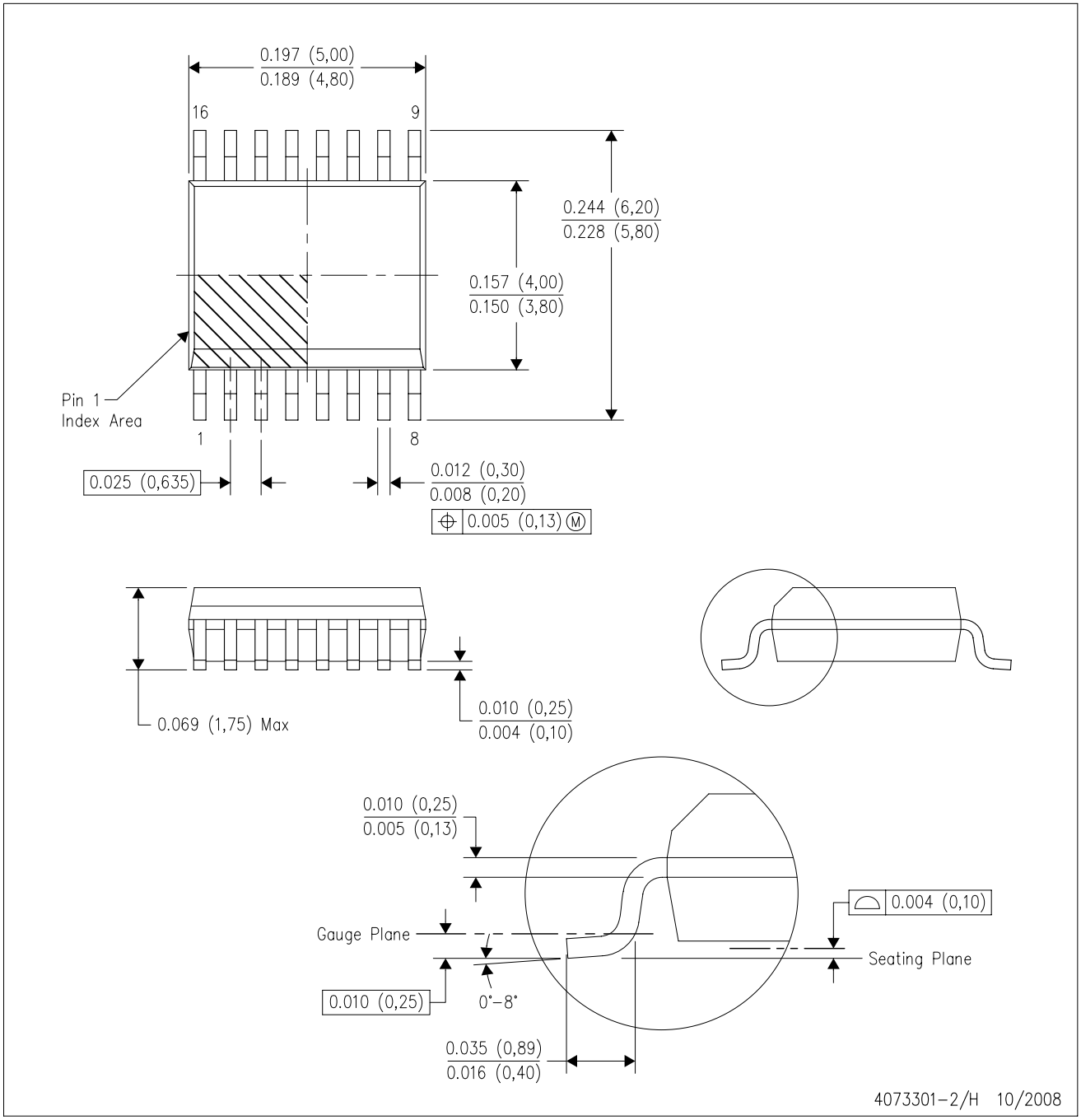
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

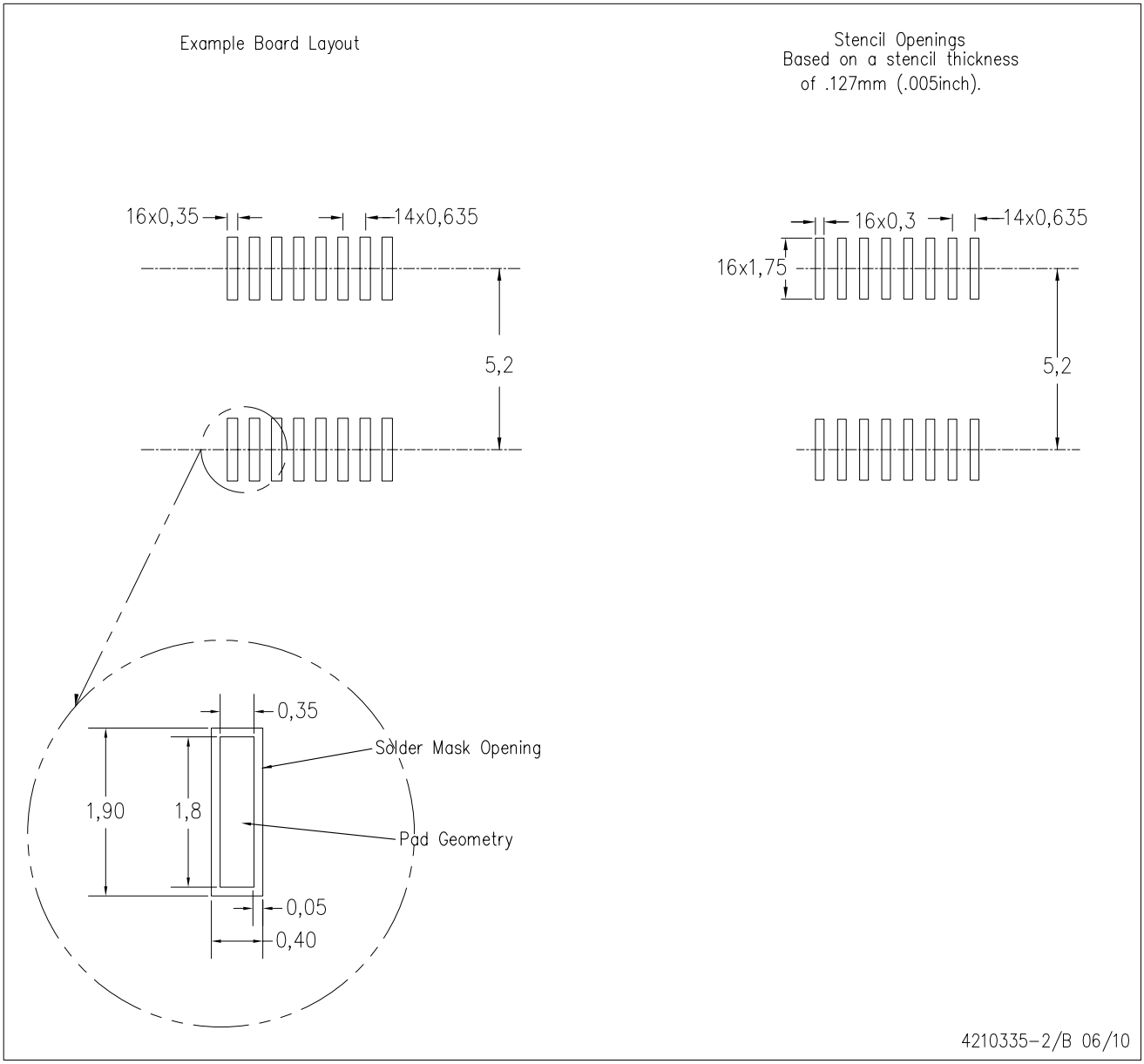
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM1754TDBQRQ1	SSOP/QSOP	DBQ	16	2000	346.0	346.0	29.0

DBQ (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AB.

DBQ (R-PDSO-G16) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Space, Avionics & Defense	www.ti.com/space-avionics-defense
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video and Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless-apps

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