EM78F651N

8-Bit Microcontroller

Product Specification

DOC. VERSION 1.1

ELAN MICROELECTRONICS CORP.

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APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial version	2006/09/20
1.1	1. Modified the General Description, Pin Assignment and Features sections. 2. Added Green Product Information. 3. Modified the Functional Block Diagram.	2006/10/20

1 General Description

The EM78F651N is an 8-bit microprocessor designed and developed with low-power, high-speed CMOS technology and high noise immunity. It has an on-chip 1K×13-bit Electrical Flash Memory and 128×8-bit in system programmable EEPROM. It provides three protection bits to prevent intrusion of user's Flash memory code. Twelve Code option bits are also available to meet user's requirements.

With its enhanced Flash-ROM feature, the EM78F651N provides a convenient way of developing and verifying user's programs. Moreover, this Flash-ROM device offers the advantages of easy and effective program updates, using development and programming tools. User can avail of the ELAN Writer to easily program his development code.

2 Features

- CPU configuration
  - 1K×13 bits on chip ROM
  - 80×8 bits on chip registers (SRAM)
  - 128 bytes in-system programmable EEPROM
    *Endurance: 100,000 write/erase cycles
  - More than 10 years data retention
  - 5-level stacks for subroutine nesting
  - Less than 2 mA at 5V/4MHz
  - Typically 20 μA, at 3V/32kHz
  - Typically 2 μA, during sleep mode
- I/O port configuration
  - 2 bidirectional I/O ports
  - Wake-up port : P6
  - 8 Programmable pull-down I/O pins
  - 8 programmable pull-high I/O pins
  - 8 programmable open-drain I/O pins
  - External interrupt : P60
- Operating voltage range:
  - Operating voltage: 2.2V~5.5V at -40°C ~85°C (Industrial)
- Operating frequency range (base on two clocks):
  - Crystal mode:
    DC ~ 20MHz @ 5V
    DC ~ 8MHz @ 3V
    DC ~ 4MHz @ 2.2V
  - ERC mode:
    DC ~ 16MHz @ 5V
    DC ~ 8MHz @ 3V
    DC ~ 4MHz @ 2.2V
  - IRC mode:
    DC ~ 16MHz @ 4.5V~5.5V
    DC ~ 4MHz @ 2.2V~5.5V
- Three available interrupts:
  - TCC overflow interrupt
  - Input-port status changed interrupt (wake-up from sleep mode)
  - External interrupt
- Peripheral configuration
  - 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
  - Power down (Sleep) mode
    *Vdd power monitor and supports low voltage detector interrupt flag
  - 4 programmable Level Voltage Detector (LVD)
  - Three security registers to prevent intrusion of Flash memory codes
  - One configuration register to accommodate user's requirements
  - 2/4/8/16 clocks per instruction cycle selected by code option
- Single instruction cycle commands
- Four Crystal range in Oscillator Mode

Crystal Range	Oscillator Mode
20MHz ~ 6MHz	HXT
6MHz ~ 1MHz	XT
1MHz ~ 100kHz	LXT1
32.768kHz	LXT2

- Programmable free running watchdog timer
- Package type:
  - 14-pin DIP 300mil : EM78F651NAPxS/xJ
  - 14-pin SOP 150mil : EM78F651NAMxS/xJ
  - 16-pin DIP 300mil : EM78F651NABPxS/xJ
  - 16-pin SOP 300mil : EM78F651NABMxS/xJ
  - 18-pin DIP 300 mil : EM78F651NCPxS/xJ
  - 18-pin SOP 300mil : EM78F651NCMxS/xJ
  - 20-pin DIP 300mil : EM78F651NDPxS/xJ
  - 20-pin SSOP 209mil : EM78F651NDKMxS/XJ

  Green products do not contain hazardous substances.

3 Pin Assignment

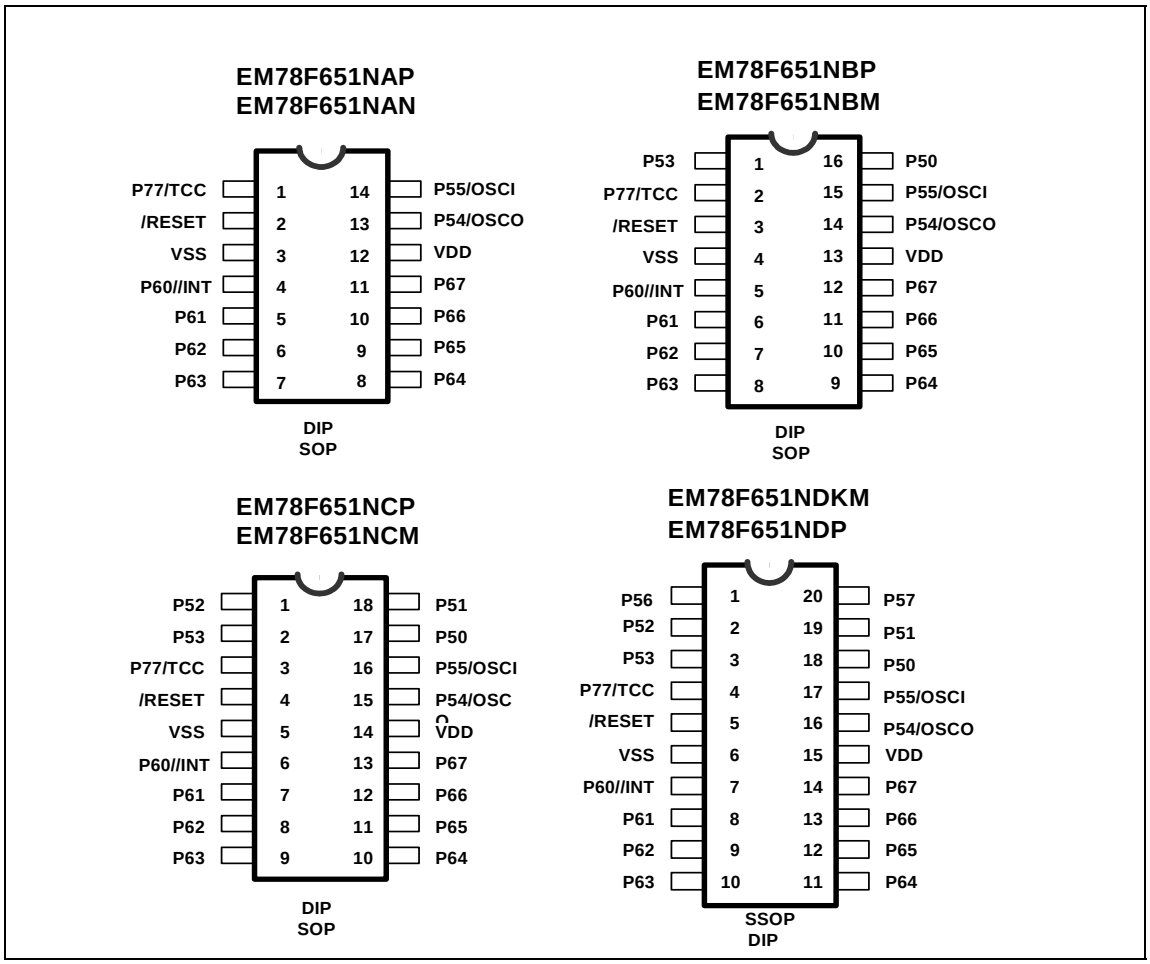


Fig. 3-1 Pin Assignment

4 Pin Description

Table 1 EM78F651NAP, EM78F651NAM

Symbol	Pin No.	Type	Function
P54~P55	13, 14	I/O	Bidirectional 2-bit input/output pins
P60~P67	4~11	I/O	Bidirectional 8-bit input/output pins. These can be pulled-high or can be open drain by software programming. P60~63 can also be pulled down by software.
P77	1	I/O	P77 is an open drain I/O pin.
OSCI	14	I	Crystal type: Crystal input terminal or external clock input pin ERC type: RC oscillator input pin
OSCO	13	I/O	Crystal type: Output terminal for crystal oscillator or external clock input pin. RC type: Instruction clock output. External clock signal input.
TCC	1	I	Real time clock/counter (with Schmitt Trigger input pin) must be tied to VDD or VSS if not in use.
/INT	4	I	External interrupt pin triggered by a falling edge.
/RESET	2	I	Input pin with Schmitt Trigger. If this pin remains at logic low, the controller will also remain in reset condition.
VDD	12	–	Power supply
VSS	3	–	Ground

Table 2 EM78F651NBP, EM78F651NBM

Symbol	Pin No.	Type	Function
P50, P53 P54~P55	16, 1, 14, 15	I/O	Bidirectional 4-bit input/output pins 50, P53 can be pulled-down by software.
P60~P67	5~12	I/O	Bidirectional 8-bit input/output pins. These can be pulled-high or can be open drain by software programming. P60~63 can also be pulled down by software.
P77	2	I/O	P77 is an open drain I/O pin.
OSCI	15	I	Crystal type: Crystal input terminal or external clock input pin ERC type: RC oscillator input pin
OSCO	14	I/O	Crystal type: Output terminal for crystal oscillator or external clock input pin. RC type: Instruction clock output. External clock signal input.
TCC	2	I	The real time clock/counter (with Schmitt Trigger input pin) must be tied to VDD or VSS if not in use.
/INT	5	I	External interrupt pin triggered by a falling edge.
/RESET	3	I	Input pin with Schmitt Trigger. If this pin remains at logic low, the controller will also remain in reset condition.
VDD	13	-	Power supply
VSS	4	-	Ground

Table 3 EM78F651NCP, EM78F651NCM

Symbol	Pin No.	Type	Function
P50~P53 P54~P55	17, 18, 12, 15, 16	I/O	P50~P53 are bidirectional 4-bit input/output pins and can be pulled-down by software.
P60~P67	6~13	I/O	Bidirectional 8-bit input/output pins. These can be pulled-high or can be open drain by software programming. P60~63 can also be pulled down by software.
P77	3	I/O	P77 is an open drain I/O pin.
OSCI	16	I	Crystal type: Crystal input terminal or external clock input pin ERC type: RC oscillator input pin
OSCO	15	I/O	Crystal type: Output terminal for crystal oscillator or external clock input pin. RC type: Instruction clock output. External clock signal input.
TCC	3	I	Real time clock/counter (with Schmitt Trigger input pin) must be tied to VDD or VSS if not in use.
/INT	6	I	External interrupt pin triggered by a falling edge.
/RESET	4	I	Input pin with Schmitt Trigger. If this pin remains at logic low, the controller will also remain in reset condition.
VDD	14	-	Power supply
VSS	5	-	Ground

Table 4 EM78F651NDKM, EM78F651NDP

Symbol	Pin No.	Type	Function
P50~P57	18, 19, 2, 3, 16, 17, 1, 20	I/O	P50~P57 are bidirectional 8-it input/output pins. P50 and P51 can also be defined as the R-option pins. P50~P53 can be pulled-down by software.
P60~P67	7~14	I/O	Bidirectional 8-bit input/output pins. These can be pulled-high or can be open drain by software programming. P60~63 can also be pulled down by software.
P77	4	I/O	P77 is an open drain I/O pin.
OSCI	17	I	Crystal type: Crystal input terminal or external clock input pin ERC type: RC oscillator input pin
OSCO	16	I/O	Crystal type: Output terminal for crystal oscillator or external clock input pin. RC type: Instruction clock output. External clock signal input.
TCC	4	I	The real time clock/counter (with Schmitt Trigger input pin) must be tied to VDD or VSS if not in use.
/INT	7	I	External interrupt pin triggered by a falling edge.
/RESET	5	I	Input pin with Schmitt Trigger. If this pin remains at logic low, the controller will also remain in reset condition.
VDD	15	-	Power supply
VSS	5	-	Ground

5 Block Diagram

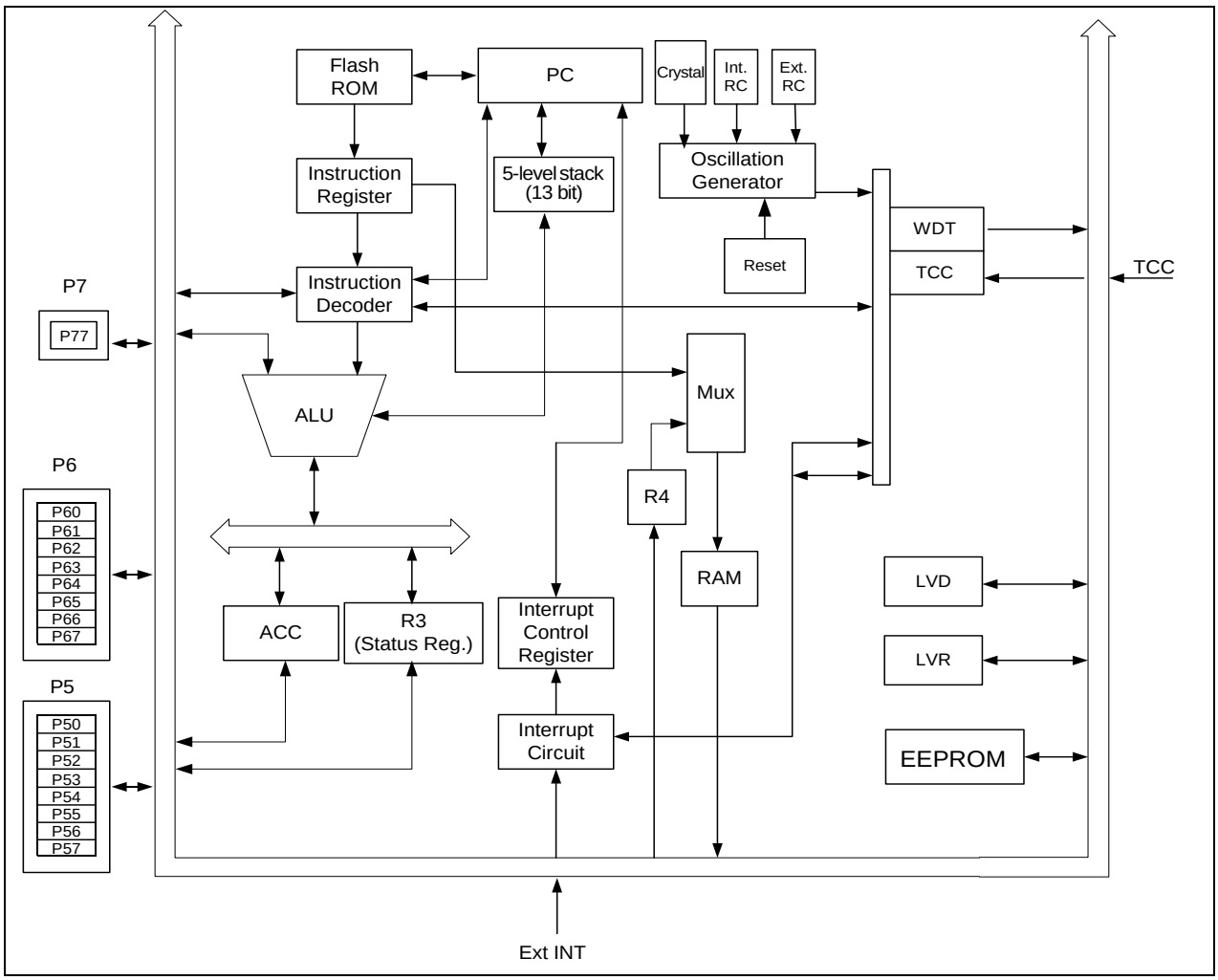


Fig. 5-1 Functional Block Diagram

6 Function Description

6.1 Operational Registers

6.1.1 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is used as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

6.1.2 R1 (Timer Clock/Counter)

R1 is incremented by an external signal edge, which is defined by TE bit (CONT-4) through the TCC pin, or by the instruction cycle clock. It is writable and readable as any other registers. It is defined by resetting PSTE (CONT-3).

The prescaler is assigned to TCC, if the PSTE bit (CONT-3) is reset. The contents of the prescaler counter are cleared only when the TCC register is written with a value.

6.1.3 R2 (Program Counter) & Stack

Depending on the device type, R2 and hardware stack are 10-bit wide. The structure is depicted in Fig 6-1.

The configuration structure generates 1024×13 bits on-chip Flash ROM addresses to the relative programming instruction codes. One program page is 1024 words long.

R2 is set as all "0"s when under a reset condition.

"JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows PC to go to any location within a page.

"CALL" instruction loads the lower 10 bits of the PC, and then PC+1 is pushed into the stack. Thus, the subroutine entry address can be located anywhere within a page.

"RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.

"ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.

"MOV R2, A" allows to load an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits of the PC won't be changed.

Any instruction except "ADD R2,A" that is written to R2 (e.g. "MOV R2, A", "BC R2, 6", etc.) will cause the ninth bit and the tenth bit (A8~A9) of the PC to remain unchanged.

All instructions are single instruction cycle (fclk/2 or fclk/4) except for the instruction that would change the contents of R2. Such instruction will need one more instruction cycle.

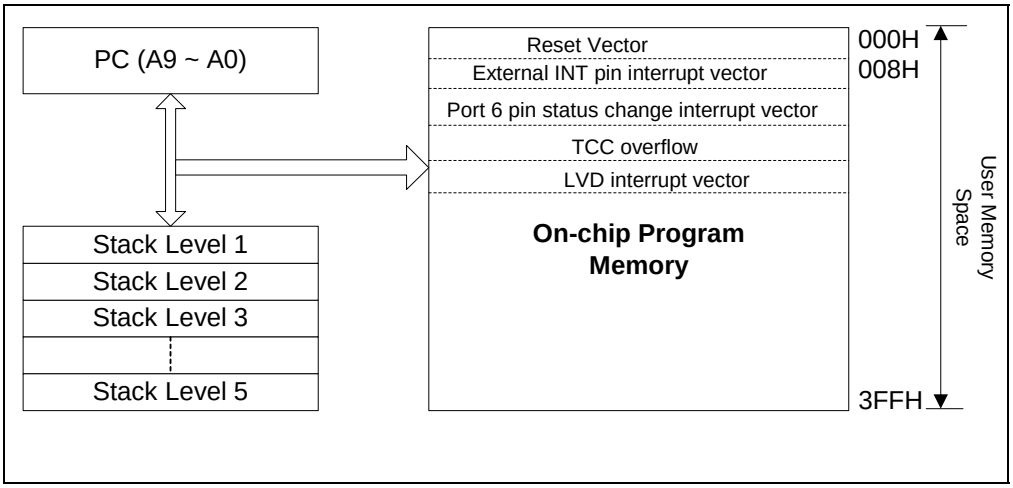


Fig. 6-1 Program Counter Organization

Address	R PAGE Registers		IOC PAGE Registers	
00	R0	(IAR)	Reserve	
01	R1	(TCC)	CONT	(Control Register)
02	R2	(PC)	Reserve	
03	R3	(Status)	Reserve	
04	R4	(RSR)	Reserve	
05	R5	(Port 5)	IOC5	(I/O Port Control Register)
06	R6	(Port 6)	IOC6	(I/O Port Control Register)
07	R7	(Port 7)	IOC7	(I/O Port Control Register)
08	Reserve		Reserve	
09	Reserve		Reserve	
0A	RA	(WUCR)	IOCA	(WDT Control Register)
0B	RB	(EECON)	IOCB	(Pull-down Register)
0C	RC	(EEADR)	IOCC	(Open-drain Control)
0D	RD	(EEDATA)	IOCD	(Pull-high Control Register)
0E	RE	(LVD Control)	Reserve	
0F	RF	(Interrupt Status)	IOCF	(Interrupt Mask Register)
10 : 1F	General Registers			
20 : 3F	Bank 0	Bank 1		

Fig. 6-2 Data Memory Configuration

6.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GP2	GP1	GP0	T	P	Z	DC	C

Bits 7 ~ 5 (GP2 ~ 0): General-purpose read/write bits

Bit 4 (T): Time-out bit

Set to 1 with the "SLEP" and "WDTC" commands, or during power up and reset to 0 by WDT time-out.

Bit 3 (P): Power down bit

Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.

Bit 2 (Z): Zero flag

Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.5 R4 (RAM Select Register)

Bit 7: not used (read only). Bit 7 is always set to “0” at all time.

Bit 6 is used to select Bank 0 or Bank 1.

Bits 5~0 are used to select registers (address: 00~3F) in indirect addressing mode.

Z flag of R3 is set to “1” when R4 content is equal to “3F.” When R4=R4+1, R4 content will select as R0.

See the configuration of the data memory in Fig 6-2.

6.1.6 R5 ~ R7 (Port 5 ~ Port 7)

R5 and R6 are I/O registers.

Only Bits 4, 5 of R5 are available (EM78F651NA)

Only Bits 0, 1, 4, 5 of R5 are available (EM78F651NB)

Only the lower 6 bits of R5 are available (EM78F651NC, D)

Only Bit 0 of R7 is available

6.1.7 R8 ~ R9

Reserved registers

6.1.8 RA (Wake- up Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	ICWE	-	-	-	-	-	-

Bit 7: Not used. Set all "0"

Bit 6 (ICWE): Port 6 input status change wake-up enable bit

0 = Disable Port 6 input status change wake-up

1 = Enable Port 6 input status change wake-up

Bits 5~0: Not used. Set all to "0".

6.1.9 RB (EEPROM Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RD	WR	EEWE	EEDF	EEPC	-	-	-

Bit 7: Read control register

0 : Does not execute EEPROM read

1 : Read EEPROM content, (RD can be set by software, RD is cleared by hardware after Read instruction is completed)

Bit 6 : Write control register

0 : Write cycle to the EEPROM is complete.

1 : Initiate a write cycle, (WR can be set by software, WR is cleared by hardware after Write cycle is completed)

Bit 5 : EEPROM Write Enable bit.

0 : Prohibit write to the EEPROM

1 : Allows EEPROM write cycles

Bit 4 : EEPROM Detective Flag

0 : Write cycle is completed

1 : Write cycle is unfinished

Bits 3 : EEPROM power-down control bit

0 : Switch off the EEPROM

1 : EEPROM is operating

Bits 2 ~ 0: Not used, set to "0" at all time

6.1.10 RC (128 Bytes EEPROM Address)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	EE_A6	EE_A5	EE_A4	EE_A3	EE_A2	EE_A1	EE_A0

Bit 7 ： Not used, fixed at “0”

Bits 6 ~ 0 ： 128 bytes EEPROM address

6.1.11 RD (128 Bytes EEPROM Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EE_D7	EE_D6	EE_D5	EE_D4	EE_D3	EE_D2	EE_D1	EE_D0

Bits 7 ~ 0 ： 128 bytes EEPROM data

6.1.12 RE (LVD Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	LVDEN	/LVD	LVD1	LVD0

Bits 7 ~ 4: Not used, set to “0” at all time

Bit 3 (LVDEN): Low Voltage Detect Enable Bit

0 : LVD disable

1 : LVD enable

Bit 2 (/LVD): Low Voltage Detector. This is a read only bit. When the VDD pin voltage is lower than LVD voltage interrupt level (selected by LVD1 and LVD0), this bit will be cleared.

0 : low voltage is detected

1 : low voltage is not detected or LVD function is disabled

Bit 1~Bit 0 (LVD1~LVD0): Low Voltage Detect level select bits

LVD1	LVD0	LVD Voltage Interrupt Level
0	0	2.1
0	1	3.1
1	0	3.8
1	1	4.3

6.1.13 RF (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDIF	-	-	-	-	EXIF	ICIF	TCIF

Note: " 1 " means with interrupt request **" 0 "** means no interrupt occurs

Bit 7 (LVDIF): Low voltage Detector interrupt flag

When LVD1, LVD0 = "0, 0", Vdd > 2.3V, LVDIF is "0", Vdd ≤ 2.3V, set LVDIF to "1". LVDIF reset to "0" by software.

When LVD1, LVD0 = "0, 1", Vdd > 3.3V, LVDIF is "0", Vdd ≤ 3.3V, set LVDIF to "1". LVDIF reset to "0" by software.

When LVD1, LVD0 = "1, 0", Vdd > 4.0V, LVDIF is "0", Vdd ≤ 4.0V, set LVDIF to "1". LVDIF reset to "0" by software.

When LVD1, LVD0 = "1, 1", Vdd > 4.5V, LVDIF is "0", Vdd ≤ 4.5V, set LVDIF to "1". LVDIF reset to "0" by software.

Bits 6 ~ 3 Not used. Set all to"0".

Bit 2 (EXIF) External interrupt flag. Set by a falling edge on /INT pin, reset by software.

Bit 1 (ICIF) Port 6 input status change interrupt flag. Set when Port 6 input changes, reset by software.

Bit 0 (TCIF) TCC overflow interrupt flag. Set when TCC overflows, reset by software.

RF can be cleared by instruction but cannot be set.

IOCF is the interrupt mask register.

Note that the result of reading RF is the "logic AND" of RF and IOCF.

6.1.14 R10 ~ R3F

All of these are 8-bit general-purpose registers.

6.2 Special Function Registers

6.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator, which is not an addressable register.

6.2.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	/INT	TS	TE	PSTE	PST2	PST1	PST0

Bit 7 Not used, set to "0" at all time.

Bit 6 (/INT): Interrupt enable flag

0 : masked by DISI or hardware interrupt

1 : enabled by ENI/RETI instructions

Bit 5 (TS): TCC signal source

0 : internal instruction cycle clock

1 : transition on TCC pin

Bit 4 (TE): TCC signal edge

0 : increment if a transition from low to high takes place on TCC pin

1 : increment if a transition from high to low takes place on TCC pin

Bit 3 (PSTE): Prescaler enable bit for TCC

0 : prescaler disable bit, TCC rate is 1:1

1 : prescaler enable bit, TCC rate is set as Bit 2~Bit 0

Bit 0 (PST0) ~ Bit 2 (PST2): TCC prescaler bits

PST2	PST1	PST0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

CONT register is both readable and writable.

6.2.3 IOC5 ~ IOC7 (I/O Port Control Register)

A value of "1" sets the relative I/O pin into high impedance, while "0" defines the relative I/O pin as output.

Only Bits 4, 5 of R5 are available (EM78F651NA)

Only Bits 0, 3, 4, 5 of IOC5 can be defined (EM78F651NB)

Only the lower 6 bits of IOC5 can be defined (EM78F651NC)

Only Bit 0 of IOC7 is available, when P7.0 is set as output, a pull-high resistor must be tied to Vdd, since this is an internal open-drain circuit.

IOC5 and IOC7 registers are both readable and writable.

6.2.4 IOCA (WDT Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	-	-	PSWE	PSW2	PSW1	PSW0

Bit 7 (WDTE) Control bit used to enable the Watchdog timer

0 : Disable WDT

1 : Enable WDT

WDTE is both readable and writable.

Bit 6 (EIS): Control bit used to define the function of P60 (/INT) pin

0 : P60, bidirectional I/O pin

1 : /INT, external interrupt pin. In this case, the I/O control bit of P60 (Bit 0 of IOC6) must be set to "1".

When EIS is "0", the path of /INT is masked. When EIS is "1", the status of /INT pin can also be read by way of reading Port 6 (R6). Refer to Fig 6-5 (a).

EIS is both readable and writable.

Bits 5~4: Not used, set to “0” at all time

Bit 3 (PSWE): Prescaler enable bit for WDT

0 : prescaler disable bit, WDT rate is 1:1

1 : prescaler enable bit, WDT rate is set as Bit 0~Bit 2

Bit 2 (PSW2) ~ Bit 0 (PSW0): WDT prescaler bits

PSW2	PSW1	PSW0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.2.5 IOCB (Pull-down Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PD7	/PD6	/PD5	/PD4	/PD3	/PD2	/PD1	/PD0

Bit 7 (/PD7): Control bit used to enable the of P63 pull-down pin

0 : Enable internal pull-down

1 : Disable internal pull-down

Bit 6 (/PD6): Control bit used to enable the P62 pull-down pin

Bit 5 (/PD5): Control bit used to enable the P61 pull-down pin

Bit 4 (/PD4): Control bit used to enable the P60 pull-down pin

Bit 3 (/PD3): Control bit used to enable the P53 pull-down pin

Bit 2 (/PD2): Control bit used to enable the P52 pull-down pin

Bit 1 (/PD1): Control bit used to enable the P51 pull-down pin

Bit 0 (/PD0): Control bit used to enable the P50 pull-down pin

The IOCB Register is both readable and writable.

6.2.6 IOCC (Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0

Bit 7 (OD7): Control bit used to enable the open-drain output of P67 pin

0 : Disable open-drain output

1 : Enable open-drain output

Bit 6 (OD6): Control bit used to enable the open-drain output of P66 pin

Bit 5 (OD5): Control bit used to enable the open-drain output of P65 pin

Bit 4 (OD4): Control bit used to enable the open-drain output of P64 pin

Bit 3 (OD3): Control bit used to enable the open-drain output of P63 pin

Bit 2 (OD2): Control bit used to enable the open-drain output of P62 pin

Bit 1 (OD1): Control bit used to enable the open-drain output of P61 pin

Bit 0 (OD0): Control bit used to enable the open-drain output of P60 pin

The IOCC Register is both readable and writable.

6.2.7 IOCD (Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH7	/PH6	/PH5	/PH4	/PH3	/PH2	/PH1	/PH0

Bit 7 (/PH7): Control bit used to enable the P67 pull-high pin.

0 : Enable internal pull-high

1 : Disable internal pull-high

Bit 6 (/PH6): Control bit used to enable the P66 pull-high pin

Bit 5 (/PH5): Control bit used to enable the P65 pull-high pin

Bit 4 (/PH4): Control bit used to enable the P64 pull-high pin

Bit 3 (/PH3): Control bit used to enable the P63 pull-high pin

Bit 2 (/PH2): Control bit used to enable the P62 pull-high pin

Bit 1 (/PH1): Control bit used to enable the P61 pull-high pin

Bit 0 (/PH0): Control bit used to enable the P60 pull-high pin

The IOCD Register is both readable and writable.

6.2.8 IOCF (Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDIE	-	-	-	-	EXIE	ICIE	TCIE

Bit 7 (LVDIE): LVDIF interrupt enable bit

0 : disable LVDIF interrupt

1 : enable LVDIF interrupt

Bits 6~3: Not used, set to “0” at all time

Bit 2 (EXIE): EXIF interrupt enable bit

0 : disable EXIF interrupt

1 : enable EXIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit

0 : disable ICIF interrupt

1 : enable ICIF interrupt

Bit 0 (TCIE): TCIF interrupt enable bit

0 : disable TCIF interrupt

1 : enable TCIF interrupt

Individual interrupt is enabled by setting its associated control bit in the IOCF to "1".

Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Fig 6-8.

The IOCF register is both readable and writable.

6.3 TCC/WDT & Prescaler

There are two 8-bit counters available as prescalers for the TCC and WDT respectively. The PST0~PST2 bits of the CONT register are used to determine the ratio of the prescaler of TCC. Likewise, the PSW0~PSW2 bits of the IOCE0 register are used to determine the WDT prescaler. The prescaler counter will be cleared by the instructions each time they are written into TCC. The WDT and prescaler will be cleared by the "WDTC" and "SLEP" instructions. Fig 6-3 depicts the circuit diagram of TCC/WDT.

R1 (TCC) is an 8-bit timer/counter. The clock source of TCC can be internal clock or external signal input (edge selectable from the TCC pin). If TCC signal source is from the internal clock, TCC will be incremented by 1 at every instruction cycle (without prescaler). As illustrated in Fig 6-3, selection of CLK=Fosc/2 or CLK=Fosc/4 depends on the Code Option bit <CLKS>. CLK=Fosc/2 is selected if the CLKS bit is "0", and CLK=Fosc/4 is selected if the CLKS bit is "1". If TCC signal source is from external clock input, TCC will be incremented by 1 at every falling edge or rising edge of the TCC pin. TCC pin input time length (kept in High or low level) must be greater than 1CLK. The TCC will stop running when sleep mode occurs.

The watchdog timer is a free running on-chip RC oscillator. The WDT will keep on running even after the oscillator driver has been turned off (i.e. in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during normal mode by software programming. Refer to WDTE bit of IOCE0 register. With no prescaler, the WDT time-out period is approximately 18 ms[1] (one oscillator start-up timer period).

It is recommended to use Port 6 Input Status Change Interrupt if user wants to use the Interrupt function.

[1] **Note:** VDD=5V, WDT time-out period = 16.5ms ± 8% VDD=3V
WDT time-out period = 18ms ± 8%.

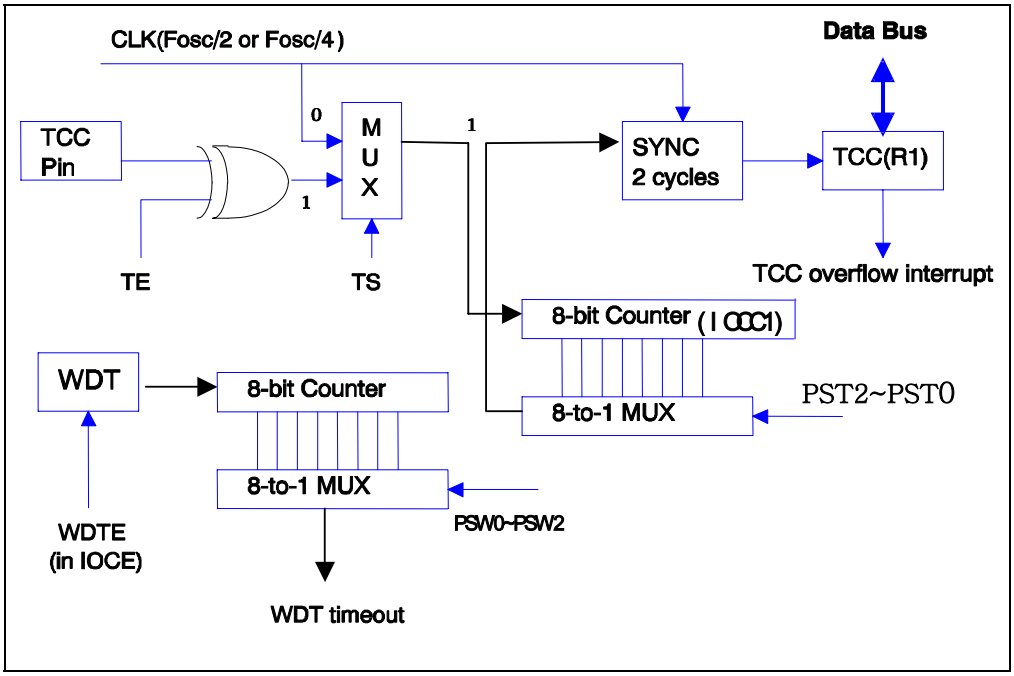


Fig. 6-3 Block Diagram of TCC and WDT

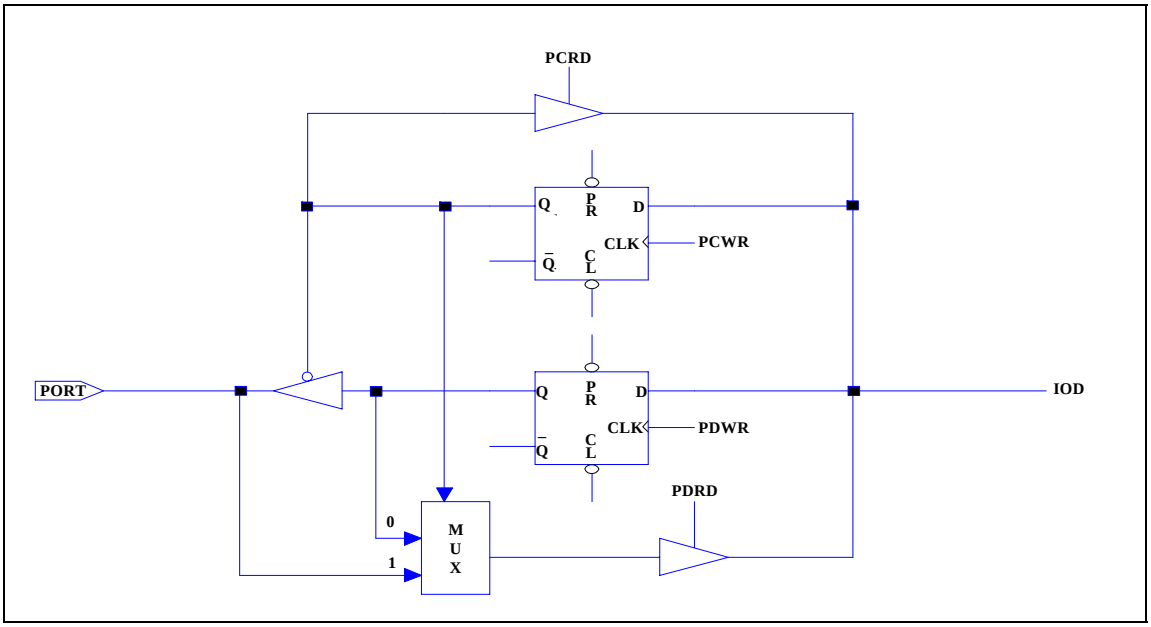
Table 5 Internal RC Drift Rate (Ta=25°C, VDD=2.3V~5.5 V, VSS=0V)

Internal RC	Drift Rate			
	Temperature (-40°C~85°C)	Voltage	Process	Total
16.5 ms	± 3%	5V	± 5%	±8%
18 ms	± 3%	3V	± 5%	± 8%

6.4 I/O Ports

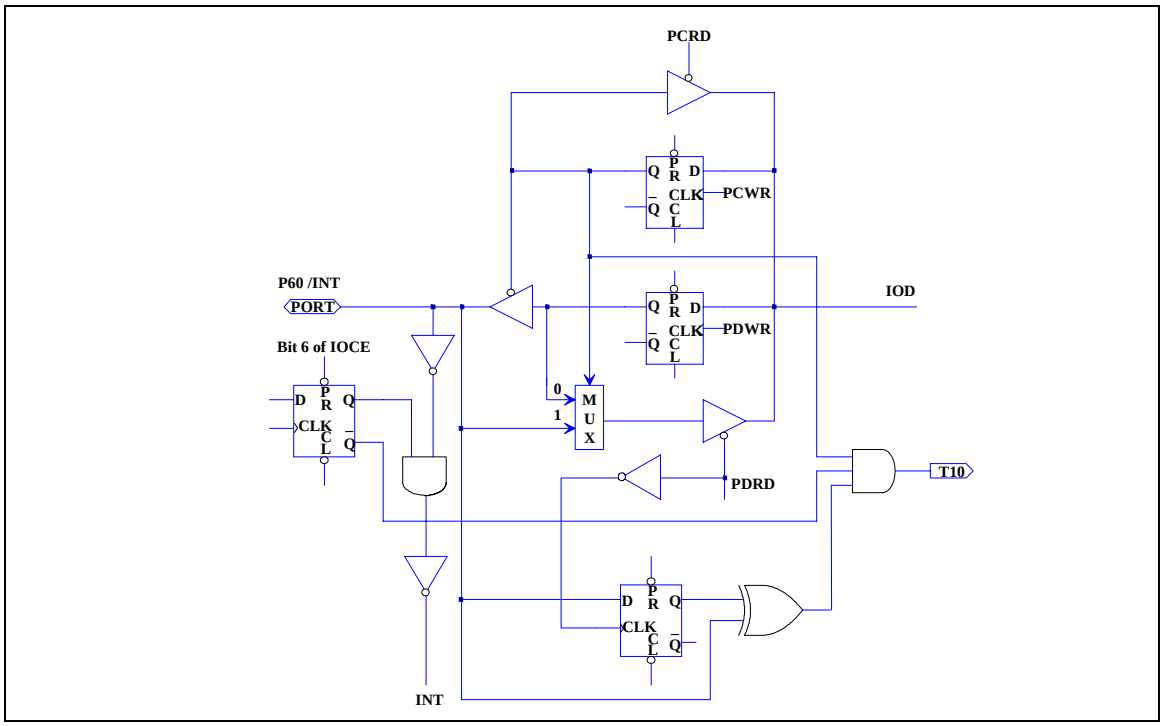
The I/O registers, Port 5, Port 6 and Port 7, are bidirectional tri-state I/O ports. Port 6 can be pulled high internally by software. In addition, Port 6 can also have open-drain output by software. Input status change interrupt (or wake-up) function on Port 6 P50 ~ P53 and P60 ~ P63 pins can be pulled down by software. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC7). When Port 7.0 is set as output, the internal circuit becomes open-drain, so it must be tied to pull-high to work normally.

The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5, Port 6 and Port 7 are shown in the following Figures 6-4, 6-5 (a), 6-5 (b), and Figure 6-6.



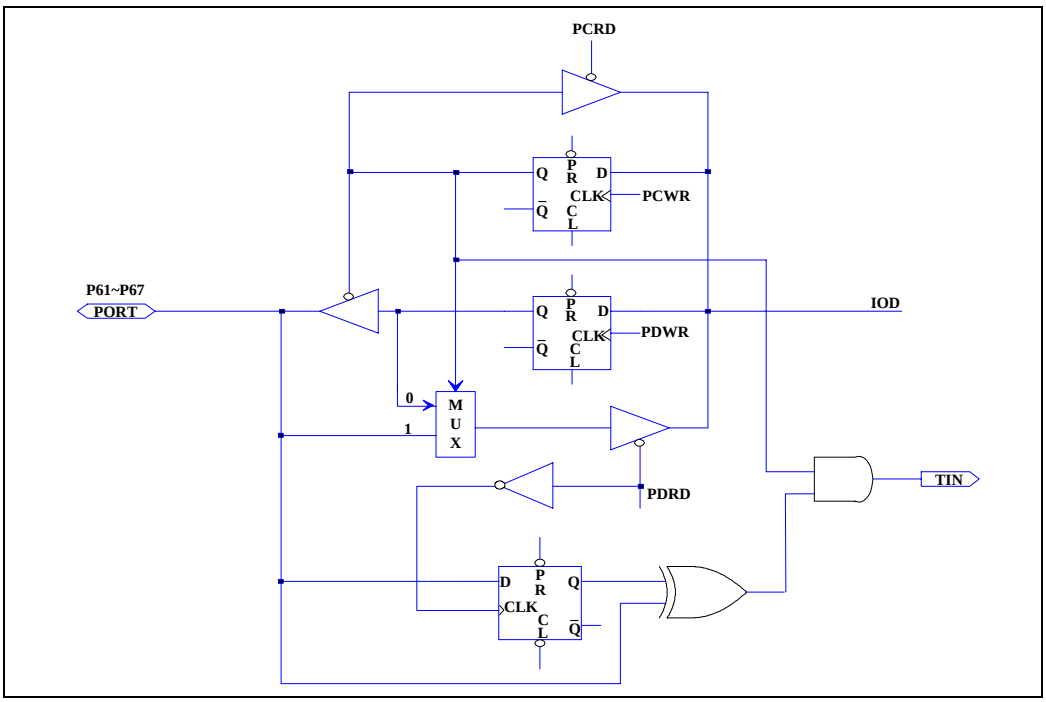
Note: Pull-down is not shown in the figure.

Fig. 6-4 Port 5 and Port 7.0 I/O Port and I/O Control Register Circuit



Note: Pull-high (down) and Open-drain are not shown in the figure.

Fig. 6-5 (a) P60 (/INT) I/O Port and I/O Control Register Circuit



Note: Pull-high (down) and Open-drain are not shown in the figure.

Fig. 6-5 (b) P61~P67 I/O Port and I/O Control Register Circuit

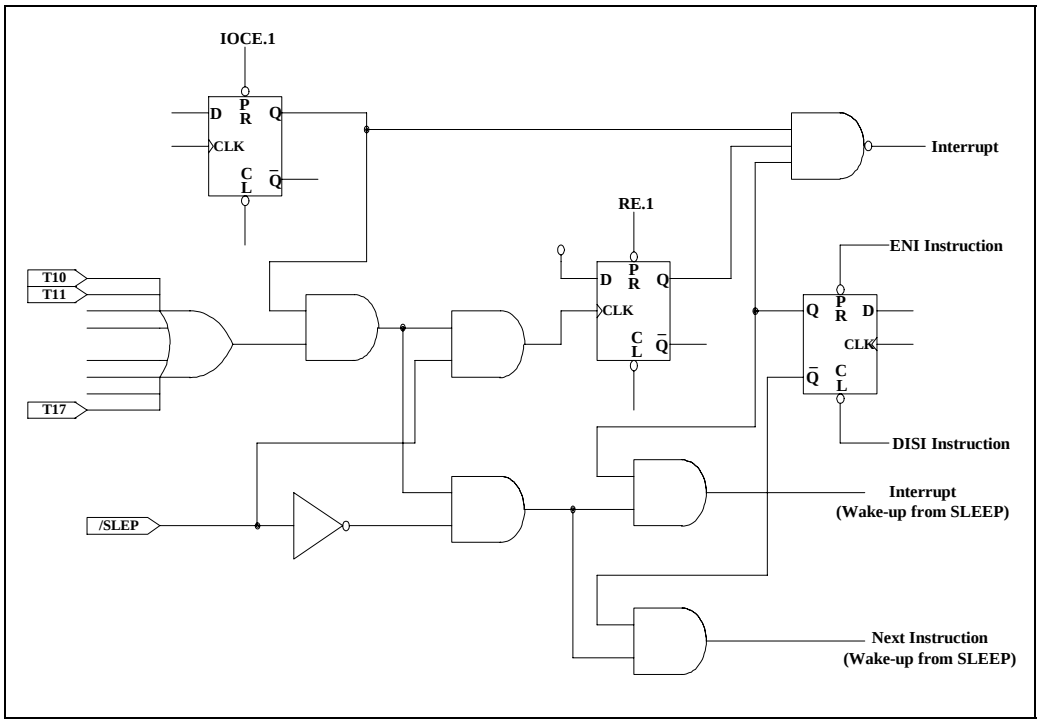


Fig. 6-5 (c) Block Diagram of I/O Port 6 with Input Change Interrupt/Wake-up

Table 6 Usage of Port 6 Input Change Wake-up/Interrupt Function

Usage of Port 6 Input Status Change Wake-up/Interrupt	
(I) Wake-up from Port 6 Input Status Change (a) Before Sleep 1. Disable WDT[2] (use this very carefully) 2. Read I/O Port 6 (MOV R6,R6) 3 a. Enable interrupt (Set IOCF.1), after wake-up if "ENI" switch to interrupt vector (006H), if "DISI" excute next instruction 3 b. Disable interrupt (Set IOCF.1), always execute next instruction 4. Enable wake-up enable bit (Set RA.6) 5 a. Execute "SLEP" instruction b. After Wake-up 1. IF "ENI" → Interrupt vector (006H) 2. IF "DISI" → Next instruction	(II) Port 6 Input Status Change Interrupt 1. Read I/O Port 6 (MOV R6,R6) 2. Execute "ENI" 3. Enable interrupt (Set IOCF.1) 4. IF Port 6 change (interrupt) → Interrupt vector (006H)

6.5 Reset and Wake-up

6.5.1 Reset

A reset is initiated by one of the following events:

(1) Power-on reset

(2) /RESET pin input "low", or

(3) WDT time-out (if enabled)

The device is kept in a reset condition for a period of approx. 18ms[3] (one oscillator start-up timer period) after the reset is detected. And if the /Reset pin goes "low" or WDT time-out is active, a reset is generated, in RC mode the reset time is 34 clocks, High crystal mode reset time is 2ms and 32clocks. In low crystal mode, the reset time is 500ms. Once a reset occurs, the following functions are performed. Refer to Fig 6-7.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog timer and prescaler are cleared.

[2] **Note:** Software disables WDT (watchdog timer) but hardware must be enabled before applying Port 6 Change Wake-Up function. (Code Option Register and Bit 11 (ENWDTB-) set to "1").

[3] **Note:** Vdd = 5V, set up time period = 16.8ms ± 8%
Vdd = 3V, set up time period = 18ms ± 8%

- When power is switched on, the upper three bits of R3 are cleared.
- The bits of the RB, RC, RD, RD, RE registers are set to their previous status.
- The bits of the CONT register are set to all "1" except for Bit 6 (INT flag).
- The bits of the IOCA register are set to all "1".
- The bits of the IOCB register are set to all "1".
- The IOCC register is cleared.
- The bits of the IOCD register are set to all "1".
- Bit 7 of the IOCE register is set to "1", and Bits 4 and 6 are cleared.
- Bits 0~2 of RF and Bits 0~2 of IOCF register are cleared.

Sleep (power down) mode is asserted by executing the “SLEP” instruction. While entering sleep mode, WDT (if enabled) is cleared but keeps on running. After a wake-up, in RC mode the wake-up time is 34 clocks, High crystal mode wake-up time is 2 ms and 32 clocks. In low crystal mode, wake-up time is 500 ms. The controller can be awakened by:

(1) External reset input on /RESET pin

(2) WDT time-out (if enabled), or

(3) Port 6 input status changes (if enabled)

The first two cases will cause the EM78F651N to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). The third case must set RA bit6, the 1 bit decide what’s wake-up source to wake-up EM78F651N. Before SLEP instruction, enable the IOCF.1, the third case is considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) decides whether or not the controller branches to the interrupt vector following wake-up. If ENI is executed before SLEP, the instruction will begin to execute from the address 006H after wake-up. If DISI is executed before SLEP, the operation will restart from the succeeding instruction right next to SLEP after wake-up. In IOCF.1 disable before SLEP instruction, after wake-up EM78F651N will restart and execute next instruction sequentially.

In Case 2, can be enabled before entering the sleep mode and Case 3, must be disabled. That is,

[a] if Port 6 Input Status Change Interrupt and External interrupt(/INT) are enabled before SLEP, WDT must be disabled by software. However, the WDT bit in the option register remains enabled. Hence, the EM78F651N, can be awakened only by Case 1 or 3.

[b] If WDT is enabled before SLEP, Port 6 Input Status Change wake-up and External interrupt (/INT) must be disabled. Hence, the EM78F651N, can be awakened only by Case 1 or 2. Refer to the section on Interrupt.

If Port 6 Input Status Change Interrupt is used to wake-up the EM78F651N, (Case [a] above), the following instructions must be executed before SLEP:

```
MOV A, @xx000110b ; Select internal TCC clock
CONTW
CLR R1            ; Clear TCC and prescaler
WDTC              ; Clear WDT and prescaler
MOV A, @0xxx1110b ; Select WDT prescaler & disable WDT
IOW RA
MOV R6, R6        ; Read Port 6
MOV A, @00000x1xb ; Enable Port 6 input change interrupt
IOW RF
ENI (or DISI)     ; Enable (or disable) global interrupt
SLEP              ; Sleep
NOP
```

One problem user should be aware of, is that after waking up from sleep mode, WDT would be enabled automatically. The WDT operation (being enabled or disabled) should be handled appropriately by software after waking up from sleep mode.

Table 7 Summary of Registers Initialized Values

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC5	Bit Name	C57	C56	C55	C54	C53	C52	C51	C50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC6	Bit Name	C67	C66	C65	C64	C63	C62	C61	C60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC7	Bit Name	C77	-	-	-	-	-	-	-
		Power-on	1	U	U	U	U	U	U	U
		/RESET and WDT	1	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	CONT	Bit Name	×	/INT	TS	TE	PAB	PSR2	PSR1	PSR0
		Power-on	1	0	1	1	1	1	1	1
		/RESET and WDT	1	0	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x01	R1 (TCC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x02	R2 (PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	*0/P	*0/P	*0/P	*0/P	*1/P	*0/P	*0/P	*0/P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x03	R3 (SR)	Bit Name	GP2	GP1	GP0	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	t	t	P	P	P
		Wake-up from Pin Change	P	P	P	t	t	P	P	P
0x04	R4 (RSR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	U	U	U	U	U	U
		/RESET and WDT	0	0	P	P	P	P	P	P
		Wake-up from Pin Change	0	0	P	P	P	P	P	P
0x05	P5	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x06	P6	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x07	P7	Bit Name	P77	×	×	×	×	×	×	×
		Power-on	U	0	0	0	0	0	0	0
		/RESET and WDT	P	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	0	0	0	0	0	0	0
0x7~0x9	R7~R9	Bit Name	-	-	-	-	-	-	-	-
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0XA	RA (WCR)	Bit Name	-	ICWE	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	P	0	0	0	0	0	0
		Wake-up from Pin Change	0	P	0	0	0	0	0	0

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0XB	RB (ECR)	Bit Name	RD	WR	EEWE	EEDF	EEPC	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	P	P	P	P	P	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	0	0	0
0XC	RC	Bit Name	-	EE_A5	EE_A5	EE_A4	EE_A3	EE_A2	EE_A1	EE_A0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	P	P	P	P	P	P	P
		Wake-up from Pin Change	0	P	P	P	P	P	P	P
0XD	RD	Bit Name	EE_D7	EE_D6	EE_D5	EE_D4	EE_D3	EE_D2	EE_D1	EE_D0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0XE	RE	Bit Name	-	-	-	-	LVDEN	/LVD	LVD1	LVD0
		Power-on	0	0	0	0	0	1	0	0
		/RESET and WDT	0	0	0	0	0	1	0	0
		Wake-up from Pin Change	0	0	0	0	P	P	P	P
0x0F	RF(ISR)	Bit Name	LVDHIF	×	×	×	×	EXIF	ICIF	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	U	U	U	U	0	0	0
		Wake-up from Pin Change	P	U	U	U	U	P	P	P
0x0A	IOCA	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0B	IOCB	Bit Name	/PD7	/PD6	/PD5	/PD4	/PD3	/PD2	/PD1	/PD0
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0C	IOCC	Bit Name	OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0D	IOCD	Bit Name	/PH7	/PH6	/PH5	/PH4	/PH3	/PH2	/PH1	/PH0
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0E	IOCE	Bit Name	WDTE	EIS	×	×	PSWE	PSW2	PSW1	PSW0
		Power-on	1	0	U	0	1	1	1	1
		/RESET and WDT	1	0	U	0	1	1	1	1
		Wake-up from Pin Change	1	P	U	P	P	P	P	P
0x0F	IOCF	Bit Name	×	×	×	×	×	EXIE	ICIE	TCIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	U	U	U	U	U	P	P	P
0x10~0x2F	R10~R2F	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Legend: **"×"** = not used **"P"** = previous value before reset
"u" = unknown or don't care **"t"** = check Table 8

* To jump Address 0x08, or to execute the instruction next to the "SLEP" instruction.

6.5.2 Status of RST, T, and P of the Status Register

A reset condition is initiated by the following events:

1. Power-on condition

2. High-low-high pulse on /RESET pin

3. Watchdog timer time-out

The values of T and P, listed in Table 8 are used to check how the processor wakes up. Table 9 shows the events that may affect the status of T and P.

Table 8 Values of RST, T and P after Reset

Reset Type	T	P
Power on	1	1
/RESET during Operating mode	*P	*P
/RESET wake-up during Sleep mode	1	0
WDT during Operating mode	0	*P
WDT wake-up during Sleep mode	0	0
Wake-Up on pin change during Sleep mode	1	0

* P: Previous status before reset

Table 9 Status of T and P Being Affected by Events.

Event	T	P
Power on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-Up on pin change during SLEEP mode	1	0

* P: Previous value before reset

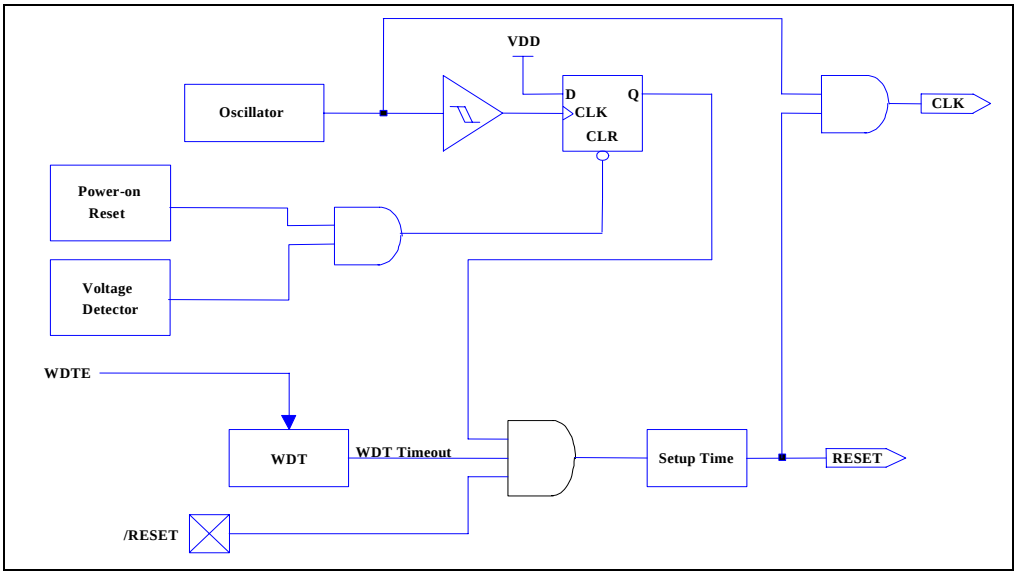


Fig. 6-6 Block Diagram of Controller Reset

6.6 Interrupt

The EM78F651N, has three falling-edge interrupts listed below:

(1) TCC overflow interrupt

(2) Port 6 Input Status Change interrupt

(3) External interrupt [(P60, /INT) pin]

(4) LVD (Low Voltage Detector) interrupt

RF is the interrupt status register that records the interrupt requests in the relative flags/bits. IOCF is the interrupt mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the enabled interrupts occurs, the next instruction will be fetched from address in the priority as shown in Table 10. Once in the interrupt service routine, the source of an interrupt can be determined by polling the flag bits in RF. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and before interrupts are enabled to avoid recursive interrupts.

When an interrupt is generated by the LVD (low voltage detector), in the code option enable LVD interrupt is selected, the next instruction will be fetched from address 00CH.

When an interrupt is generated by the Timer clock/counter (if enabled), the next instruction will be fetched from address 009 (TCC).

Before the Port 6 Input Status Change Interrupt is enabled, reading Port 6 (e.g. "MOV R6,R6") is necessary. Each Port 6 pin will have this feature if its status changes. The Port 6 Input Status Change Interrupt will wake up the EM78F651N from sleep mode if it is enabled prior to going into sleep mode by executing SLEP instruction. When wake-up occurs, the controller will continue to execute program in-line if the global interrupt is disabled. If the global interrupt is enabled, it will branch out to the interrupt vector 006H.

External interrupt equipped with digital noise rejection circuit (input pulse less than **8 system clocks time** is eliminated as noise), **but in Low crystal oscillator (LXT) mode the noise rejection circuit will be disabled.** When an interrupt (Falling edge) is generated by the External interrupt (when enabled), the next instruction will be fetched from address 003H.

The flag (except ICIF bit) in the Interrupt Status Register (RF) is set regardless of the status of its mask bit or the execution of ENI. Note that the outcome of RF will be the logic AND of RF and IOCF (refer to Fig 6-8). The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

Before the interrupt subroutine is executed, the contents of ACC and the R3 and R4 register will be saved by hardware. If another interrupt occurred, the ACC, R3 and R4 will be replaced by the new interrupt. After the interrupt service routine is finished, ACC, R3 and R4 will be pushed back.

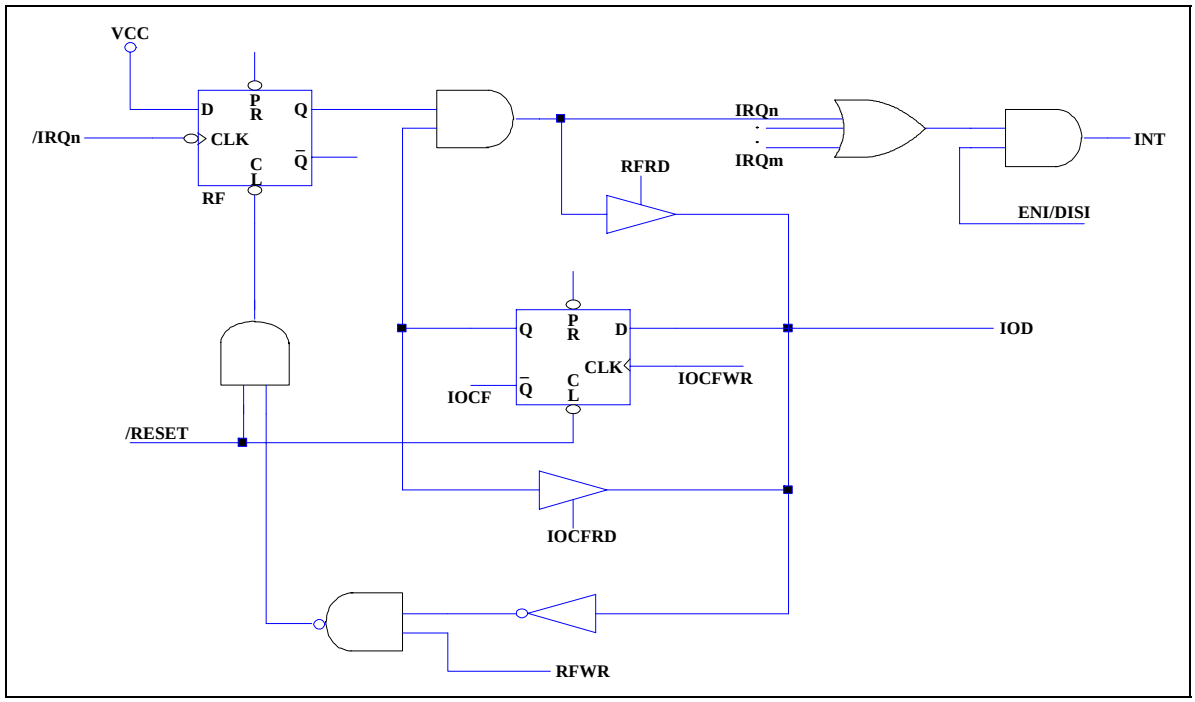


Fig. 6-7 Interrupt Input Circuit

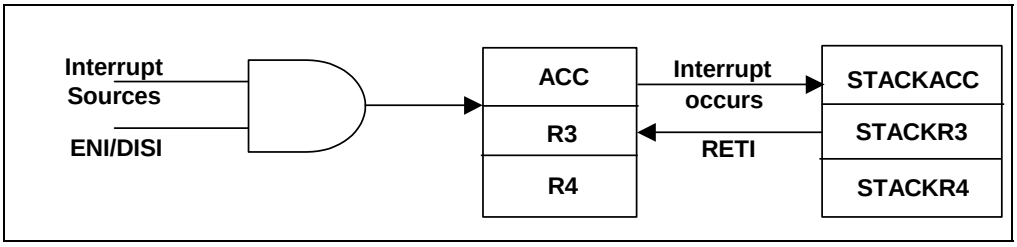


Fig. 6-8 Interrupt Back-up Diagram

Table 10 Interrupt Vector

Interrupt Vector	Interrupt Status	Priority
003H	External interrupt	1
006H	Port 6 pin change	2
009H	TCC overflow interrupt	3
00CH	LVD interrupt	4

Note: Priority is in descending order, i.e. 1 is the highest priority, 4 is the lowest priority

6.7 LVD (Low Voltage Detector)

During power source unstable situations, such as external power noise interference or EMS test condition, it will cause the power to vibrate fiercely. At the time Vdd is unsettled, it is probably below the working voltage. When the system supply voltage,

Vdd, is below the working voltage, the IC kernel must keep all register status automatically.

LVD property is set at Register RE, Bit 1, 0 detailed operation mode is as follows:

Bits 1~Bit 0 (LVD1~LVD0): Low Voltage Detect level control Bits.

LVD1	LVD0	LVD Voltage Interrupt Level
0	0	2.1
0	1	3.1
1	0	3.8
1	1	4.3

The LVD status and interrupt flag is referred to as RF

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RF	LVDIF	-	-	-	-	EXIF	ICIF	TCIF

Bit 7 (LVDIF): Low voltage Detector interrupt flag.

When LVD1, LVD0 = “0, 0”, Vdd > 2.3V, LVDIF is “0”, Vdd ≤ 2.3V, set LVDIF to “1”. LVDIF is reset to “0” by software.

When LVD1, LVD0 = “0, 1”, Vdd > 3.3V, LVDIF is “0”, Vdd ≤ 3.3V, set LVDIF to “1”. LVDIF is reset to “0” by software.

When LVD1, LVD0 = “1, 0”, Vdd > 4.0V, LVDIF is “0”, Vdd ≤ 4.0V, set LVDIF to “1”. LVDIF is reset to “0” by software.

When LVD1, LVD0 = “1, 1”, Vdd > 4.5V, LVDIF is “0”, Vdd ≤ 4.5V, set LVDIF to “1”. LVDIF is reset to “0” by software.

The following steps are needed to setup the LVD function:

Set the LVDEN of Register RE to “1”, then use Bit 1, 0 (LVD1, LVD0) of Register RE to set LVD interrupt level

Wait for LVD interrupt to occur.

Clear LVD interrupt flag

The internal LVD module uses internal circuit to fit. When the LVDEN is set to enable the LVD module, the current consumption will increase to about 10μA.

During sleep mode, the LVD module continues to operate. If the device voltage drops slowly and crosses the detect point, the LVDIF bit will be set and the device won’t wake-up from Sleep mode. Until the other wake-up sources wake up the device, the LVD interrupt flag is still set at the prior status.

When the system resets, the LVD flag will be cleared.

Figure 6-9 shows the LVD module to detect the external voltage situation.

When Vdd drops not below V_{LVD}, LVDIF remain at “0”.

When Vdd drops below V_{LVD}, LVDIF is set to “1”. If global ENI enable, LVDIF will be set to “1”, the next instruction will branch to interrupt vector. The LVD interrupt flag is cleared to “0” by software.

When Vdd drops below V_{RESET} and is less than 80µs, the system will all maintain the register status and system halt but oscillation is active. When Vdd drops below V_{RESET} and is more than 80µs, a system reset will occur, and for the following waveform situation, refer to Section 6.5.1 Reset Description.

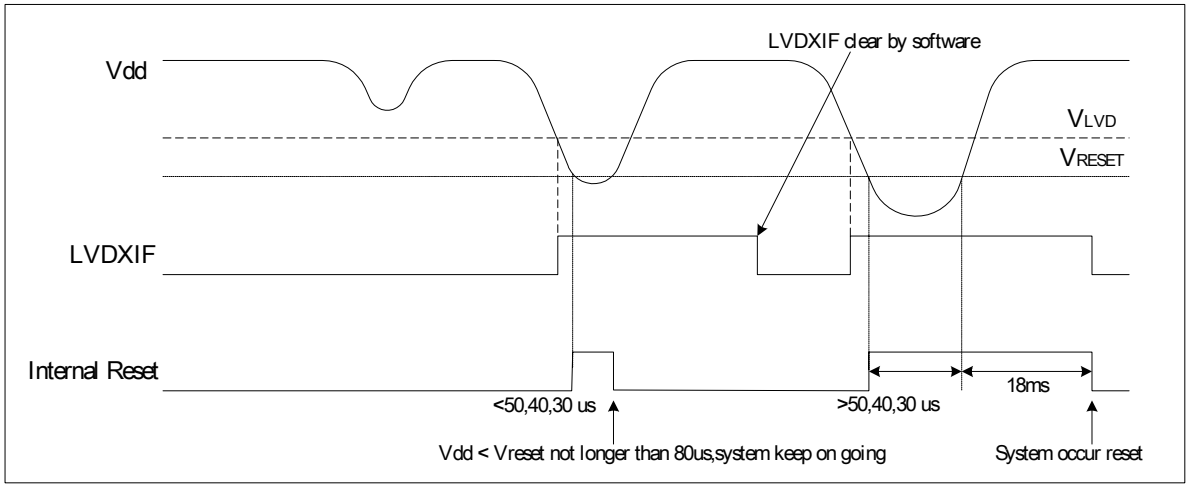


Fig. 6-9 LVD Waveform Situation

6.8 Data EEPROM

The Data EEPROM is readable and writable during normal operation over the whole Vdd range. The operation for Data EEPROM is base on a single byte. A write operation makes an erase-then-write cycle to take place on the allocated byte.

The Data EEPROM memory provides high erase and write cycles. A byte write automatically erases the location and writes the new value.

6.8.1 Data EEPROM Control Register

6.8.1.1 RB (EEPROM Control Register)

The EECR (EEPROM Control Register) is the control register for configuring and initiating the control register status.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RD	WR	EEWE	EEDF	EEPC	-	-	-

Bit 7 : Read control register

0 : Does not execute EEPROM read

1 : Read EEPROM content, (RD can be set by software, RD is cleared by hardware after Read instruction is completed)

Bit 6 : Write control register

0 : Write cycle to the EEPROM is complete.

1 : Initiate a write cycle, (WR can be set by software, WR is cleared by hardware after Write cycle is completed)

Bit 5：EEPROM Write Enable bit

0 : Prohibit write to the EEPROM

1 : Allows EEPROM write cycles.

Bit 4：EEPROM Detect Flag

0 : Write cycle is completed

1 : Write cycle is unfinished

Bit 3：EEPROM power-down control bit

0 : Switch off the EEPROM

1 : EEPROM is operating

Bits 2 ~ 0: Not used, set to “0” at all time

6.8.1.2 RC (128 Bytes EEPROM Address)

When accessing the EEPROM data memory, the RC (128 bytes EEPROM address register) holds the address to be accessed. According the operation, the RD (128 bytes EEPROM Data register) holds the data to written, or the data read, at the address in RC.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	EE_A6	EE_A5	EE_A4	EE_A3	EE_A2	EE_A1	EE_A0

Bit 7： Not used, fixed at “0”.

Bits 6 ~ 0： 128 bytes EEPROM address

6.8.1.3 RD (128 Bytes EEPROM Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EE_D7	EE_D6	EE_D5	EE_D4	EE_D3	EE_D2	EE_D1	EE_D0

Bits 7 ~ 0： 128 bytes EEPROM data

6.8.2 Programming Step / Example Demonstration

6.8.2.1 Programming Step

Follow these steps to write or read data from the EEPROM:

(1) Set the RC.EEPC bit to 1 for enable EEPROM power.

(2) Write the address to RC (128 bytes EEPROM address).

a.1. Set the RC.EEWE bit to 1, if the write function is employed.

a.2. Write the 8-bit data value to be programmed in the RD (128 bytes EEPROM data)

a.3. Set the RC.WR bit to 1, then execute write function

b. Set the RC.READ bit to 1, after which, execute read function

(3) a. Wait for the RC.EEDF or RC.WR to be cleared

b. Wait for the RC.EEDF to be cleared

(4) For the next conversion, go to Step 2 as required.

(5) If user wants to save power and to make sure the EEPROM data is not used, clear the RC.EEPC.

6.8.2.2 Example Demonstration Programs

```
;To define the control register
;Write data to EEPROM
RC == 0x0C
RB == 0x0B
RD == 0x0D
Read == 0x07
WR == 0x06
EEWE == 0x05
EEDF == 0x04
EEPC == 0x03

BS RB, EEPC      ; Set the EEPROM power on
MOV A,@0x0A
MOV RC,A         ; Assign the address from EEPROM
BS RB, EEWE      ; Enable the EEPROM write function
MOV A,@0x55
MOV RD,A         ; Set the data for EEPROM
BS RB,WR         ; Write value to EEPROM
JBC RB,EEDF      ; To check the EEPROM bit complete or not
JMP $-1

;To define the control register
;Read data from EEPROM
RC == 0x0C
RD == 0x0D
Read == 0x07
WR == 0x06
EEWE == 0x05
EEDF == 0x04
EEPC == 0x03

BS RB, EEPC      ; Set the EEPROM power on
MOV A,@0x0A
MOV RC,A         ; Assign the address from EEPROM
BS RB, Read      ; Set EEPROM read function
JBC RB,EEDF      ; To check the EEPROM bit complete or not
JMP $-1
MOV A,RD
```

6.9 Oscillator

6.9.1 Oscillator Modes

The device can be operated in four different oscillator modes, such as Internal RC oscillator mode (IRC), External RC oscillator mode (ERC), High Crystal oscillator mode (HXT), and Low Crystal oscillator mode (LXT). User can select one of such modes by programming OSC2, OCS1 and OSC0 in the Code Option register. Table11 depicts how these four modes are defined.

The up-limited operation frequency of the crystal/resonator on the different VDD is listed in Table 11

Table 11 Oscillator Modes defined by OSC2 ~ OSC0

Mode	OSC2	OSC1	OSC0
XT (Crystal oscillator mode)	0	0	0
HXT (High Crystal oscillator mode)	0	0	1
LXT1 (Low Crystal 1 oscillator mode)	0	1	0
LXT2 (Low Crystal 2 oscillator mode)	0	1	1
IRC mode, OSCO (P54) act as I/O pin	1	0	0
IRC mode, OSCO (P54) act as RCOUT pin	1	0	1
ERC mode, OSCO (P54) act as I/O pin	1	1	0
ERC mode, OSCO (P54) act as RCOUT pin	1	1	1

NOTE

1. Frequency range of HXT mode is 20MHz ~ 6MHz.
2. Frequency range of XT mode is 6MHz ~ 1MHz.
3. Frequency range of LXT1 mode is 1MHz ~ 100kHz.
4. Frequency range of XT mode is 32kHz.

Table 12 Summary of Maximum Operating Speeds

Conditions	VDD	Max Fxt. (MHz)
Two cycles with two clocks	2.5	4.0
	3.0	8.0
	5.0	20.0

6.9.2 Crystal Oscillator/Ceramic Resonators (Crystal)

The EM78F651N can be driven by an external clock signal through the OSCI pin as shown in Fig 6-10 below.

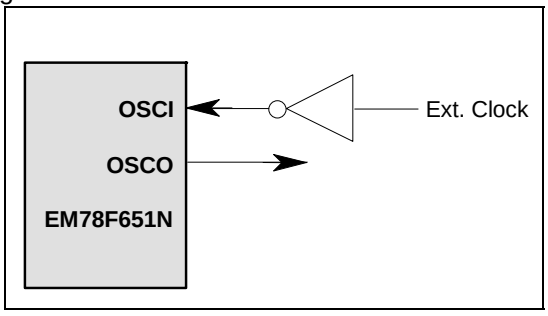


Fig. 6-10 Circuit for External Clock Input

In most applications, pin OSCI and pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation. Fig 6-11 depicts such circuit. The same thing applies whether it is in the HXT mode or in the LXT mode. Table 13 provides the recommended values of C1 and C2. Since each resonator has its own attribute, user should refer to its specification for appropriate values of C1 and C2. RS, a serial resistor, may be necessary for AT strip cut crystal or low frequency mode.

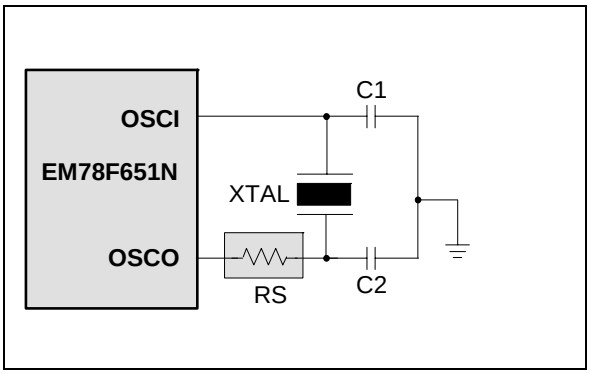


Fig. 6-11 Circuit for Crystal/Resonator

Table 13 Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonator

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Ceramic Resonators	HXT	455kHz	100~150	100~150
		2.0 MHz	20~40	20~40
		4.0 MHz	10~30	10~30
Crystal Oscillator	LXT	32.768kHz	25	15
		100kHz	25	25
		200kHz	25	25
	HXT	455kHz	20~40	20~150
		1.0MHz	15~30	15~30
		2.0MHz	15	15
		4.0MHz	15	15

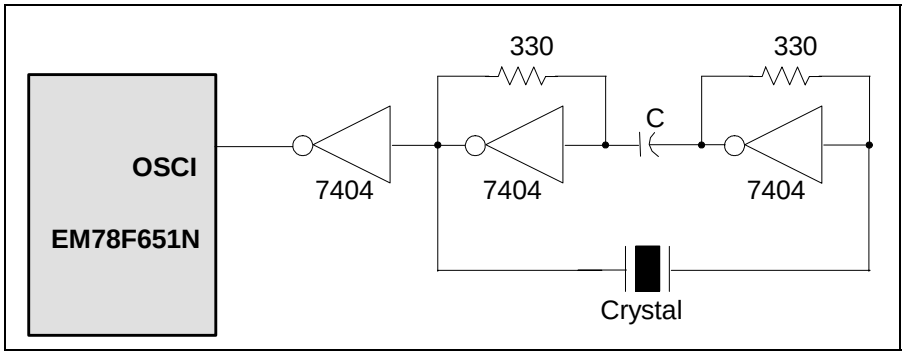


Fig. 6-12 Circuit for Crystal/Resonator-Series Mode

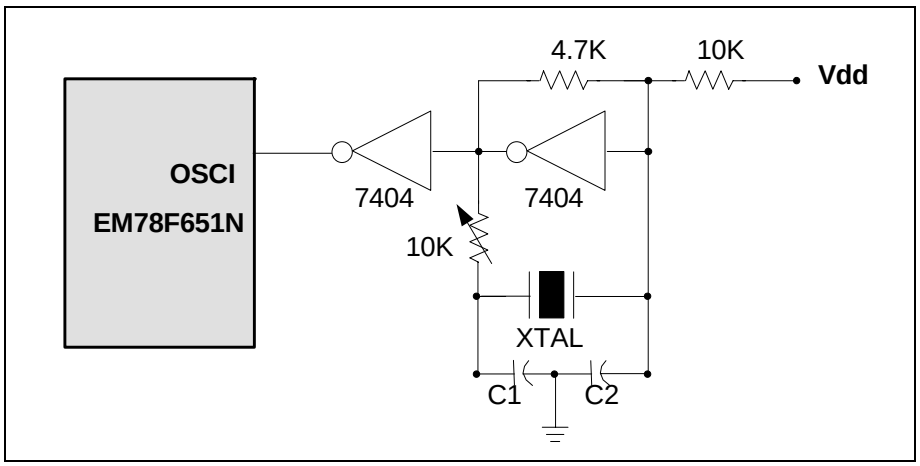


Fig. 6-13 Circuit for Crystal/Resonator-Parallel Mode

6.9.3 External RC Oscillator Mode

For some applications that do not need a very precise timing calculation, the RC oscillator (Fig 6-14) offers a cost-effective oscillator configuration.. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (Rext), the capacitor (Cext), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to manufacturing process variation.

In order to maintain a stable system frequency, the values of the Cext should not be less than 20pF, and that the value of Rext should not be greater than 1 MΩ. If they cannot be kept in this range, the frequency is easily affected by noise, humidity, and leakage.

The smaller the Rext in the RC oscillator, the faster its frequency will be. On the contrary, for very low Rext values, for instance, 1 KΩ, the oscillator becomes unstable since the NMOS cannot discharge correctly the current of the capacitance.

Based on the above reasons, it must be kept in mind that all of the supply voltage, the operation temperature, the components of the RC oscillator, the package types, and the PCB layout, will affect the system frequency.

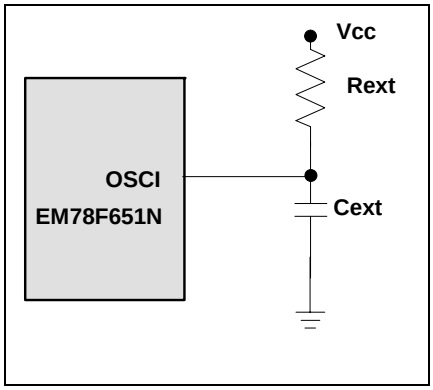


Fig. 6-14 Circuit for External RC Oscillator Mode

Table 14 RC Oscillator Frequencies

Cext	Rext	Average Fosc 5V, 25°C	Average Fosc 3V, 25°C
20 pF	3.3k	3.3 MHz	3 MHz
	5.1k	2.27 MHz	2.1 MHz
	10k	1.1 MHz	1.05 MHz
	100k	145kHz	145kHz
100 pF	3.3k	1.02 MHz	0.98 MHz
	5.1k	724kHz	694kHz
	10k	360kHz	360kHz
	100k	45kHz	47kHz
300 pF	3.3k	400kHz	380kHz
	5.1k	280kHz	270kHz
	10k	143kHz	140kHz
	100k	14kHz	14kHz

Note: [1]: Measured based on DIP packages.

[2]: The values are for design reference only.

6.9.4 Internal RC Oscillator Mode

EM78F651N offers a versatile internal RC mode with default frequency value of 4MHz. Internal RC oscillator mode has other frequencies (1MHz, 8MHz and 455kHz) that can be set by Code Option (Word 1), RCM1 and RCM0. All these four main frequencies can be calibrated by programming the Code Option (Word 1) bits, C4~C0. Table 15 describes a typical instance of the calibration.

Table 15 Internal RC Drift Rate (Ta=25°C, VDD=5 V± 5%, VSS=0V)

Internal RC	Drift Rate			
	Temperature (-40°C~85°C)	Voltage (2.3V~5.5V)	Process	Total
4MHz	± 3%	± 5%	± 3%	± 11%
16MHz	± 3%	± 5%	± 5%	± 13%
3.58MHz	± 3%	± 5%	± 5%	± 13%
455kHz	± 3%	± 5%	± 5%	± 13%

Table 16 Calibration Selections for Internal RC Mode

C4	C3	C2	C1	C0	*Cycle Time (ns)	*Frequency (MHz)
1	1	1	1	1	399	2.506
1	1	1	1	0	385	2.6
1	1	1	0	1	371	2.693
1	1	1	0	0	358	2.786
1	1	0	1	1	347	2.879
1	1	0	1	0	336	2.973
1	1	0	0	1	326	3.066
1	1	0	0	0	316	3.159

C4	C3	C2	C1	C0	*Cycle Time (ns)	*Frequency (MHz)
0	1	1	1	1	307	3.253
0	1	1	1	0	298	3.346
0	1	1	0	1	290	3.439
0	1	1	0	0	283	3.533
0	1	0	1	1	275	3.626
0	1	0	1	0	268	3.719
0	1	0	0	1	262	3.813
0	1	0	0	0	256	3.906
0	0	0	0	0	250	4.00
0	0	0	0	1	244	4.093
0	0	0	1	0	238	4.186
0	0	0	1	1	233	4.279
0	0	1	0	0	228	4.373
0	0	1	0	1	223	4.466
0	0	1	1	0	219	4.559
0	0	1	1	1	214	4.653
1	0	0	0	0	210	4.746
1	0	0	0	1	206	4.839
1	0	0	1	0	202	4.933
1	0	0	1	1	198	5.026
1	0	1	0	0	195	5.119
1	0	1	0	1	191	5.213
1	0	1	1	0	188	5.306
1	0	1	1	1	185	5.4

* 1.Theoretical values, for reference only. It depend on process.
2. Similar way of calculation is also applicable for low frequency mode.

6.10 Code Option Register

The EM78F651N has a Code option word that is not part of the normal program memory. The option bits cannot be accessed during normal program execution.

Code Option Register and Customer ID Register arrangement distribution:

Word 0	Word 1	Word 2
Bit 12~Bit 0	Bit 12~Bit 0	Bit 12~Bit 0

6.10.1 Code Option Register (Word 0)

Word 0					
Bit 12	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**
-	NRHL	NRE	CYES	CLKS1	CLKS0

Word 0						
Bit 6	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
ENWDTB	OSC2	OSC1	OSC0	PR2	PR1	PR0

Bit 12: Not used, set to "0" at all time.

Bit 11 (NRHL): Noise rejection high/low pulse define bit. INT pin is falling edge trigger.

1 : Pulses equal to 8/fc [s] is regarded as signal

0 : Pulses equal to 32/fc [s] is regarded as signal (default)

NOTE

The noise rejection function is turned off in the LXT2 and sleep mode.

Bit 10 (NRE): Noise rejection enable (depend on EM78F651N). INT pin is falling edge trigger.

1 : disable noise rejection

0 : enable noise rejection (default) but in Low Crystal oscillator (LXT) mode, the noise rejection circuit is always disabled

Bit 9 (CYES): Instruction cycle selection bit

1 : one instruction cycle (default)

0 : two instruction cycles

Bit 8~7 (CLKS1 and CLKS0): Instruction period option bit

Instruction Period	CLKS1	CLKS0
4 clocks	0	0
2 clocks	0	1
8 clocks	1	0
16 clocks	1	1

Refer to the section on Instruction Set.

Bit 6 (ENWDTB): Watchdog timer enable bit

1 : Enable

0 : Disable

Bits 5~3 (OSC2 ~ OSC0): Oscillator Mode Selection bits

Oscillator Modes defined by OSC2 ~ OSC0

Mode	OSC2	OSC1	OSC0
XT (Crystal oscillator mode)	0	0	0
HXT (High Crystal oscillator mode)	0	0	1
LXT1 (Low Crystal 1 oscillator mode)	0	1	0
LXT2 (Low Crystal 2 oscillator mode)	0	1	1
IRC mode, OSCO (P54) act as I/O pin	1	0	0
IRC mode, OSCO (P54) act as RCOUT pin	1	0	1
ERC mode, OSCO (P54) act as I/O pin	1	1	0
ERC mode, OSCO (P54) act as RCOUT pin	1	1	1

Note: 1. Frequency range of HXT mode is 20MHz ~ 6MHz.
2. Frequency range of XT mode is 6MHz ~ 1MHz.
3. Frequency range of LXT1 mode is 1MHz ~ 100kHz.
4. Frequency range of LXT2 mode is 32kHz.

Bit 2~0 (PR2~PR0): Protect Bit. PR2~PR0 are protect bits, protect type is as follows:

PR2	PR1	PR0	Protect
1	1	1	Enable
1	1	0	Enable
1	0	1	Enable
1	0	0	Enable
0	1	1	Enable
0	1	0	Enable
0	0	1	Enable
0	0	0	Disable

Word 1					
Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7
-	TCEN	-	SHE	C4	C3

Word 1						
Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C2	C1	C0	RCM1	RCM0	LVR1	LVR0

Bit 12: Not used, set to “1” at all time

Bit 11(TCEN): TCC enable bit

0 : P77/TCC is set as P77 (default)

1 : P77/TCC is set as TCC

Bit 10: Not used, set to “0” at all time.

Bit 9 (SHE): System Halt Enable Bit.

0 : Enable

1 : Disable

Bits 8, 7, 6, 5 and Bit 4 (C4, C3, C2, C1, C0): internal RC mode calibration bits.

Calibration Selection for Internal RC Mode

C4	C3	C2	C1	C0	*Cycle Time (ns)	*Frequency (MHz)
1	1	1	1	1	399	2.506
1	1	1	1	0	385	2.6
1	1	1	0	1	371	2.693
1	1	1	0	0	358	2.786
1	1	0	1	1	347	2.879
1	1	0	1	0	336	2.973
1	1	0	0	1	326	3.066
1	1	0	0	0	316	3.159
0	1	1	1	1	307	3.253
0	1	1	1	0	298	3.346
0	1	1	0	1	290	3.439
0	1	1	0	0	283	3.533
0	1	0	1	1	275	3.626
0	1	0	1	0	268	3.719
0	1	0	0	1	262	3.813
0	1	0	0	0	256	3.906
0	0	0	0	0	250	4.00
0	0	0	0	1	244	4.093
0	0	0	1	0	238	4.186
0	0	0	1	1	233	4.279
0	0	1	0	0	228	4.373
0	0	1	0	1	223	4.466
0	0	1	1	0	219	4.559
0	0	1	1	1	214	4.653
1	0	0	0	0	210	4.746
1	0	0	0	1	206	4.839
1	0	0	1	0	202	4.933
1	0	0	1	1	198	5.026
1	0	1	0	0	195	5.119
1	0	1	0	1	191	5.213
1	0	1	1	0	188	5.306
1	0	1	1	1	185	5.4

Note: 1. Theoretical values, an instance of the high frequency mode, are shown for reference only. It depends on the process.

2. Similar way of calculation is also applicable for low frequency mode.

Bit 3 and Bit 2 (RCM1, RCM0): RC mode selection bits

RCM 1	RCM 0	*Frequency(MHz)
0	0	4
0	1	16
1	0	3.58
1	1	455kHz

Bits 1~0 (LVR1 ~ LVR0): Low Voltage Reset Enable bits

LVR1	LVR0	Reset Level	Release Level
0	0	NA	NA
0	1	2.6V	2.8V
1	0	3.3V	3.45V
1	1	3.8V	3.9V

LVR1, LVR0="0, 0" : LVR disable, power- on reset point of EM78F651N is 2.0V.

LVR1, LVR0="0, 1" : If Vdd < 2.6V, the EM78F651N will be reset.

LVR1, LVR0="1, 0" : If Vdd < 3.3V, the EM78F651N will be reset.

LVR1, LVR0="1, 1" : If Vdd < 3.8V, the EM78F651N will be reset.

6.10.2 Customer ID Register (Word 2)

Bit 12~Bit 0
XXXXXXXXXXXXX

Bits 12~0: Customer's ID code

6.11 Power-on Considerations

Any microcontroller is not guaranteed to start to operate properly before the power supply stays has stabilized. The EM78F651N has an on-chip Power-on Voltage Detector (POVD) with a detecting level of 2.0V. It will work well if Vdd can rise quick enough (50 ms or less). In many critical applications, however, extra devices are still required to assist in solving power-up problems.

6.12 External Power-on Reset Circuit

The circuit shown in Fig 6-15 implements an external RC to produce a reset pulse. The pulse width (time constant) should be kept long enough for Vdd to reached minimum operation voltage. This circuit is used when the power supply has slow rise time. Because the current leakage from the /RESET pin is ±5μA, it is recommended that R should not be greater than 40 K. In this way, the /RESET pin voltage is held below 0.2V. The diode (D) acts as a short circuit at the moment of power down.

The capacitor C will discharge rapidly and fully. Rin, the current-limited resistor, will prevent high current or ESD (electrostatic discharge) from flowing to pin /RESET.

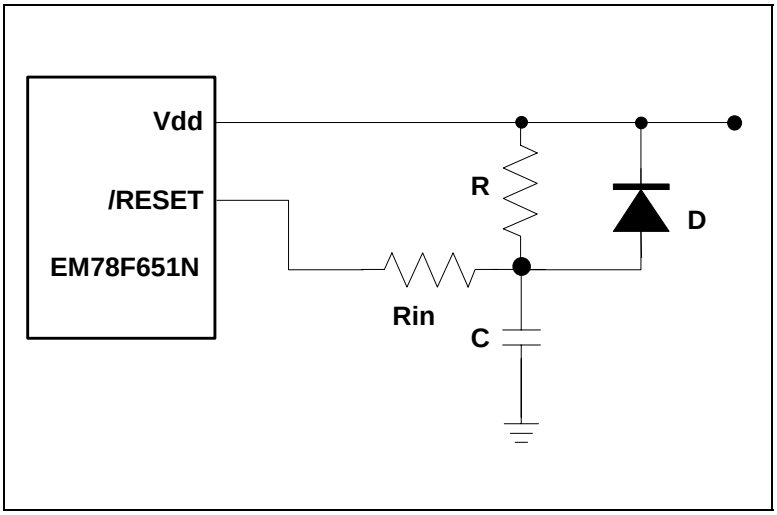


Fig. 6-15 External Power-Up Reset Circuit

6.13 Residue-Voltage Protection

When battery is replaced, device power (Vdd) is taken off but residue-voltage remains. The residue-voltage may trip below Vdd minimum, but not to zero. This condition may cause a poor power-on reset. Fig 6-16 and Fig 6-17 shows how to build a residue-voltage protection circuit.

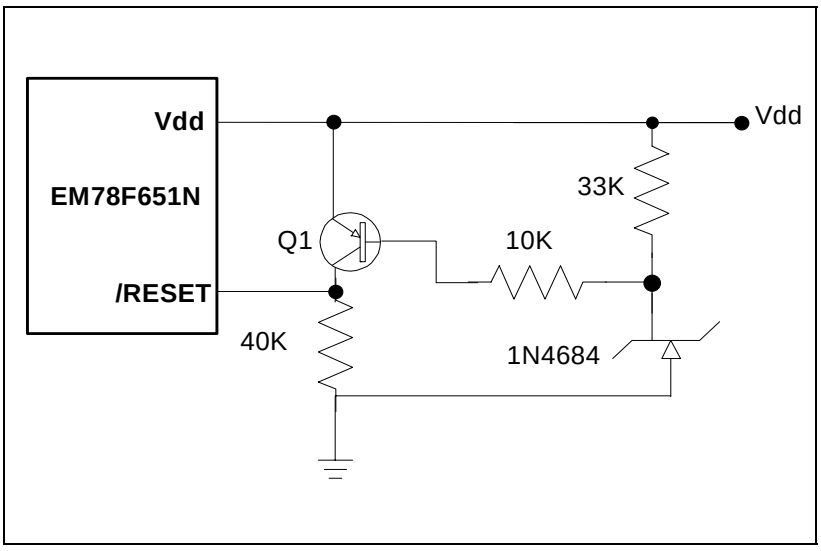


Fig. 6-16 Circuit 1 for the Residue Voltage Protection

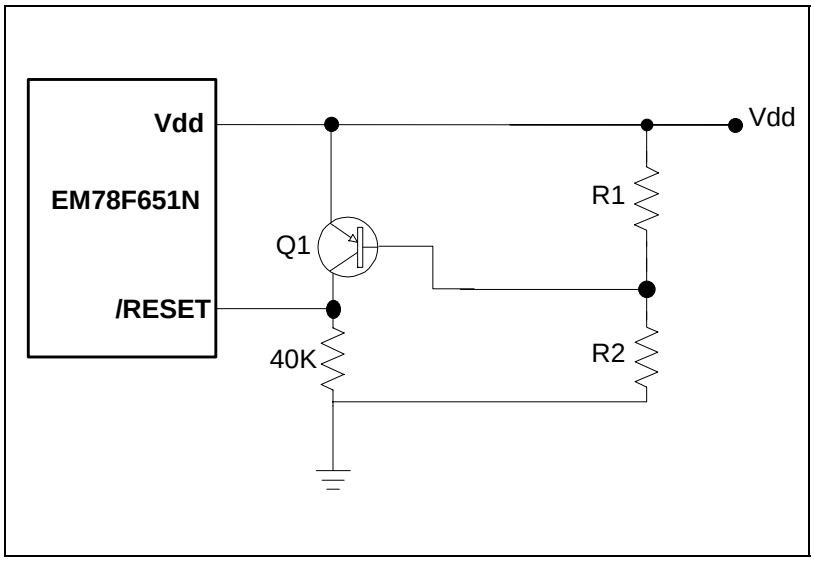


Fig. 6-17 Circuit 2 for the Residue Voltage Protection

6.14 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of two oscillator periods), unless the program counter is changed by instruction "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g. "SUB R2,A", "BS(C) R2,6", "CLR R2", etc.). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows:

(A) Change one instruction cycle to consist of four oscillator periods.

(B) "JMP", "CALL", "RET", "RETL", "RETI", or the conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") commands which were tested to be true, are executed within two instruction cycles. The instructions that are written to the program counter also take two instruction cycles.

Case (A) is selected by the Code Option bit, called CLK. One instruction cycle consists of two oscillator clocks if CLK is low, and four oscillator clocks if CLK is high.

Note that once the four oscillator periods within one instruction cycle is selected as in Case (A), the internal clock source to TCC should be CLK=Fosc/4, instead of Fosc / 2 as indicated in Fig 6-3.

In addition, the instruction set has the following features:

(1) Every bit of any register can be set, cleared, or tested directly.

(2) The I/O register can be regarded as general register. That is, the same instruction can operate on the I/O register.

Convention:

R = Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.

b = Bit field designator that selects the value for the bit located in the register R and which affects the operation.

k = 8 or 10-bit constant or literal value

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P
0 0000 0000 0100	0004	WDTC	0 → WDT	T, P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None [1]
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None [1]
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z, C, DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z, C, DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ R → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ R → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z, C, DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z, C, DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None [2]
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None [3]
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP], (Page, k) → PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z, C, DC
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z, C, DC
1 1110 1001 000k	1E9k	BANK k	K->R3(6)	None

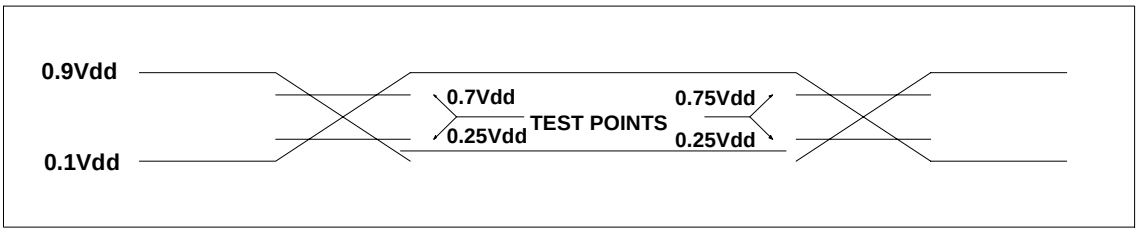
Note: [1] This instruction is applicable to IOC5~IOC6, IOCB ~ IOCF only.

[2] This instruction is not recommended for RF operation.

[3] This instruction cannot operate under RF.

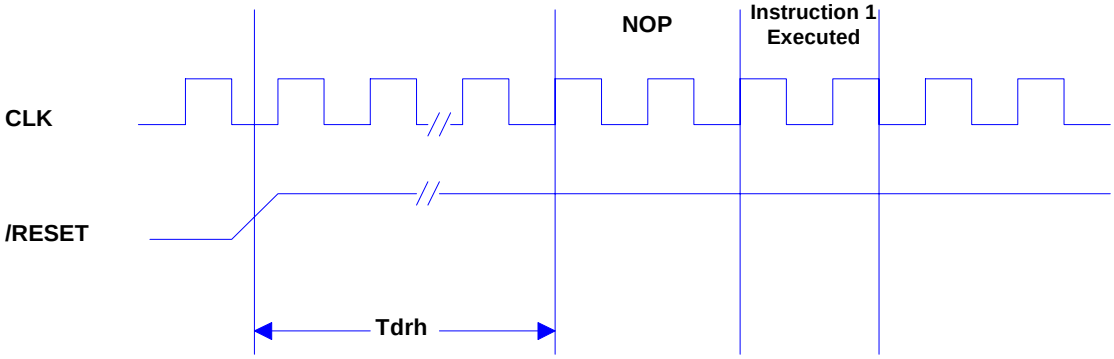
7 Timing Diagrams

AC Test Input/Output Waveform

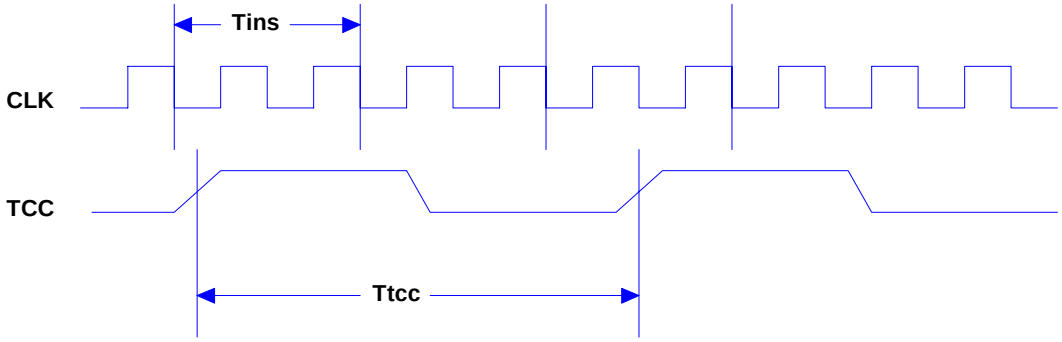


AC Testing : Input is driven at 0.9Vdd for logic "1",and 0.1Vdd for logic "0".Timing measurements are made at 0.75Vdd for logic "1",and 0.25Vdd for logic "0".

RESET Timing (CLK="0")



TCC Input Timing (CLKS="0")



8 Absolute Maximum Ratings

- **EM78F651N**

Items	Rating
Temperature under bias	0°C to 70°C
Storage temperature	-65°C to 150°C
Working voltage	2.2 to 5.5V
Working frequency	DC to 20MHz*
Input voltage	Vss-0.3V to Vdd+0.5V
Output voltage	Vss-0.3V to Vdd+0.5V

Note: These parameters are theoretical values and have not been tested.

9 DC Electrical Characteristic

Ta=25 °C, VDD=5.0V±5%, VSS=0V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Fxt	Crystal: VDD to 3V	Two cycles with two clocks	DC	10	14	MHz
	Crystal: VDD to 5V		DC	20	24	MHz
	ERC: VDD to 5V	R: 5.1KΩ, C: 100 pF	F±30%	830	F±30%	kHz
	IRC: VDD to 5 V	4MHz, 1MHz, 455kHz, 8MHz	F±30%	F	F±30%	Hz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	–	–	±1	μA
IRC1	IRC: VDD to 5V	RCM0:RCM1=0:0	2.9	4	5.7	MHz
IRCE	Internal RC oscillator error per stage		±4.3	±4.5	±4.7	%
IRC2	IRC: VDD to 5V	RCM0:RCM1=1:0	11.6	16	22	MHz
IRC3	IRC: VDD to 5V	RCM0:RCM1=0:1	2.5	3.58	5.15	MHz
IRC4	IRC: VDD to 5V	RCM0:RCM1=1:1	330	455	645	kHz
VIHRC	Input High Threshold Voltage (Schmitt Trigger)	OSCI in RC mode	3.9	4	4.1	V
IERC1	Sink current	VI from low to high, VI=5V	21	22	23	mA
VILRC	Input Low Threshold Voltage (Schmitt Trigger)	OSCI in RC mode	1.7	1.8	1.9	V
IERC2	Sink current	VI from high to low, VI=2V	16	17	18	mA
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-1	0	1	μA
VIH1	Input High Voltage (Schmitt Trigger)	Ports 5, 6, 7	0.75Vdd	–	Vdd+0.3V	V
VIL1	Input Low Voltage (Schmitt Trigger)	Ports 5, 6, 7	-0.3V	–	0.25Vdd	V
VIHT1	Input High Threshold Voltage (Schmitt Trigger)	/RESET	0.75Vdd	–	Vdd+0.3V	V
VILT1	Input Low Threshold Voltage (Schmitt Trigger)	/RESET	-0.3V	–	0.25Vdd	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIHT2	Input High Threshold Voltage (Schmitt Trigger)	TCC, INT	0.75Vdd	–	Vdd+0.3V	V
VILT2	Input Low Threshold Voltage Schmitt Trigger)	TCC, INT	-0.3V	–	0.25Vdd	V
VIHX1	Clock Input High Voltage	OSCI in crystal mode	2.9	3.0	3.1	V
VILX1	Clock Input Low Voltage	OSCI in crystal mode	1.7	1.8	1.9	V
IOH1	Output High Voltage (Ports 5, 6)	VOH = VDD-0.5V	–	-3.5	–	mA
IOL1	Output Low Voltage (Ports 5, 7)	VOL = GND+0.5V	–	10	–	mA
IOL2	Output Low Voltage (Ports 6)	VOL = GND+0.5V	–	18	–	mA
IPH	Pull-high current	Pull-high active, input pin at VSS	-45	-65	-85	μA
IPL	Pull-low current	Pull-low active, Input pin at Vdd	5	25	40	μA
ISB1	Power down current	All input and I/O pins at VDD, Output pin floating, WDT disabled	–	1.0	2.0	μA
ISB2	Power down current	All input and I/O pins at VDD, Output pin floating, WDT enabled	–	850	1000	μA
ICC1	Operating supply current at two clocks	/RESET= 'High', Fosc=32kHz (Crystal type, CLKS="0"), Output pin floating, WDT disabled	12	15	20	μA
ICC2	Operating supply current at two clocks	/RESET= 'High', Fosc=32kHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled	–	300	350	μA
ICC3	Operating supply current at two clocks	/RESET= 'High', Fosc=4MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled	–	1.3	1.6	mA
ICC4	Operating supply current at two clocks	/RESET= 'High', Fosc=10MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled	–	2.7	3.0	mA

Note: These parameters are theoretical values and have not been tested.

* Data in the Minimum, Typical, Maximum (“Min”, “Typ”, ”Max”) columns are based on characterization results at 25°C. This data is for design guidance only and is not tested.

LVD (Low Voltage Detector) Electrical Characteristics

Symbol	Parameter	Condition	Min.*	Typ.	Max.**	Unit
LVD1	LVD1 Voltage interrupt level(Schmitt trigger)	Vdd=5V	2.1±0.1		2.2±0.1	V
LVD2	LVD2 Voltage interrupt level(Schmitt trigger)	Vdd=5V	3.1±0.1		3.3±0.1	V
LVD3	LVD3 Voltage interrupt level(Schmitt trigger)	Vdd=5V	3.8±0.1		3.9±0.1	V
LVD4	LVD4 Voltage interrupt level(Schmitt trigger)	Vdd=5V	4.3±0.1		4.4±0.1	V

Note: *VDD Voltage from High to Low.
** VDD Voltage from Low to High.

LVR (Low Voltage Reset) Electrical Characteristics

Symbol	Parameter	Condition	Min.*	Typ.	Max.**	Unit
LVR1	LVR1 Voltage reset level (Schmitt trigger)	Vdd=5V	–	–	–	V
LVR2	LVR2 Voltage reset level (Schmitt trigger)	Vdd=5V	2.6±0.15	–	2.8±0.15	V
LVR3	LVR3 Voltage reset level (Schmitt trigger)	Vdd=5V	3.3±0.15	–	3.45±0.15	V
LVR4	LVR4 Voltage reset level (Schmitt trigger)	Vdd=5V	3.8±0.15	–	3.9±0.15	V

Note: *VDD Voltage from High to Low.
** VDD Voltage from Low to High.

Data EEPROM Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tprog	Erase/Write cycle time	Vdd = 2.0~ 5.5V Temperature = -40°C ~ 85°C	–	6	–	ms
Treten	Data Retention		–	10	–	Years
Tendu	Endurance time		–	100K	–	Cycles

Program Flash memory Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tprog	Erase/Write cycle time	Vdd = 5.0V Temperature = -40°C ~ 85°C	–	4	–	ms
Treten	Data Retention		–	10	–	Years
Tendu	Endurance time		–	100K	–	Cycles

10 AC Electrical Characteristic

EM78F651N, 0 ≤ Ta ≤ 70°C, VDD=5V, VSS=0V

-40 ≤ Ta ≤ 85°C, VDD=5V, VSS=0V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type	100	–	DC	ns
		RC type	500	–	DC	ns
Ttcc	TCC input period	–	(Tins+20)/N*	–	–	ns
Tdrh	Device reset hold time	–	11.8	16.8	21.8	ms
Trst	/RESET pulse width	Ta = 25°C	2000	–	–	ns
Twdt	Watchdog timer period	Ta = 25°C	11.8	16.8	21.8	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	–	20	–	ns
Tdelay	Output pin delay time	Cload=20pF	–	50	–	ns

Note: These parameters are theoretical values and have not been tested.

* Data in the Minimum, Typical, Maximum (“Min”, “Typ”, ”Max”) columns are based on characterization results at 25°C. This data is for design guidance only and is not tested.

* N = selected prescaler ratio

APPENDIX

A Package Type

Flash MCU	Package Type	Pin Count	Package Size
EM78F651NAP	DIP	14	300 mil
EM78F651NAPS/NAPJ	DIP	14	300 mil
EM78F651NAM	SOP	14	150 mil
EM78F651NAMS/NAMJ	SOP	14	150 mil
EM78F651NBP	DIP	16	300 mil
EM78F651NBPS/NBPJ	DIP	16	300 mil
EM78F651NBM	SOP	16	300 mil
EM78F651NBMS/NBMJ	SOP	16	300 mil
EM78F651NCP	DIP	18	300 mil
EM78F651NCPS/NCPJ	DIP	18	300 mil
EM78F651NCM	SOP	18	300 mil
EM78F651NCMS/NCMJ	SOP	18	300 mil
EM78F651NDKM	SSOP	20	209 mil
EM78F651NDKMS/NDKMJ	SSOP	20	209 mil
EM78F651NDP	DIP	20	300mil
EM78F651NDPS/NDPJ	DIP	20	300mil

Green products do not contain hazardous substances.

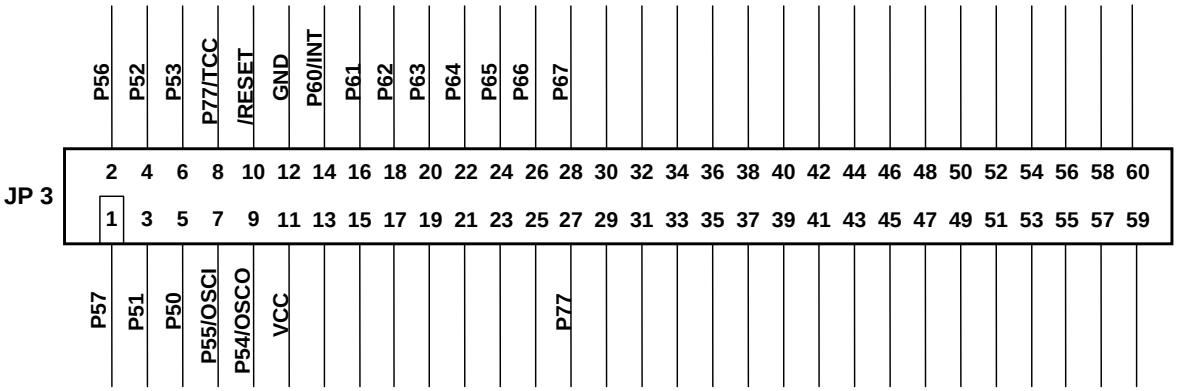
The third edition of Sony SS-00259 standard.

Pb contents should be less the 100ppm

Pb contents comply with Sony specs.

Electroplate type	Pure Tin
Ingredient (%)	Sn:100%
Melting point (°C)	232°C
Electrical resistivity (μΩ cm)	11.4
Hardness (hv)	8~10
Elongation (%)	>50%

B ICE 652N Output Pin Assignment (JP 3)



C EM78F651N Program Pin:

In the following IC diagram, “Pin # number” means the Pin to be connected to the Socket in DWTR.