

FAIRCHILD
SEMICONDUCTOR™

April 1988
Revised September 2000

74F161A • 74F163A

Synchronous Presettable Binary Counter

General Description

The 74F161A and 74F163A are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multi-stage counters. The 74F161A has an asynchronous Master-Reset input that overrides all other inputs and forces the outputs LOW. The 74F163A has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock. The 74F161A and 74F163A are high-speed versions of the 74F161 and 74F163.

Features

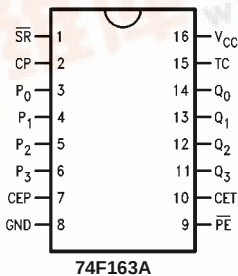
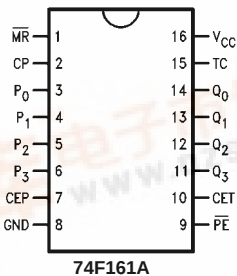
- Synchronous counting and loading
- High-speed synchronous expansion
- Typical count frequency of 120 MHz

Ordering Code:

Order Number	Package Number	Package Description
74F161ASC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74F161ASJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F161APC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
74F163ASC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74F163ASJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F163APC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

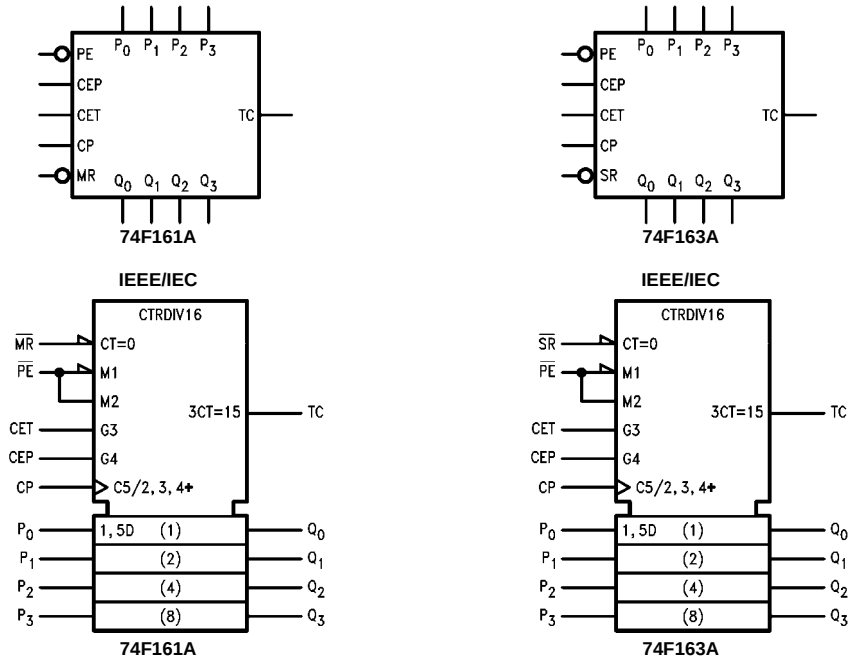


74F161A • 74F163A Synchronous Presettable Binary Counter



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Logic Symbols



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
CEP	Count Enable Parallel Input	1.0/1.0	20 μ A/-0.6 mA
CET	Count Enable Trickle Input	1.0/2.0	20 μ A/-1.2 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μ A/-0.6 mA
$\overline{MR}$ (74F161A)	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	20 μ A/-0.6 mA
$\overline{SR}$ (74F163A)	Synchronous Reset Input (Active LOW)	1.0/2.0	20 μ A/-1.2 mA
P ₀ -P ₃	Parallel Data Inputs	1.0/1.0	20 μ A/-0.6 mA
$\overline{PE}$	Parallel Enable Input (Active LOW)	1.0/2.0	20 μ A/-1.2 mA
Q ₀ -Q ₃	Flip-Flop Outputs	50/33.3	-1 mA/20 mA
TC	Terminal Count Output	50/33.3	-1 mA/20 mA

Functional Description

The 74F161A and 74F163A count in modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the 74F161A) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset (74F161A), synchronous reset (74F163A), parallel load, count-up and hold. Five control inputs—Master Reset (MR, 74F161A), Synchronous Reset (SR, 74F163A), Parallel Enable (PE), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on MR overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on SR overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on PE overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next

rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ (74F161A) or $\overline{SR}$ (74F163A) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The 74F161A and 74F163A use D-type edge triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and the counter is in state 15. To implement synchronous multi-stage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. Please refer to the 74F568 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers.

Logic Equations: Count Enable = CEP • CET • $\overline{PE}$

$$TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot CET$$

Mode Select Table

$\overline{SR}$ (Note 1)	$\overline{PE}$	CET	CE P	Action on the Rising Clock Edge (↗)
L	X	X	X	Reset (Clear)
H	L	X	X	Load (P _n →Q _n)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

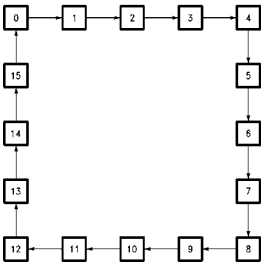
H = HIGH Voltage Level

L = LOW Voltage Level

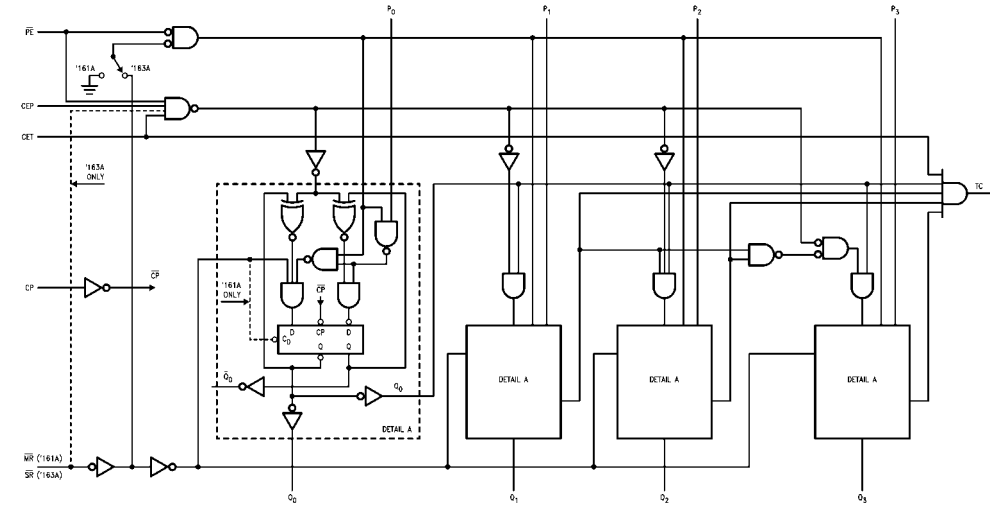
X = Immaterial

Note 1: For 74F163A only

State Diagram



Block Diagram



74F161A • 74F163A

Absolute Maximum Ratings^(Note 2)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V _{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 3)	−0.5V to +7.0V
Input Current (Note 3)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	−0.5V to V _{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

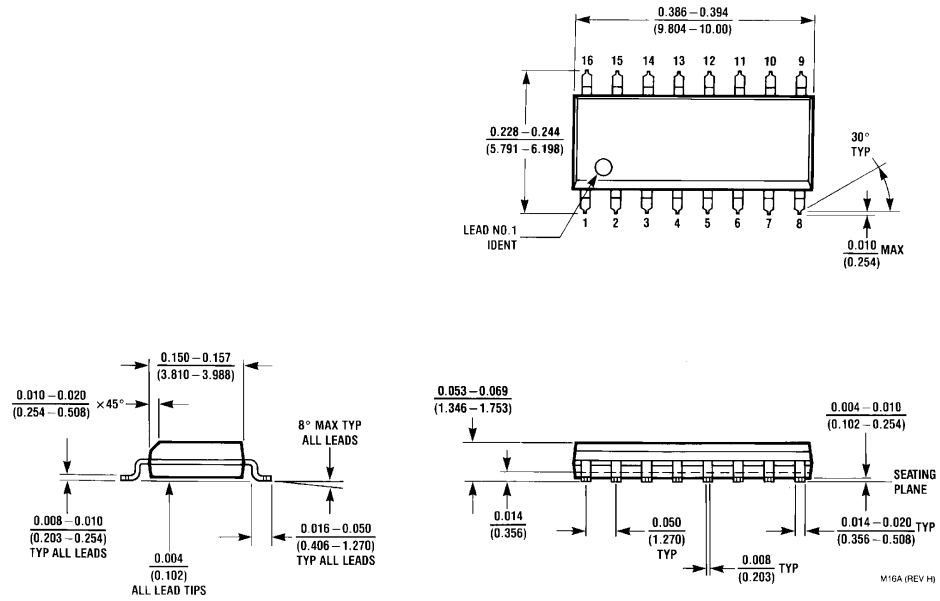
DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I _{IN} = −18 mA
V _{OH}	Output HIGH Voltage	10% V _{CC} 5% V _{CC}	2.5 2.7		V	Min	
V _{OL}	Output LOW Voltage	10% V _{CC}		0.5	V	Min	I _{OL} = 20 mA
I _{IH}	Input HIGH Current			5.0	μA	Max	V _{IN} = 2.7V
I _{bvi}	Input HIGH Current Breakdown Test			7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current			3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			−0.6 −1.2	mA mA	Max Max	V _{IN} = 0.5V (CEP, CP, $\overline{MR}$, P ₀ –P ₃) V _{IN} = 0.5V (CET, PE, SR)
I _{OS}	Output Short-Circuit Current	−60		−150	mA	Max	V _{OUT} = 0V
I _{CC}	Power Supply Current		37	55	mA	Max	

AC Electrical Characteristics							
Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A = -55°C to +125°C V _{CC} = +5.0V C _L = 50 pF		Units
		Min	Typ	Max	Min	Max	
t _{MAX}	Maximum Count Frequency	100	120		75	90	MHz
t _{PLH}	Propagation Delay CP to Q _n (PE Input HIGH)	3.5	5.5	7.5	3.5	9.0	ns
t _{PHL}	Propagation Delay CP to Q _n (PE Input LOW)	3.5	7.5	10.0	3.5	11.5	
t _{PLH}	Propagation Delay CP to Q _n (PE Input LOW)	4.0	6.0	8.5	4.0	10.0	ns
t _{PHL}	Propagation Delay CP to TC	4.0	6.0	8.5	4.0	10.0	
t _{PLH}	Propagation Delay CP to TC	5.0	10.0	14.0	5.0	16.5	ns
t _{PHL}	Propagation Delay CET to TC	5.0	10.0	14.0	5.0	15.5	
t _{PLH}	Propagation Delay CET to TC	2.5	4.5	7.5	2.5	9.0	ns
t _{PHL}	Propagation Delay MR to Q _n (74F161A)	2.5	4.5	7.5	2.5	9.0	
t _{PHL}	Propagation Delay MR to Q _n (74F161A)	5.5	9.0	12.0	5.5	14.0	ns
t _{PHL}	Propagation Delay MR to TC (74F161A)	4.5	8.0	10.5	4.5	12.5	ns
AC Operating Requirements							
Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V		T _A = -55°C to +125°C V _{CC} = +5.0V		T _A = 0°C to +70°C V _{CC} = +5.0V	Units
		Min	Max	Min	Max	Min	Max
t _S (H)	Setup Time, HIGH or LOW P _n to CP	5.0		5.5		5.0	ns
t _S (L)	Hold Time, HIGH or LOW P _n to CP	5.0		5.5		5.0	
t _H (H)	Setup Time, HIGH or LOW P _n to CP	2.0		2.5		2.0	ns
t _H (L)	Hold Time, HIGH or LOW PE or SR to CP	2.0		2.5		2.0	
t _S (H)	Setup Time, HIGH or LOW PE or SR to CP	11.0		13.5		11.5	ns
t _S (L)	Hold Time, HIGH or LOW PE or SR to CP	8.5		10.5		9.5	
t _H (H)	Setup Time, HIGH or LOW CEP or CET to CP	2.0		3.6		2.0	ns
t _H (L)	Hold Time, HIGH or LOW CEP or CET to CP	0		0		0	
t _S (H)	Setup Time, HIGH or LOW MR to CP (74F161A)	11.0		13.0		11.5	ns
t _S (L)	Hold Time, HIGH or LOW MR to CP (74F161A)	5.0		6.0		5.0	
t _H (H)	Clock Pulse Width (Load) HIGH or LOW	0		0		0	ns
t _H (L)	Clock Pulse Width (Count) HIGH or LOW	0		0		0	
t _W (H)	MR Pulse Width, LOW (74F161A)	5.0		5.0		5.0	ns
t _W (L)	Recovery Time MR to CP (74F161A)	5.0		5.0		5.0	ns
t _{REC}	Recovery Time MR to CP (74F161A)	6.0		6.0		6.0	ns

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Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A

M16A (REV H)

0.47 TYP

10.2±0.1
-A-

16

9

7.8

3.9

5.3±0.1
-B-

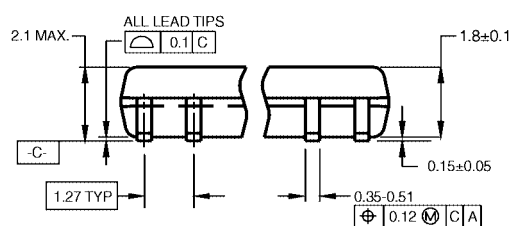
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PIN #1 IDENT.

0.2 C B A

ALL LEAD TIPS



SEE DETAIL A

0.15-0.25

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

Technical drawing of Detail A, showing a cross-section of a mechanical part. The drawing includes the following features and dimensions:

- 7° TYP**: Taper angle specification.
- 0°-8° TYP**: Taper angle specification.
- GAGE PLANE**: A horizontal plane used for measurement.
- SEATING PLANE**: A horizontal plane used for measurement.
- 0.60±0.15**: Dimension for the width of the base.
- 1.25**: Dimension for the length of the base.
- 0.25**: Dimension for the thickness of the base.

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