Positive J–$\overline{K}$ positive edge-triggered flip-flops 74F109

FEATURE

- Industrial temperature range available (–40°C to +85°C)

DESCRIPTION

The 74F109 is a dual positive edge–triggered JK–type flip–flop featuring individual J, $\overline{K}$, clock, set, and reset inputs; also true and complementary outputs. Set ($\overline{SD}$) and reset ($\overline{RD}$) are asynchronous active low inputs and operate independently of the clock (CP) input. The J and $\overline{K}$ are edge–triggered inputs which control the state changes of the flip–flops as described in the function table. Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive–going pulse. The J and $\overline{K}$ inputs must be stable just one setup time prior to the low–to–high transition of the clock for predictable operation. The J$\overline{K}$ design allows operation as a D flip–flop by tying J and $\overline{K}$ inputs together. Although the clock input is level sensitive, the positive transition of the clock pulse between the 0.8V and 2.0V levels should be equal to or less than the clock to output delay time for reliable operation.

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT(TOTAL)
74F109	125MHz	12.3mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C
16–pin plastic DIP	N74F109N	I74F109N
16–pin plastic SO	N74F109D	I74F109D

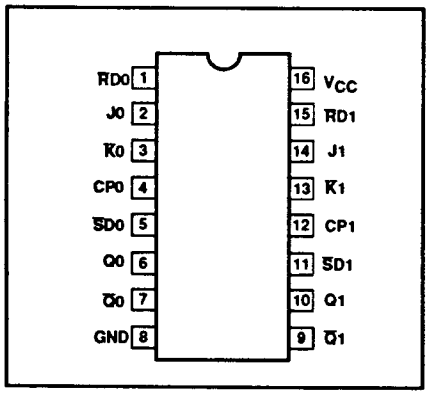
INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J0, J1	J inputs	1.0/1.0	20µA/0.6mA
$\overline{K}$0, $\overline{K}$1	K inputs	1.0/1.0	20µA/0.6mA
CP0, CP1	Clock inputs (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{SD}$0, $\overline{SD}$1	Set inputs (active low)	1.0/3.0	20µA/1.8mA
$\overline{RD}$0, $\overline{RD}$1	Reset inputs (active low)	1.0/3.0	20µA/1.8mA
Q0, Q1, $\overline{Q}$0, $\overline{Q}$1	Data outputs	50/33	1.0mA/20mA

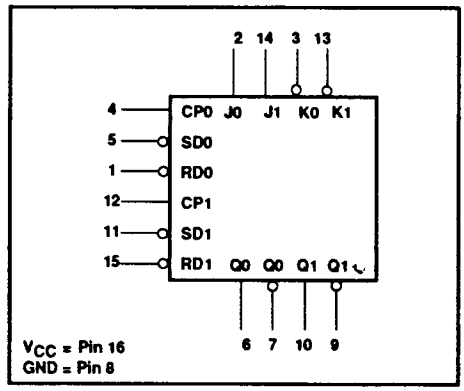
Note to input and output loading and fan out table

1. One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

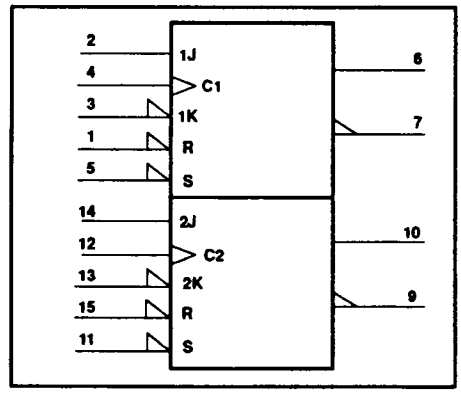
PIN CONFIGURATION



LOGIC SYMBOL



IEC/IEEE SYMBOL



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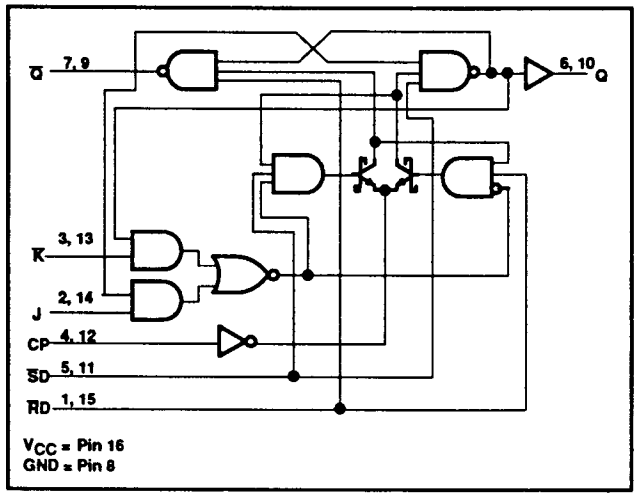
LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS		OPERATING MODE
$\overline{SD}$	$\overline{RD}$	CP	J	$\overline{K}$	Q	$\overline{Q}$	
L	H	X	X	X	H	L	Asynchronous set
H	L	X	X	X	L	H	Asynchronous reset
L	L	X	X	X	H	H	Undetermined*
H	H	↕	X	X	q	$\overline{q}$	Hold
H	H	↑	h	l	$\overline{q}$	q	Toggle
H	H	↑	h	h	H	L	Load "1" (set)
H	H	↑	l	l	L	H	Load "0" (reset)
H	H	↑	l	h	q	$\overline{q}$	Hold 'no change"

Notes to function table

1. H = High–voltage level
2. h = High–voltage level one setup time prior to low–to–high clock transition
3. L = Low–voltage level
4. l = Low–voltage level one setup time prior to low–to–high clock transition
5. q_t = Lower case indicate the state of the referenced ouput prior to the low–to–high clock transition
6. X = Don't care
7. ↑ = Low–to–high clock transition
8. ↕ = Not low–to–high clock transition
9. * = Both outputs will be high if both $\overline{SD}$ and $\overline{RD}$ go low simultaneously

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		40	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IN}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High–level output current				–1	mA
I_{OL}	Low–level output current				20	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High–level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OH} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN		±5%V_{CC}	2.7	3.4		V
V_{OL}	Low–level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN		±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current	J, $\overline{K}$, CPn	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
		$\overline{S}$Dn, $\overline{R}$Dn	V_{CC} = MAX, V_I = 0.5V					-1.8	mA
I_{OS}	Short–circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX				12.3	17	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs high in turn.

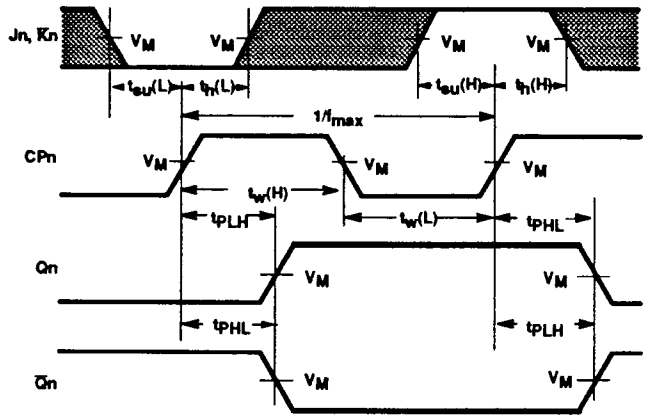
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	90	125		90		90		ns
t_{PLH} t_{PHL}	Propagation delay CPn to Qn or $\overline{Q}$n	Waveform 1	3.8 4.4	5.3 6.2	7.0 8.0	3.8 4.4	8.0 9.2	3.8 4.4	9.0 9.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}$Dn, $\overline{R}$Dn to Qn or $\overline{Q}$n	Waveform 2	3.2 3.5	5.2 7.0	7.0 9.0	3.2 3.5	8.0 10.5	2.8 3.5	9.0 10.5	ns

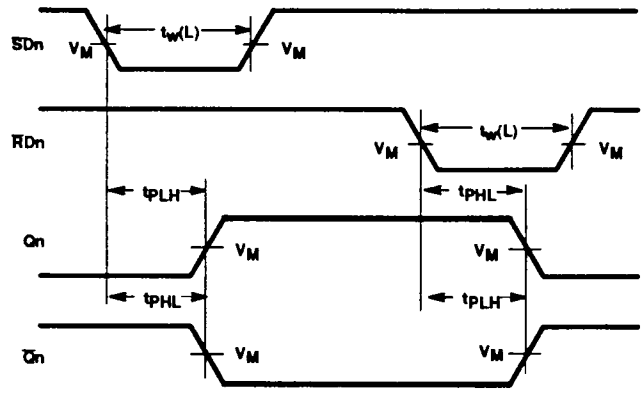
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low Dn to CPn	Waveform 1	3.0 3.0			3.0 3.0		3.0 3.0		ns
t_h (H) t_h (L)	Hold time, high or low Dn to CPn	Waveform 1	1.0 1.0			1.0 1.0		1.0 1.0		ns
t_w (H) t_w (L)	CP pulse width, high or low	Waveform 1	4.0 5.0			4.0 5.0		4.0 5.0		ns
t_w (L)	$\overline{S}$Dn or $\overline{R}$Dn pulse width, low	Waveform 2	4.0			4.0		4.0		ns
t_{rec}	Recovery time $\overline{S}$Dn or $\overline{R}$Dn to CP	Waveform 3	2.0			2.0		2.0		ns

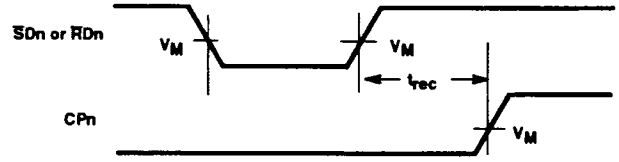
AC WAVEFORMS



Waveform 1. Propagation delay for data to output, data setup time and hold times, and clock width, and maximum clock frequency



Waveform 2. Propagation delay for set and reset to output, set and reset pulse width



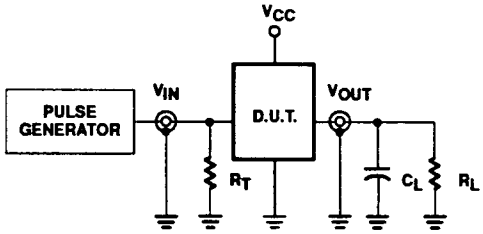
Waveform 3. Recovery time for set or reset to clock

Note to AC waveforms

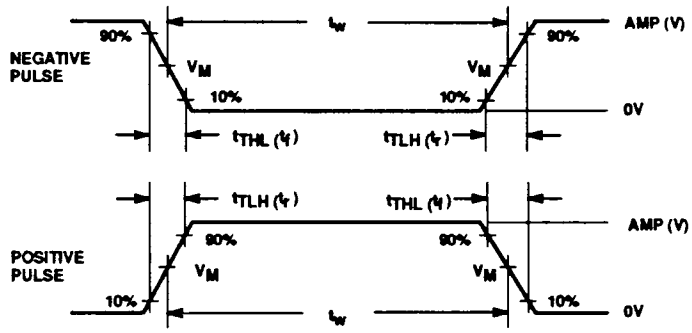
1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

Positive J–K positive edge-triggered flip-flops 74F109

TEST CIRCUIT AND WAVEFORMS



Test circuit for totem-pole outputs



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

VI. COMMERCIAL PRODUCT SPECIAL PROCESSING T-90-20

SUPR II LEVEL B

Signetics Upgraded Product Reliability (SUPR) program is designed to provide customers whose systems require an infant mortality level less than that of our non-burned-in products (which is typically below 1000 PPM).

DEVICE AVAILABILITY

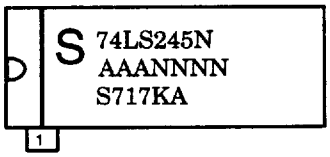
Products available for Level B processing are identified in the Price Book with a "B" suffix to the basic part number.

SUPR II LEVEL B PRICING ADDERS

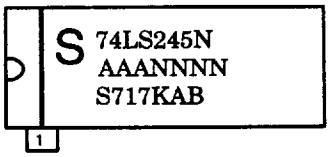
PRODUCT FAMILY	SUGGESTED RESALE ADDERS 1–99	100–999	OVER 1000
LIN	.14	.14	.11
LOG (TTL)			
(SSI)	.12	.10	.08
(MSI)	.16	.14	.11
(OCT)	.16	.14	.11
(CTM)	.16	.14	.11
LOG (ECL)			
(SSI)	.25	.23	.20
(MSI)	.25	.23	.20
LOG (LSI) (RAM) MIC (8X)	Consult Factory for Pricing		
PLD	Consult Factory for Pricing		
MCG	Consult Factory for Pricing		
DAT MIC	Not Available		

MARKING FORMAT EXAMPLES

Standard (no Burn-In) Products (Dual-in-line)



SUPR II (Burned-In) Products (Dual-in-line)



NOTE: The "B" in the 7th position on the 3rd line, when present, is the SUPR II Burn-In indicator.

TAPE AND REEL PACKAGING

SPECIFICATIONS

Tape and Reel specifications conform to Electronic Industries Association (EIA) Proposed Specification #EIA-481-A using 13 inch reels. Current incremental quantities reflect the quantities per reel. As more customers are able to handle a larger quantity per reel, this quantity will be increased.

DEVICE AVAILABILITY

Products available in tape and reel packaging are identified in the Price Book with a "T" suffix to the basic part number and are only offered as a product for sale by the reel. Return of product is limited to full reels with unbroken quality seals.

TAPE AND REEL PRICING ADDERS

PRODUCT FAMILY	SUGGESTED RESALE ADDER
MCG	.07
LIN	.07
LOG	.07
DAT MIC	PACKAGE A28 = .20 A44 = .25 A52 = .30 A68 = .40 A84 = .45 D24 = .17

VII. PACKING QUANTITY INFORMATION

T-90-20

CERAMIC DUAL IN-LINE (CERDIP)

PACKAGE CODE	PIN COUNT	QUANTITIES	
		DEVICES PER TUBE	DEVICES PER BOX
F/FE, BPA, PA	8-pin (300-mil)	48	1920
F, BCA, CA	14-pin (300-mil)	25	1000
F, BEA, EA	16-pin (300-mil)	25	1000
F, BVA, MVA	18-pin (300-mil)	21	840
F/FA, BRA, RA	20-pin (300-mil)	20	800
F, BWA, WA	22-pin (400-mil)	17	544
F/FA/F6, BJA, JA	24-pin (600-mil)	15	360
F/FA/F3/F24, BLA, LA	24-pin (300-mil)	15	600
F, BXA, XA	24-pin (400-mil)	15	480
F/FA/F28, BXA, XA	28-pin (600-mil)	13	312
FA	32-pin (600-mil)	11	264
F/FA/F40, BQA, MQA, QA	40-pin (600-mil)	9	216

CERPAC

PACKAGE CODE	PIN COUNT	QUANTITIES
		DEVICES PER TUBE
BDA/DA/W	14-pin	145
BFA/FA/W	16-pin	145
BXA/BYA/W	18-pin	100
BSA/SA/W/WB	20-pin	100
BKA/KA/W	24-pin	120
BYA/YA/W	28-pin	50

CERQUAD

PACKAGE CODE	PIN COUNT	QUANTITIES	
		DEVICES PER TRAY	DEVICES PER BOX
KA/K44	44-pin	6	6
KA/K68	68-pin	4	4
KA	84-pin	42	210

LEADLESS CHIP CARRIER

PACKAGE CODE	PIN COUNT	QUANTITIES
		DEVICES PER TUBE
B2A/2A/GA	20-pin	55
B3A/3A/GA/GC1	28-pin	43
YA/YA/GC2	32-pin	35
BUA/MXA/MUA/UA/XA/GA/GC	44-pin	27
BZA/BUA/UA/ZA/GA/GC	68-pin	19

QUANTITIES SHOWN IN GRAY REQUIRE PURCHASE TO BE MADE IN EXACT MULTIPLES OF THAT QUANTITY.

VII. PACKING QUANTITY INFORMATION

T-90-20

PLASTIC DUAL IN-LINE

PACKAGE CODE	PIN COUNT	QUANTITIES	
		DEVICES PER TUBE	DEVICES PER BOX
N/N8	8-pin (300-mil)	50	2000
N/N14/N16	14- 16-pin (300-mil)	25	1000
N	18-pin (300-mil)	20	800
N/N20	20-pin (300-mil)	18	720
N	22-pin (400-mil)	17	544
N/N6	24-pin (600-mil)	15	360
N/N3/N24	24-pin (300-mil)	15	600
N/N24	24-pin (400-mil)	15	480
N/N28	28-pin (600-mil)	13	312
N/N3	28-pin (300-mil)	13	520
N	32-pin (600-mil)	11	264
N/N40	40-pin (600-mil)	9	216
NB (Shrink)	42-pin (600-mil)	12	288
N/N48	48-pin (600-mil)	7	168
N	50-pin (900-mil)	7	112
N/N64	64-pin (900-mil)	5	80

PLASTIC LEADED CHIP CARRIER (PLCC)

PACKAGE CODE	PIN COUNT	QUANTITIES		
		DEVICES PER TUBE	DEVICES PER BOX	DEVICES PER REEL
A	20-pin	46	3680	1000
A/A28	28-pin	37	2368	750
A	32-pin	31	2232	750
A/A44	44-pin	26	1248	500
A/A52	52-pin	23	1012	500
A/A68	68-pin	18	648	250
A/A84	84-pin	15	420	250

QUANTITIES SHOWN IN GRAY REQUIRE PURCHASE TO BE MADE IN EXACT MULTIPLES OF THAT QUANTITY.

VII. PACKING QUANTITY INFORMATION

T-90-20

PLASTIC SMALL OUTLINE (SO)

PACKAGE CODE	PIN COUNT	QUANTITIES		
		DEVICES PER TUBE	DEVICES PER BOX	DEVICES PER REEL
D/D8	8-pin (150-mil)	100	10000	2500
D	8-pin (300-mil)	64	2560	1000 – 13" 700 – 7"
D/D14	14-pin (150-mil)	57	5700	2500
D	16-pin (150-mil)	50	5000	2500
D	16-pin (300-mil)	48	1920	1000
DK(SSOP)	20-pin (170-mil)	75	6750	2500
D	20-pin (300-mil)	38	1520	1000
D/D24	24-pin (300-mil)	32	1280	1000
D	28-pin (300-mil)	27	1080	1000
D	40-pin (VSO-40)	31	1240	1000 – 13" 300 – 7"
D	56-pin (VSO-56)	22	616	1000

QUAD FLAT PACK*

PACKAGE CODE	PIN COUNT	QUANTITIES	
		DEVICES PER TRAY	DEVICES PER BOX
B/B44	44-pin	50	500
B/B44	44-pin	96	480
B	52-pin	119	595
B	80-pin	66	330
B	100-pin	50	250
B	120-pin	24	120
B	120-pin (Philips source)	30	150

* Quad Flat Pack parts require dry pack handling according to EIA Standard - 583.
These parts are identified in part list section with DRY PACK in the Cross Ref Part No field.

QUANTITIES SHOWN IN GRAY REQUIRE PURCHASE TO BE MADE IN EXACT MULTIPLES OF THAT QUANTITY.