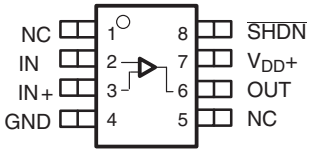
LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

Check for Samples: TLV2460-Q1, TLV2461-Q1, TLV2462-Q1, TLV2463-Q1, TLV2464-Q1, TLV2460A-Q1, TLV2461A-Q1, TLV2462A-Q1, TLV2463A-Q1, TLV2464A-Q1

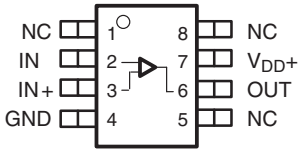
FEATURES

- Qualified for Automotive Applications
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Rail-to-Rail Output Swing
- Gain Bandwidth Product . . . 6.4 MHz
- ±80-mA Output Drive Capability
- Supply Current . . . 500 μA/Channel
- Input Offset Voltage . . . 100 μV
- Input Noise Voltage . . . 11 nV/√Hz
- Slew Rate . . . 1.6 V/μs
- Micropower Shutdown Mode (TLV2460/TLV2463) . . . 0.3 μA/Channel
- Universal Operational Amplifier EVM

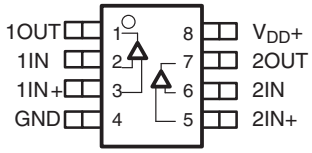
TLV2460
D OR PW PACKAGE
(TOP VIEW)



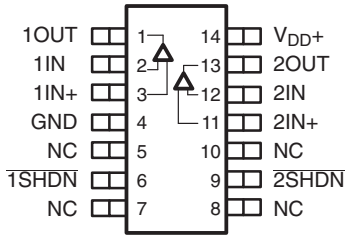
TLV2461
D OR PW PACKAGE
(TOP VIEW)



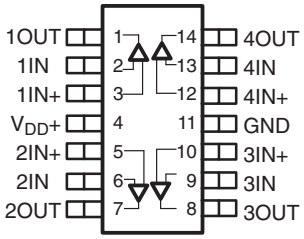
TLV2462
D, DGK, OR PW PACKAGE
(TOP VIEW)



TLV2463
D OR PW PACKAGE
(TOP VIEW)



TLV2464
D OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

DESCRIPTION

The devices in the TLV246x family of low-power rail-to-rail input/output operational amplifiers are specifically designed for portable applications. The input common-mode voltage range extends beyond the supply rails for maximum dynamic range in low-voltage systems. The amplifier output has rail-to-rail performance with high-output-drive capability, solving one of the limitations of older rail-to-rail input/output operational amplifiers. This rail-to-rail dynamic range and high output drive make the TLV246x ideal for buffering analog-to-digital converters.

The operational amplifier has 6.4-MHz bandwidth and 1.6-V/μs slew rate with only 500-μA supply current, providing good ac performance with low power consumption. Devices are available with an optional shutdown terminal, which places the amplifier in an ultralow supply-current mode (I_{DD} = 0.3 μA/channel). While in shutdown, the operational amplifier output is placed in a high-impedance state. DC applications are also well served with an input noise voltage of 11 nV/√Hz and input offset voltage of 100 μV.

ORDERING INFORMATION(1)

T_A	V_{IO}max AT 25°C	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	2000 μV	SOP – D	Reel of 2500	TLV2460QDRQ1	2460Q1
				TLV2461QDRQ1	2461Q1
				TLV2462QDRQ1	2462Q1
				TLV2463QDRQ1	2463Q1
				TLV2464QDRQ1(3)	2464Q1
		TSSOP – PW	Reel of 2000	TLV2460QPWRQ1	2460Q1
				TLV2461QPWRQ1	2461Q1
				TLV2462QPWRQ1	2462Q1
				TLV2463QPWRQ1	2463Q1
				TLV2464QPWRQ1(3)	2464Q1
		MSOP – DGK	Reel of 2500	TLV2462QDGKRQ1	QVM
	1500 μV	SOP – D	Reel of 2500	TLV2460AQDRQ1	2460AQ
				TLV2461AQDRQ1	2461AQ
				TLV2462AQDRQ1	2462AQ
				TLV2463AQDRQ1	TLV2463AQ1
				TLV2464AQDRQ1(3)	2464AQ
		TSSOP – PW	Reel of 2000	TLV2460AQPWRQ1	2460AQ
				TLV2461AQPWRQ1	2461AQ
				TLV2462AQPWRQ1	2462AQ
				TLV2463AQPWRQ1	2463AQ
				TLV2464AQPWRQ1	2464AQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) Product Preview

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

V_{DD}	Supply voltage(2)		6 V
V_{ID}	Differential input voltage range		–0.2 V to V_{DD} + 0.2 V
I_I	Input current (any input)		±200 mA
I_O	Output current		±175 mA
I_I	Total input current (into V_{DD+})		175 mA
I_O	Total output current (out of GND)		175 mA
T_A	Operating free-air temperature range		–40°C to 125°C
T_J	Maximum junction temperature		150°C
θ_{JA}	Thermal impedance, junction to ambient(3)	D (8 pin)	176°C/W
		D (14 pin)	123°C/W
		PW (8 pin)	259°C/W
		PW (14 pin)	174°C/W
		DGK (8 pin)	242°C/W
T_{stg}	Storage temperature range		–65°C to 150°C
	Latch-Up performance meets 100 mA per AEC-Q100 (Class I)		Class I
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to GND.
(3) Package thermal impedance is calculated in accordance with JESD 51-5.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{DD}	Supply voltage	Single supply	2.7	6	V
		Split supply	±1.35	±3	
V_{ICR}	Common-mode input voltage range		–0.2	V_{DD} + 0.2	V
T_A	Operating free-air temperature		–40	125	°C
	Shutdown on/off voltage level(1)	V_{IH}	2		V
		V_{IL}		0.7	

(1) Relative to voltage on the GND terminal of the device

ELECTRICAL CHARACTERISTICS

at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{DD} = 3 V, V_{IC} = 1.5 V, V_O = 1.5 V, R_S = 50 Ω	TLV246x	25°C		100	2000	μV
				Full range			2200	
			TLV246xA	25°C		150	1500	
				Full range			1700	
α_{VIO}	Temperature coefficient of input offset voltage	V_{DD} = 3 V, V_{IC} = 1.5 V, V_O = 1.5 V, R_S = 50 Ω				2		μV/°C
I_{IO}	Input offset current	V_{DD} = 3 V, V_{IC} = 1.5 V, V_O = 1.5 V, R_S = 50 Ω		25°C		2.8	7	pA
				Full range			75	
I_{IB}	Input bias current	V_{IC} = 1.5 V, V_O = 1.5 V, R_S = 50 Ω		25°C		4.4	14	pA
				Full range			75	
V_{OH}	High-level output voltage	I_O = –2.5 mA		25°C		2.9		V
				Full range	2.8			
		I_O = –10 mA		25°C		2.7		
				Full range	2.5			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V, I_{OL} = 2.5 mA		25°C		0.1		V
				Full range			0.2	
		V_{IC} = 1.5 V, I_{OL} = 10 mA		25°C		0.3		
				Full range			0.5	
I_{OS}	Short circuit output current	Sourcing		25°C		50		mA
				Full range	20			
		Sinking		25°C		40		
				Full range	20			
I_O	Output current	Measured 1 V from rail		25°C		±40		mA
A_{VD}	Large-signal differential voltage amplification	R_L = 10 kΩ		25°C	90	105		dB
				Full range	89			
$r_{i(d)}$	Differential input resistance			25°C		10^9		Ω
$c_{i(o)}$	Common-mode input capacitance	f = 10 kHz		25°C		7		pF
z_o	Closed-loop output impedance	f = 100 kHz, A_V = 10		25°C		33		Ω
CMRR	Common-mode rejection ratio	V_{ICR} = 0 V to 3 V, R_S = 50 Ω		25°C	66	80		dB
				Full range	60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 6 V, V_{IC} = V_{DD}/2, No load		25°C	80	85		dB
				Full range	75			
		V_{DD} = 3 V to 5 V, V_{IC} = V_{DD}/2, No load		25°C	85	95		
				Full range	80			
I_{DD}	Supply current (per channel)	V_O = 1.5 V, No load		25°C		0.5	0.575	μA
				Full range			0.9	
$I_{DD(SHDN)}$	Supply current in shutdown (TLV2460, TLV2463)	$\overline{SHDN}$ < 0.7 V, Per channel in shutdown		25°C		0.3		μA
				Full range			2.5	

(1) Full range is –40°C to 125°C.

OPERATING CHARACTERISTICS

V_{DD} = 3 V, at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_{O(PP)}$ = 2 V, C_L = 160 pF, R_L = 10 kΩ		25°C	1	1.6		V/μs
				Full range	0.8			
V_n	Equivalent input noise voltage	f = 100 Hz		25°C		16		nV/√Hz
		f = 1 kHz				11		
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.13		pA/√Hz
THD+N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ, f = 1 kHz	A_V = 1	25°C		0.006		%
			A_V = 10			0.02		
			A_V = 100			0.08		
$t_{(on)}$	Amplifier turn-on time	A_V = 1, R_L = 10 kΩ	Both channels	25°C		7.6		μs
			Channel 1 only, Channel 2 on			7.65		
$t_{(off)}$	Amplifier turn-off time	A_V = 1, R_L = 10 kΩ	Both channels	25°C		333		ns
			Channel 1 only, Channel 2 on			328		
			Channel 2 only, Channel 1 on			329		
	Gain-bandwidth product	f = 10 kHz, C_L = 160 pF, R_L = 10 kΩ		25°C		5.2		MHz
t_s	Settling time	$V_{(STEP)PP}$ = 2 V, A_V = –1, C_L = 10 pF, R_L = 10 kΩ	0.1%	25°C		1.47		μs
			0.01%			1.78		
		$V_{(STEP)PP}$ = 2 V, A_V = –1, C_L = 56 pF, R_L = 10 kΩ	0.1%			1.77		
			0.01%			1.98		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 160 pF		25°C		44		°
	Gain margin	R_L = 10 kΩ, C_L = 160 pF		25°C		7		dB

(1) Full range is –40°C to 125°C.

ELECTRICAL CHARACTERISTICS

at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{DD} = 5 V, V_{IC} = 2.5 V, V_O = 2.5 V, R_S = 50 Ω	TLV246x	25°C		150	2000	μV
				Full range			2200	
			TLV246xA	25°C		150	1500	
				Full range			1700	
α_{VIO}	Temperature coefficient of input offset voltage	V_{DD} = 5 V, V_{IC} = 2.5 V, V_O = 2.5 V, R_S = 50 Ω				2		μV/°C
I_{IO}	Input offset current	V_{DD} = 5 V, V_{IC} = 2.5 V, V_O = 2.5 V, R_S = 50 Ω		25°C		0.3	7	pA
				Full range			60	
I_{IB}	Input bias current	V_{DD} = 5 V, V_{IC} = 2.5 V, V_O = 2.5 V, R_S = 50 Ω		25°C		1.3	14	pA
				Full range			60	
V_{OH}	High-level output voltage	I_O = –2.5 mA		25°C		4.9		V
				Full range	4.8			
		I_O = –10 mA	TLV246x,TLV246xA	25°C		4.8		
				Full range	4.7			
			TLV2462QDGKRQ1	25°C		4.8		
				Full range	4.4			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 2.5 mA		25°C		0.1		V
				Full range			0.2	
		V_{IC} = 2.5 V, I_{OL} = 10 mA		25°C		0.2		
				Full range			0.3	
I_{OS}	Short circuit output current	Sourcing		25°C		145		mA
				Full range	60			
		Sinking		25°C		100		
				Full range	60			
I_O	Output current	Measured 1 V from rail		25°C		±80		mA
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, R_L = 10 kΩ, V_O = 1 V to 4 V		25°C	92	109		dB
				Full range	90			
$r_{i(d)}$	Differential input resistance			25°C		10^9		Ω
$c_{i(o)}$	Common-mode input capacitance	f = 10 kHz		25°C		7		pF
z_o	Closed-loop output impedance	f = 100 kHz, A_V = 10		25°C		29		Ω
CMRR	Common-mode rejection ratio	V_{ICR} = 0 V to 5 V, R_S = 50 Ω		25°C	71	85		dB
				Full range	60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 6 V, V_{IC} = V_{DD}/2, No load		25°C	80	85		dB
				Full range	75			
		V_{DD} = 3 V to 5 V, V_{IC} = V_{DD}/2, No load		25°C	85	95		
				Full range	80			
I_{DD}	Supply current (per channel)	V_O = 2.5 V, No load		25°C		0.55	0.65	μA
				Full range			1	
$I_{DD(SHDN)}$	Supply current in shutdown (TLV2460, TLV2463)	$\overline{SHDN}$ < 0.7 V, Per channel in shutdown		25°C		1		μA
				Full range			3	

(1) Full range is –40°C to 125°C.

OPERATING CHARACTERISTICS

V_{DD} = 5 V, at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_{O(PP)}$ = 2 V, C_L = 160 pF, R_L = 10 kΩ		25°C	1	1.6		V/μs
				Full range	0.8			
V_n	Equivalent input noise voltage	f = 100 Hz		25°C		14		nV/√Hz
		f = 1 kHz				11		
I_n	Equivalent input noise current	f = 100 Hz		25°C		0.13		pA/√Hz
THD+N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 4 V, R_L = 10 kΩ, f = 10 kHz	A_V = 1	25°C		0.004		%
			A_V = 10			0.01		
			A_V = 100			0.04		
$t_{(on)}$	Amplifier turn-on time	A_V = 1, R_L = 10 kΩ	Both channels	25°C		7.6		μs
			Channel 1 only, Channel 2 on			7.65		
			Channel 2 only, Channel 1 on			7.25		
$t_{(off)}$	Amplifier turn-off time	A_V = 1, R_L = 10 kΩ	Both channels	25°C		333		ns
			Channel 1 only, Channel 2 on			328		
			Channel 2 only, Channel 1 on			329		
	Gain-bandwidth product	f = 10 kHz, C_L = 160 pF, R_L = 10 kΩ		25°C		6.4		MHz
t_s	Settling time	$V_{(STEP)PP}$ = 2 V, A_V = –1, C_L = 10 pF, R_L = 10 kΩ	0.1%	25°C		1.53		μs
			0.01%			1.83		
		$V_{(STEP)PP}$ = 2 V, A_V = –1, C_L = 56 pF, R_L = 10 kΩ	0.1%			3.13		
			0.01%			3.33		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 160 pF		25°C		45		°
	Gain margin	R_L = 10 kΩ, C_L = 160 pF		25°C		7		dB

(1) Full range is –40°C to 125°C.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	vs Common-mode input voltage	1, 2
I_{IB}	Input bias current	vs Free-air temperature	3, 4
I_{IO}	Input offset current	vs Free-air temperature	3, 4
V_{OH}	High-level output voltage	vs High-level output current	5, 6
V_{OL}	Low-level output voltage	vs Low-level output current	7, 8
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	9, 10
	Open-loop gain	vs Frequency	11, 12
	Phase	vs Frequency	11, 12
A_{VD}	Differential voltage amplification	vs Load resistance	13
	Capacitive load	vs Load resistance	14
z_o	Output impedance	vs Frequency	15, 16
CMRR	Common-mode rejection ratio	vs Frequency	17
k_{SVR}	Supply-voltage rejection ratio	vs Frequency	18, 19
I_{DD}	Supply current	vs Supply voltage	20
		vs Free-air temperature	21
	Amplifier turnon characteristics		22
	Amplifier turnoff characteristics		23
	Supply current turnon		24
	Supply current turnoff		25
	Shutdown supply current	vs Free-air temperature	26
SR	Slew rate	vs Load capacitance	27
V_n	Equivalent input noise voltage	vs Frequency	28, 29
		vs Common-mode input voltage	30, 31
THD	Total harmonic distortion	vs Frequency	32, 33
THD + N	Total harmonic distortion plus noise	vs Peak-to-peak signal amplitude	34, 35
ϕ_m	Phase margin	vs Frequency	11, 12
		vs Load capacitance	36
		vs Free-air temperature	37
	Gain-bandwidth product	vs Supply voltage	38
		vs Free-air temperature	39
	Large signal follower		40, 41
	Small signal follower		42, 43
	Inverting large signal		44, 45
	Inverting small signal		46, 47

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

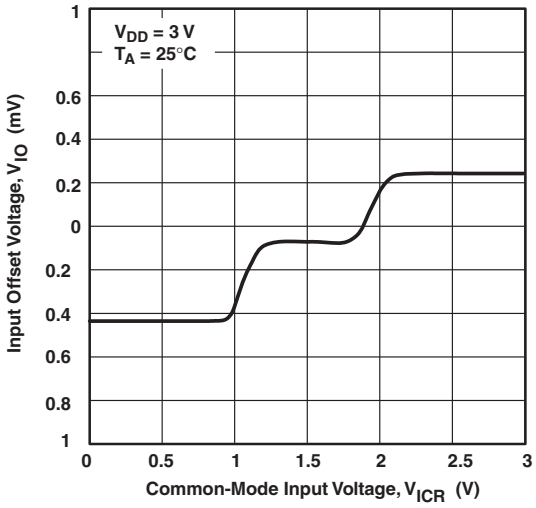


Figure 1.

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

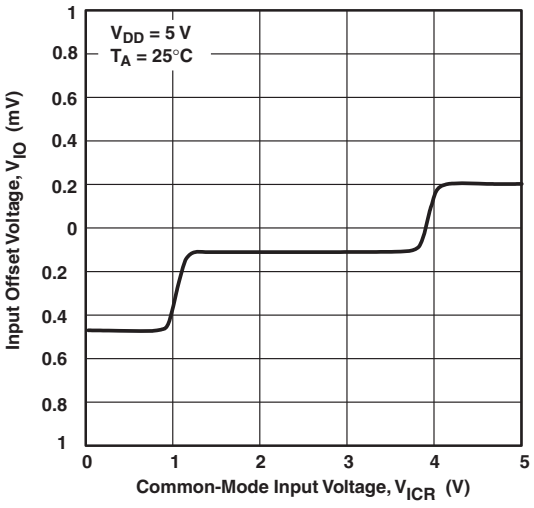


Figure 2.

INPUT BIAS AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

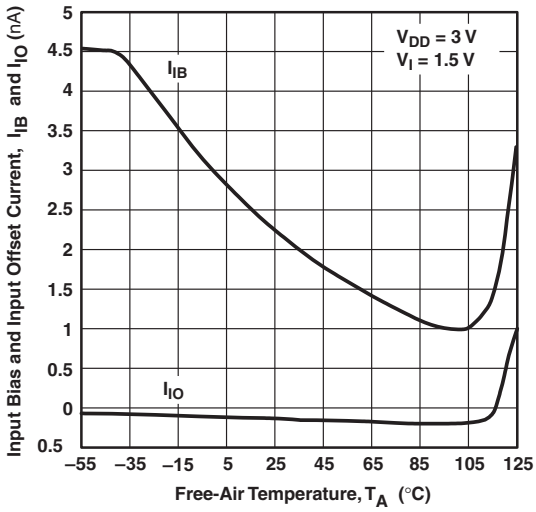


Figure 3.

INPUT BIAS AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

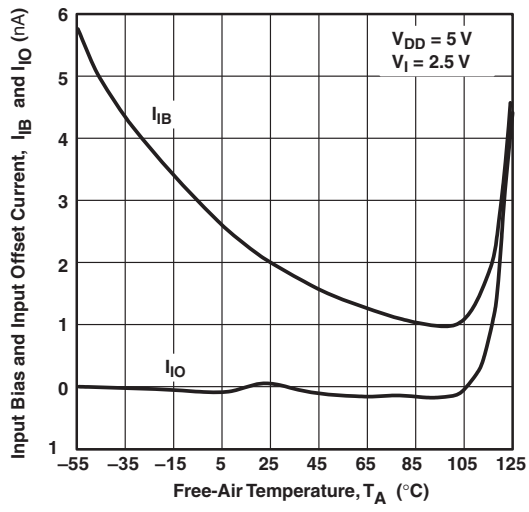


Figure 4.

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

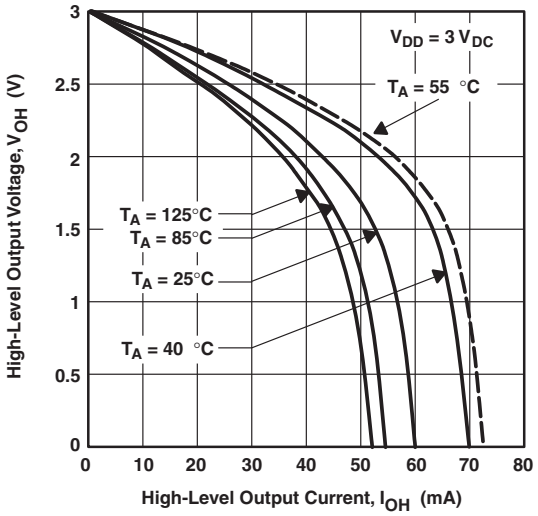


Figure 5.

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

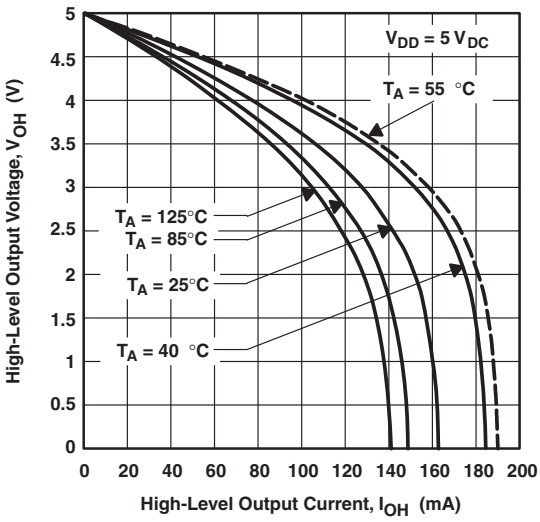


Figure 6.

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

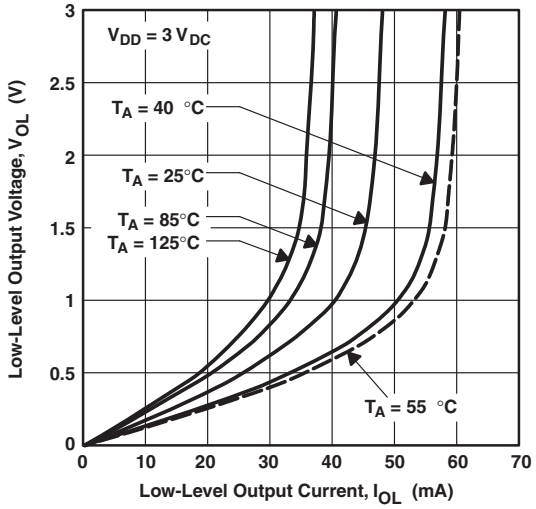


Figure 7.

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

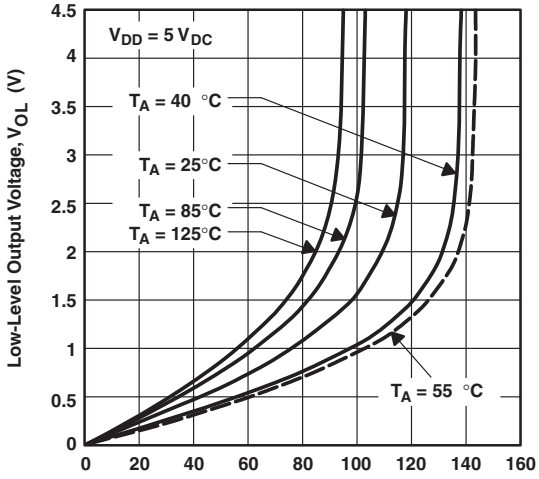


Figure 8.

PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

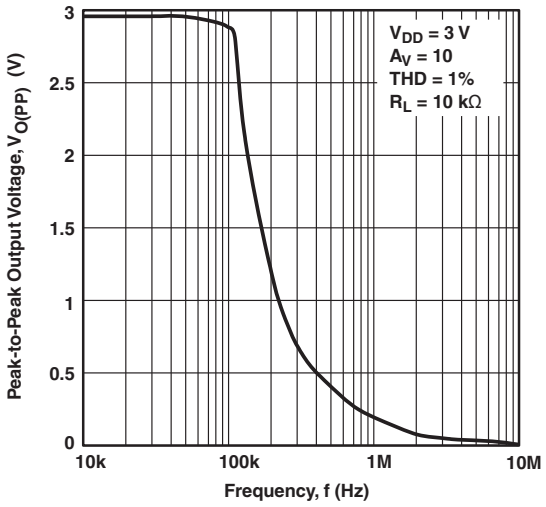


Figure 9.

PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

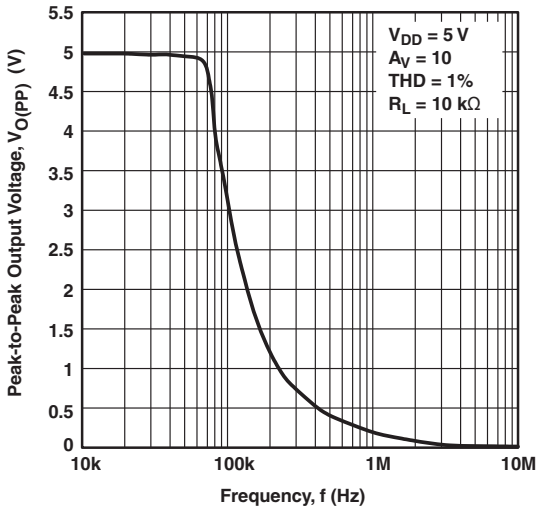


Figure 10.

OPEN-LOOP GAIN AND PHASE
vs
FREQUENCY

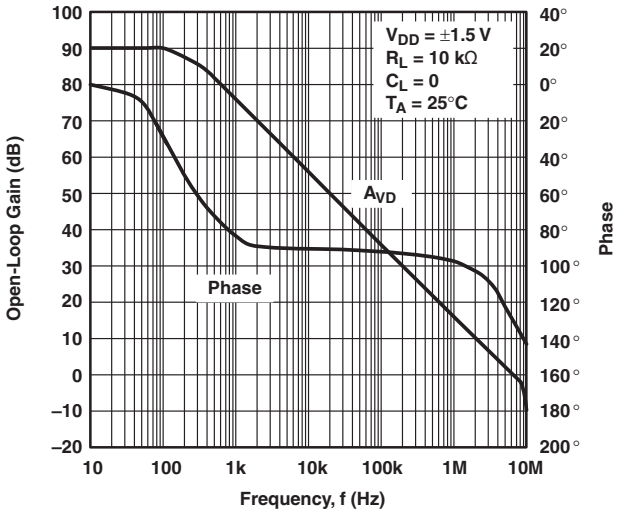


Figure 11.

OPEN-LOOP GAIN AND PHASE
vs
FREQUENCY

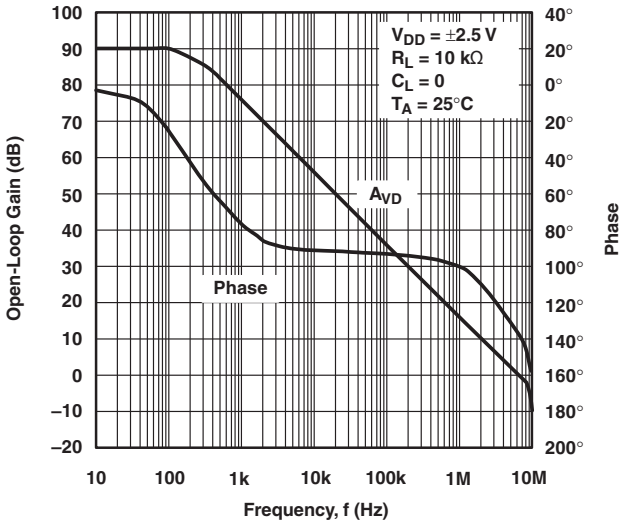


Figure 12.

DIFFERENTIAL VOLTAGE AMPLIFICATION vs LOAD RESISTANCE

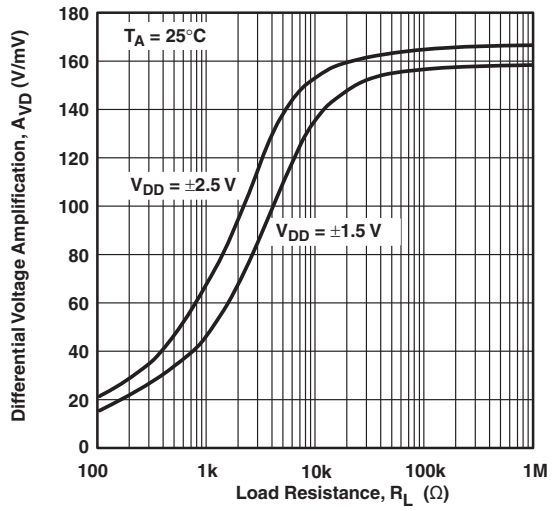


Figure 13.

CAPACITIVE LOAD vs LOAD RESISTANCE

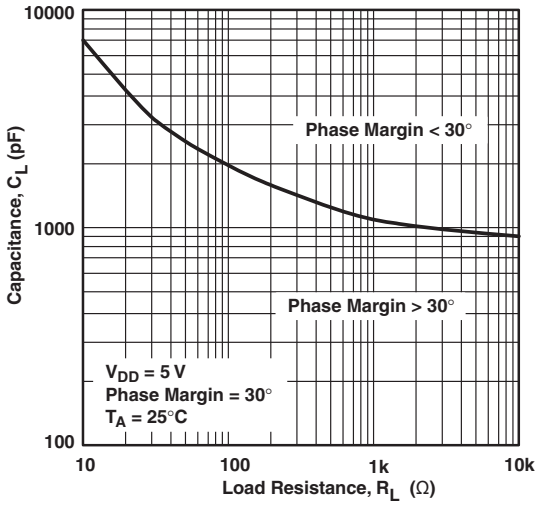


Figure 14.

OUTPUT IMPEDANCE vs FREQUENCY

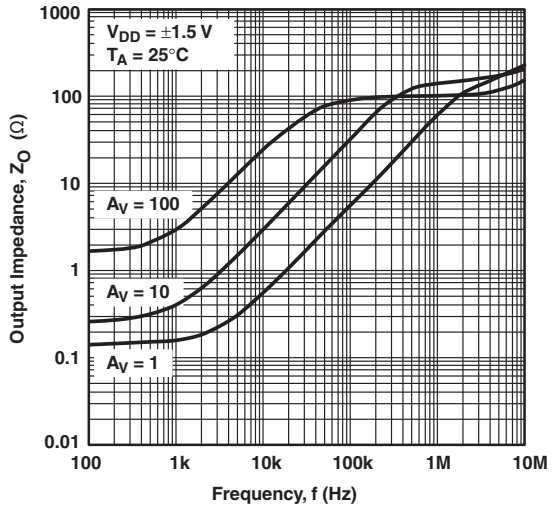


Figure 15.

OUTPUT IMPEDANCE vs FREQUENCY

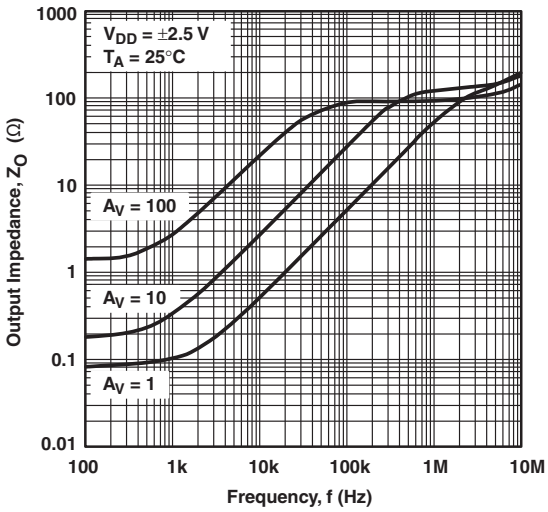


Figure 16.

COMMON-MODE REJECTION RATIO vs FREQUENCY

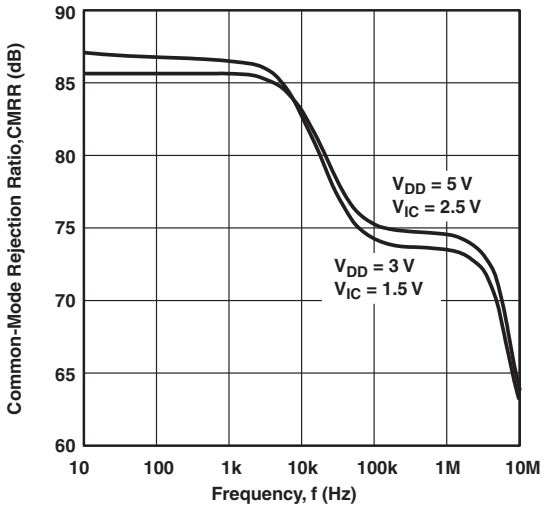


Figure 17.

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

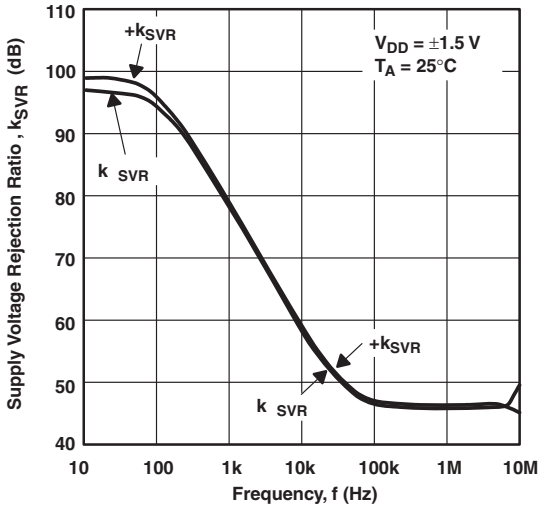


Figure 18.

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

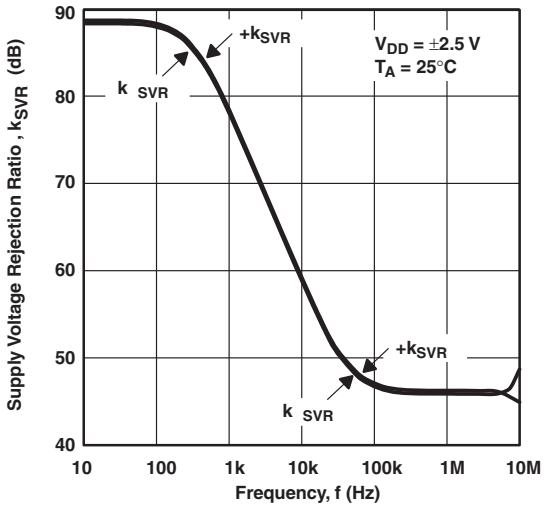


Figure 19.

SUPPLY CURRENT vs SUPPLY VOLTAGE

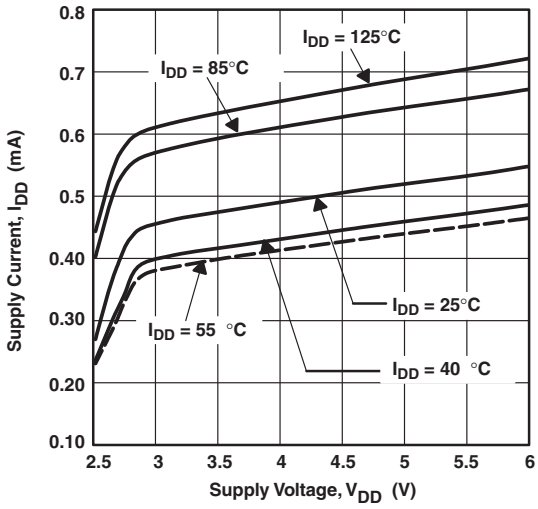


Figure 20.

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

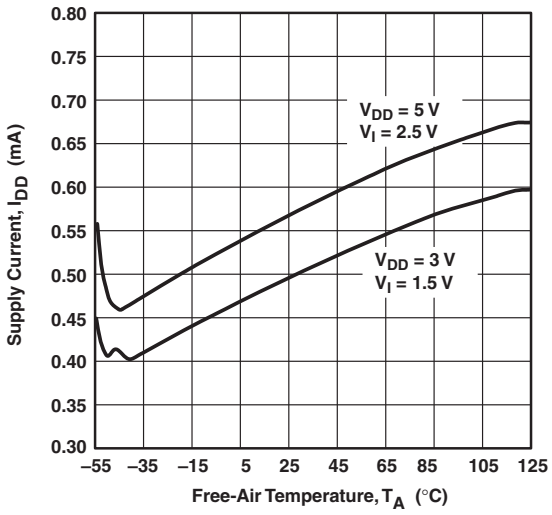


Figure 21.

AMPLIFIER WITH A SHUTDOWN PULSE TURNON CHARACTERISTICS

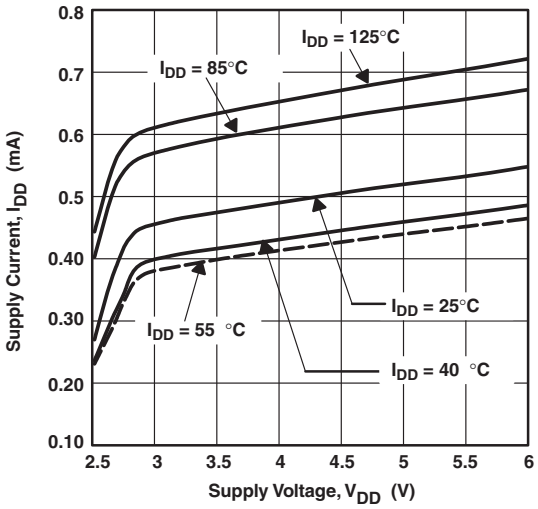


Figure 22.

AMPLIFIER WITH A SHUTDOWN PULSE TURNOFF CHARACTERISTICS

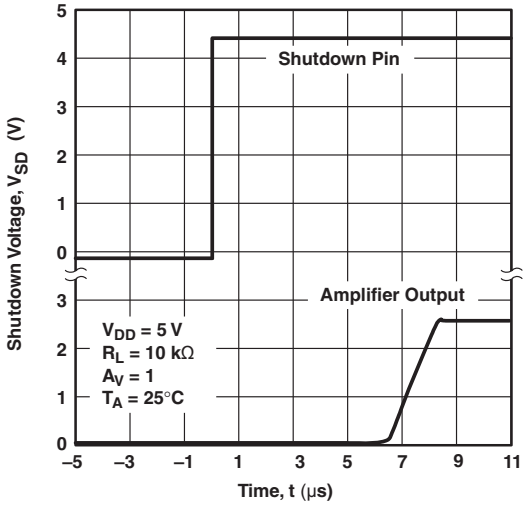


Figure 23.

SUPPLY CURRENT WITH A SHUTDOWN PULSE TURNON CHARACTERISTICS

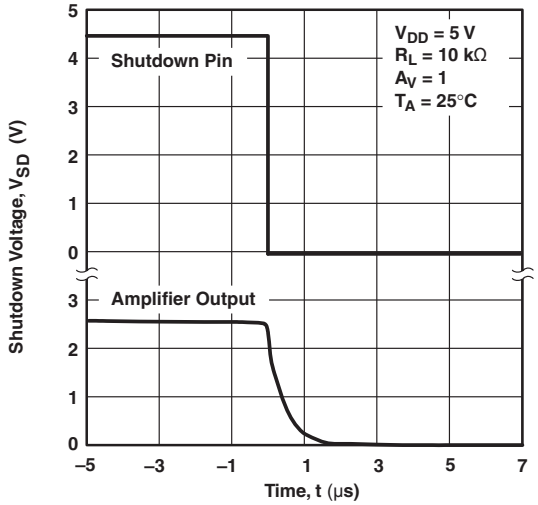


Figure 24.

TURNOFF SUPPLY CURRENT WITH A SHUTDOWN PULSE

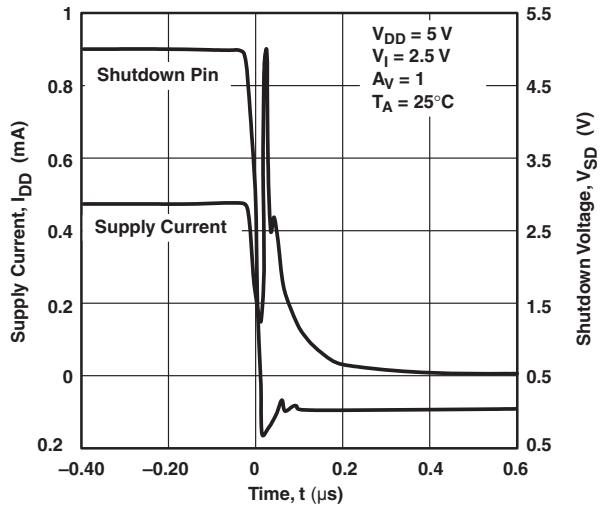


Figure 25.

SHUTDOWN SUPPLY CURRENT vs FREE-AIR TEMPERATURE

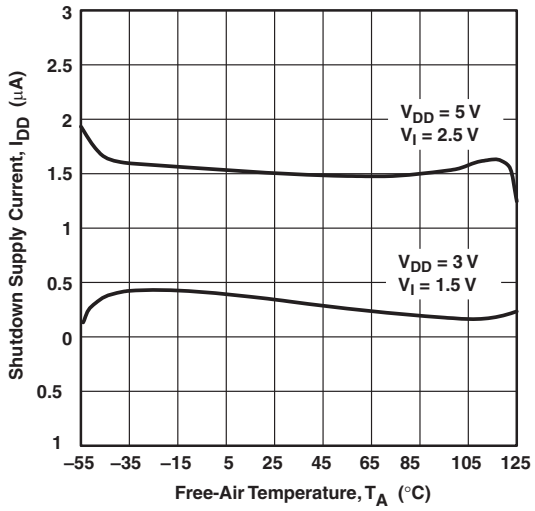


Figure 26.

SLEW RATE vs SUPPLY VOLTAGE

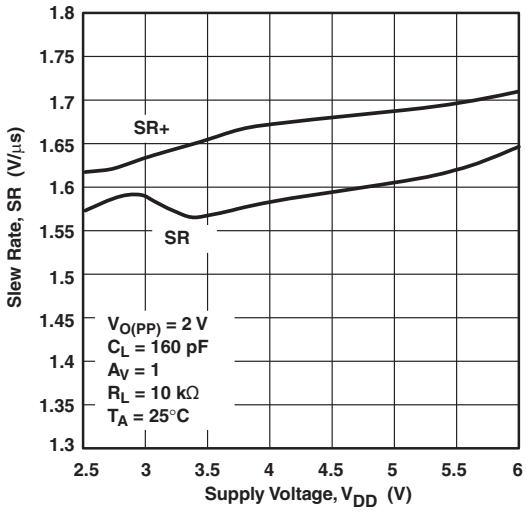


Figure 27.

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

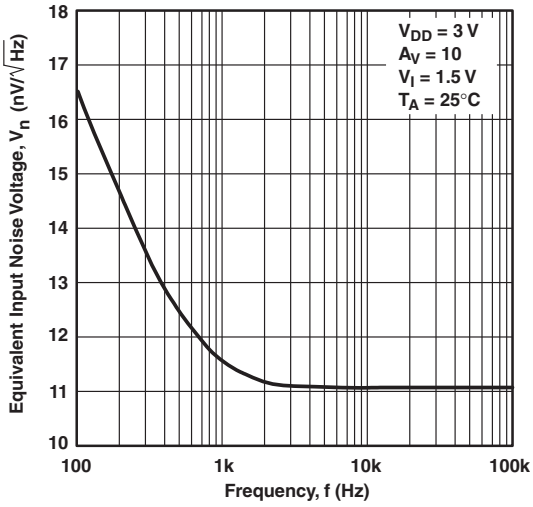


Figure 28.

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

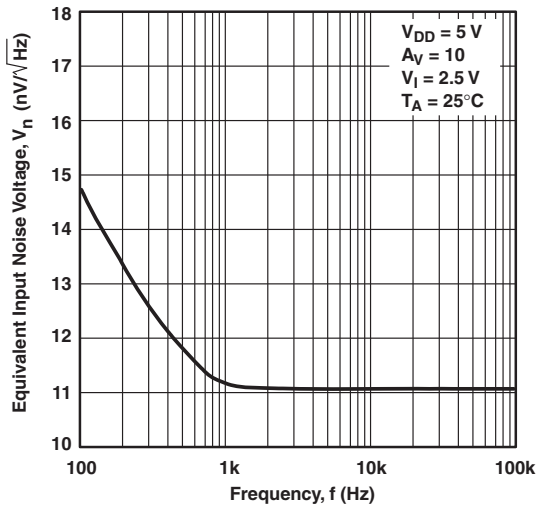


Figure 29.

EQUIVALENT INPUT NOISE VOLTAGE vs COMMON-MODE INPUT VOLTAGE

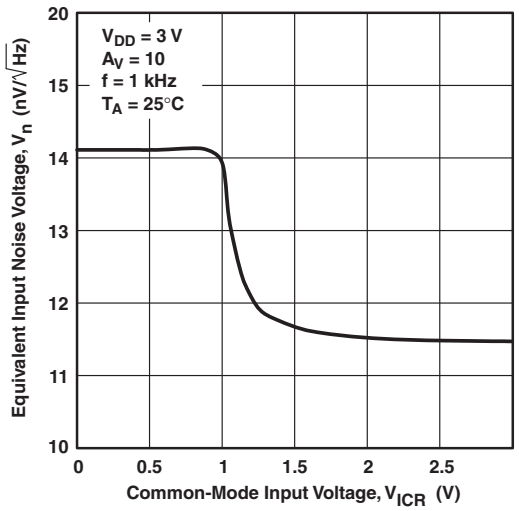


Figure 30.

EQUIVALENT INPUT NOISE VOLTAGE vs COMMON-MODE INPUT VOLTAGE

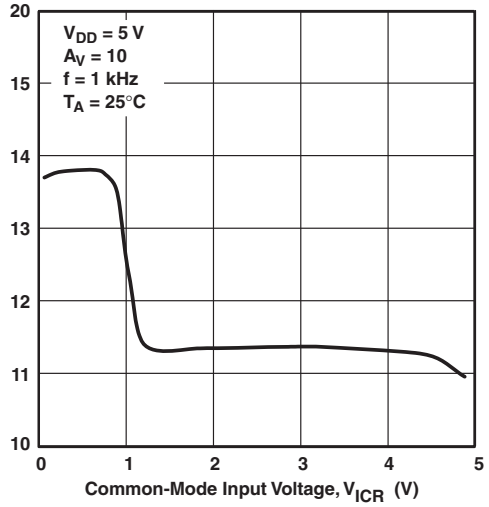


Figure 31.

TOTAL HARMONIC DISTORTION vs FREQUENCY

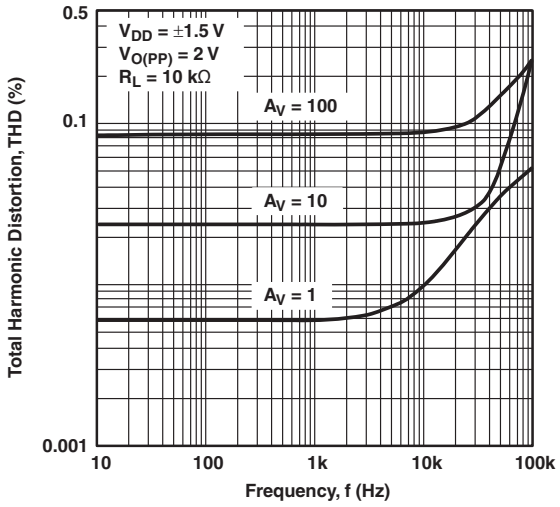


Figure 32.

TOTAL HARMONIC DISTORTION vs FREQUENCY

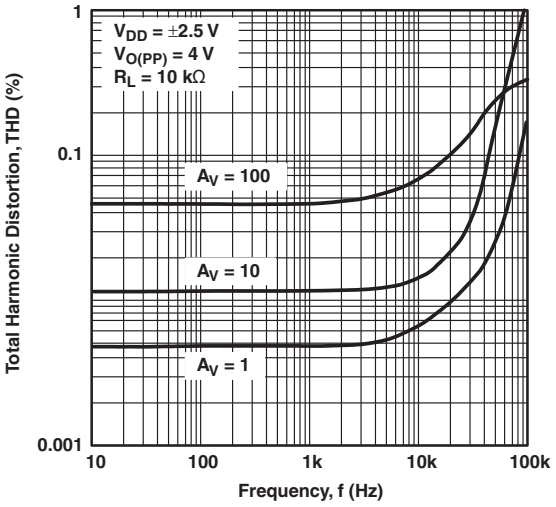


Figure 33.

TOTAL HARMONIC DISTORTION PLUS NOISE vs PEAK-TO-PEAK SIGNAL AMPLITUDE

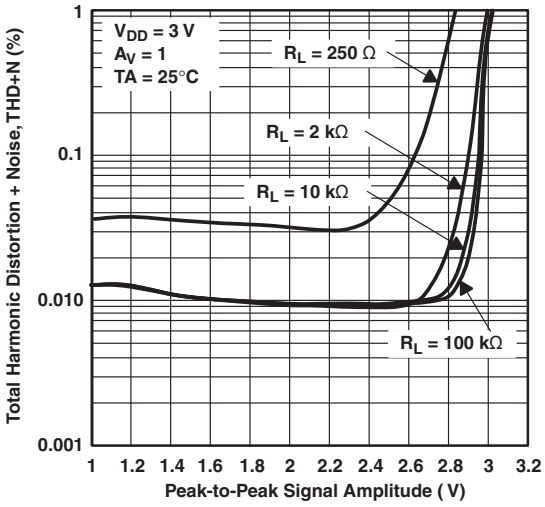


Figure 34.

TOTAL HARMONIC DISTORTION PLUS NOISE vs PEAK-TO-PEAK SIGNAL AMPLITUDE

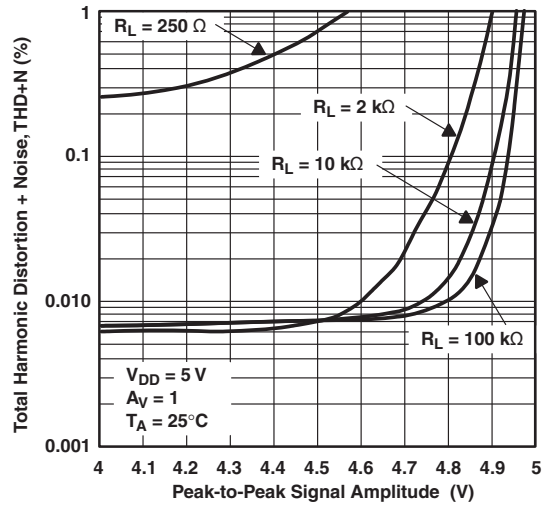


Figure 35.

PHASE MARGIN vs LOAD CAPACITANCE

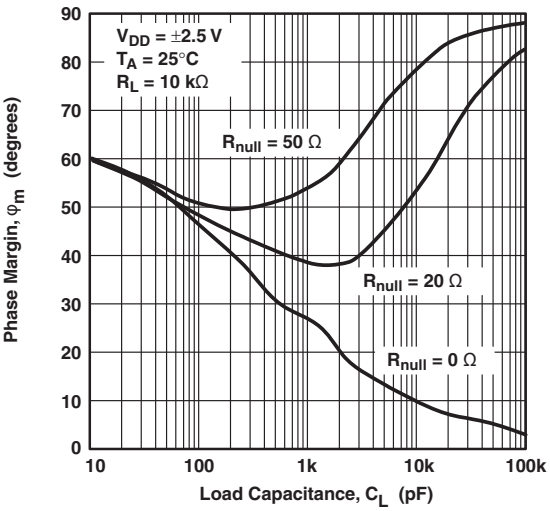


Figure 36.

PHASE MARGIN vs FREE-AIR TEMPERATURE

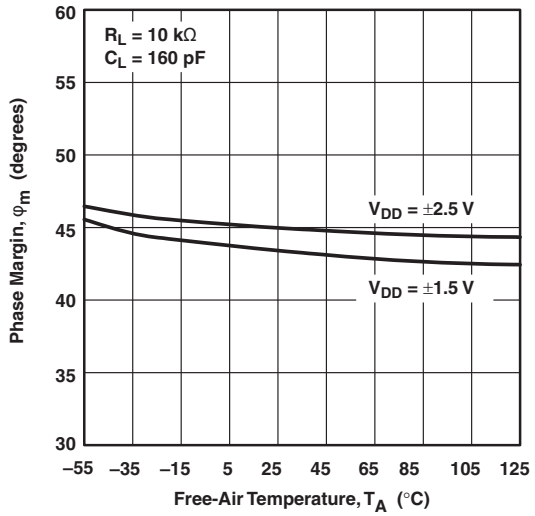


Figure 37.

GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

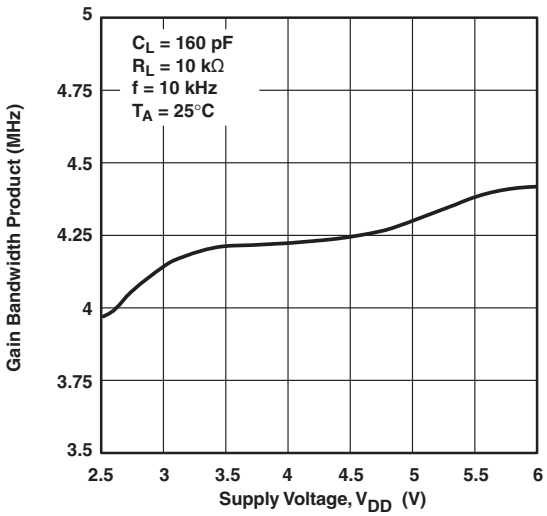


Figure 38.

GAIN BANDWIDTH PRODUCT vs FREE-AIR TEMPERATURE

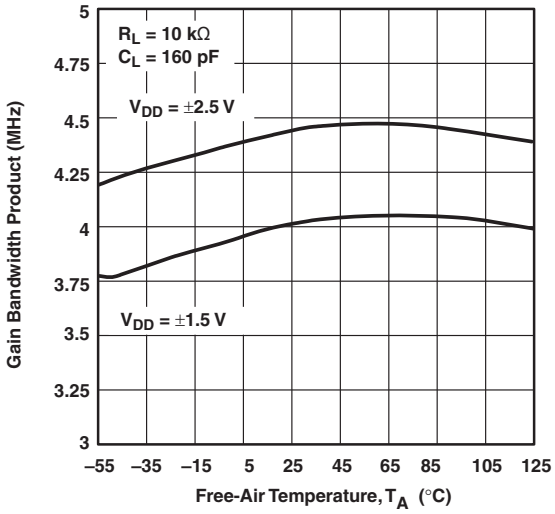


Figure 39.

LARGE SIGNAL FOLLOWER

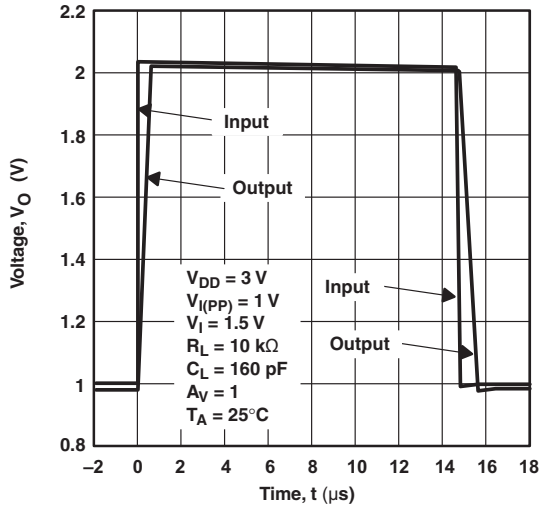


Figure 40.

LARGE SIGNAL FOLLOWER

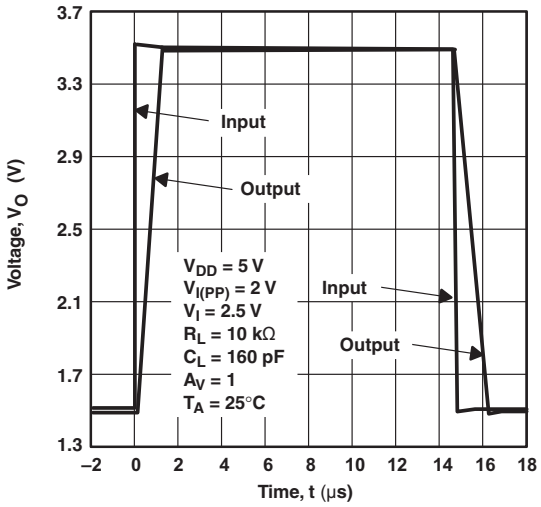


Figure 41.

SMALL SIGNAL FOLLOWER

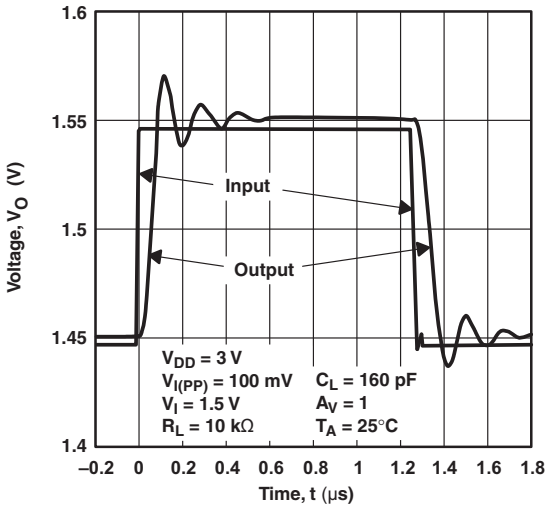


Figure 42.

SMALL SIGNAL FOLLOWER

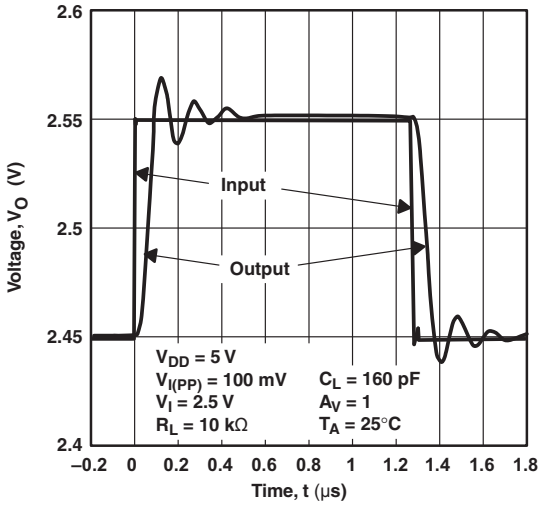


Figure 43.

INVERTING LARGE SIGNAL

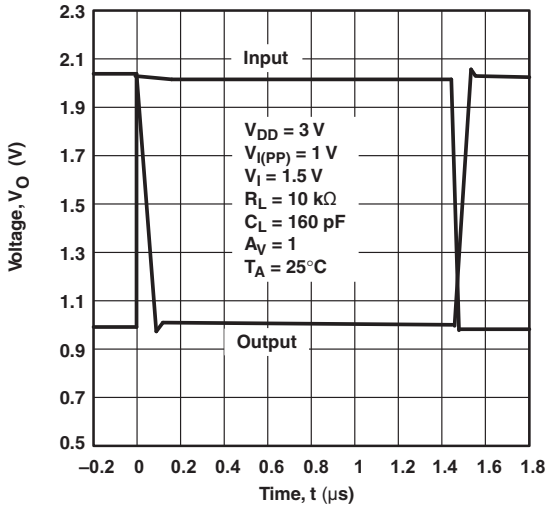


Figure 44.

INVERTING LARGE SIGNAL

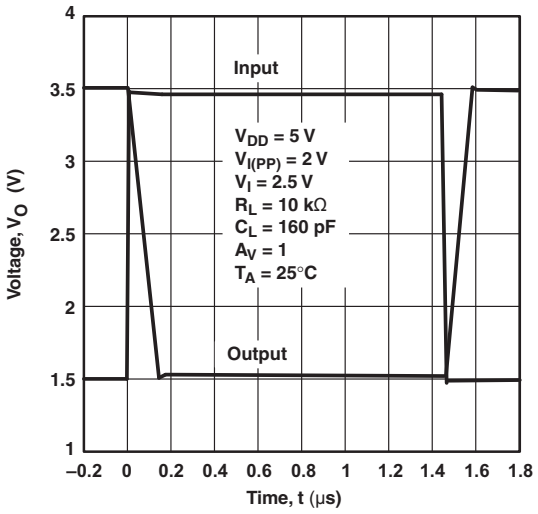


Figure 45.

INVERTING SMALL SIGNAL

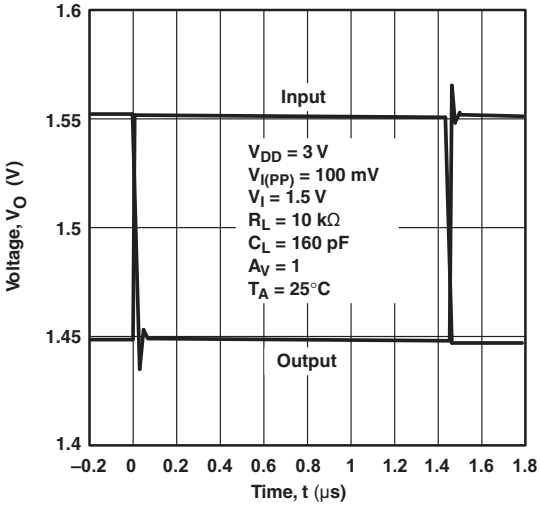


Figure 46.

INVERTING SMALL SIGNAL

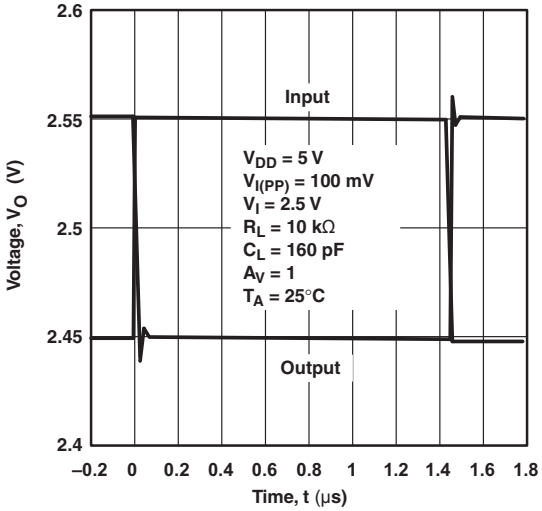


Figure 47.

PARAMETER MEASUREMENT INFORMATION

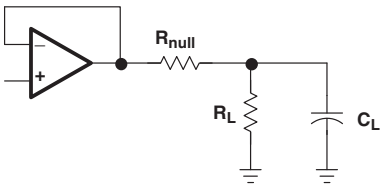


Figure 48.

APPLICATION INFORMATION

Driving a Capacitive Load

When the amplifier is configured in this manner, capacitive loading directly on the output decreases the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series (R_{NULL}) with the output of the amplifier, as shown in Figure 49. A minimum value of 20 Ω works well for most applications.

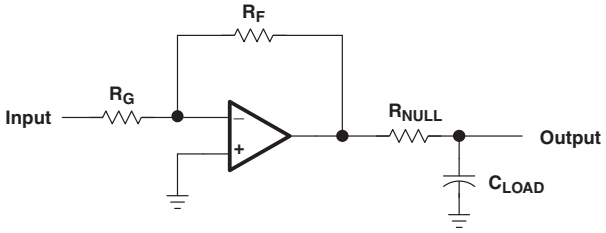
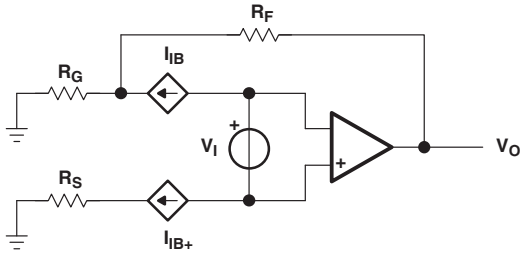


Figure 49. Driving a Capacitive Load

Offset Voltage

The output offset voltage (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The schematic and formula in Figure 50 can be used to calculate the output offset voltage.



$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB} + R_S\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-} R_F$$

Figure 50. Output Offset Voltage Model

General Configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 51).

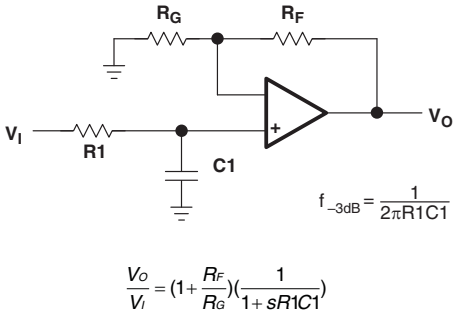


Figure 51. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is eight to ten times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

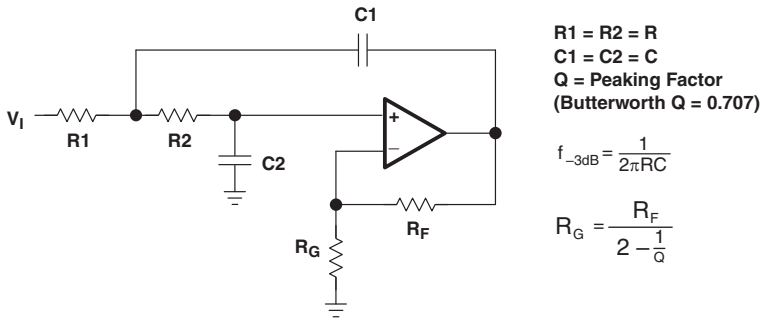


Figure 52. 2-Pole Low-Pass Sallen-Key Filter

Shutdown Function

Two members of the TLV246x family (TLV2460 and TLV2463) have a shutdown terminal for conserving battery life in portable applications. When the shutdown terminal is tied low, the supply current is reduced to 0.3 μA/channel, the amplifier is disabled, and the outputs are placed in a high-impedance mode. To enable the amplifier, the shutdown terminal can either be left floating or pulled high. When the shutdown terminal is left floating, care should be taken to ensure that parasitic leakage current at the shutdown terminal does not inadvertently place the operational amplifier into shutdown. The shutdown terminal threshold is always referenced to $V_{DD}/2$. Therefore, when operating the device with split supply voltages (e.g., ±2.5 V), the shutdown terminal must be pulled to $V_{DD}-$ (not GND) to disable the operational amplifier.

The amplifier's output with a shutdown pulse is shown in Figure 22, Figure 23, Figure 24, and Figure 25. The amplifier is powered with a single 5-V supply and configured as a noninverting configuration with a gain of 5. The amplifier turnon and turnoff times are measured from the 50% point of the shutdown pulse to the 50% point of the output waveform. The times for the single, dual, and quad are listed in the data tables.

Circuit Layout Considerations

To achieve the levels of high performance of the TLV246x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes − It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.

- Proper power supply decoupling − Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets − Sockets can be used but are not recommended. The additional lead inductance in the socket pins often leads to stability problems. Surface-mount packages soldered directly to the printed circuit board is the best implementation.
- Short trace runs/compact part placements − Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This minimizes stray capacitance at the input of the amplifier.
- Surface-mount passive components − Using surface-mount passive components is recommended for high-performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout, thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

General Power Dissipation Considerations

For a given θJA, the maximum power dissipation is shown in Figure 53 and is calculated by Equation 1:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}}\right) \quad (1)$$

Where:

P_D = Maximum power dissipation of TLV246x (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Ambient free-air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)

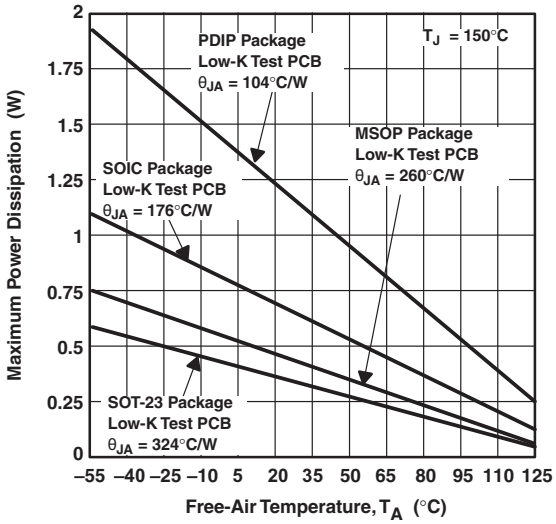


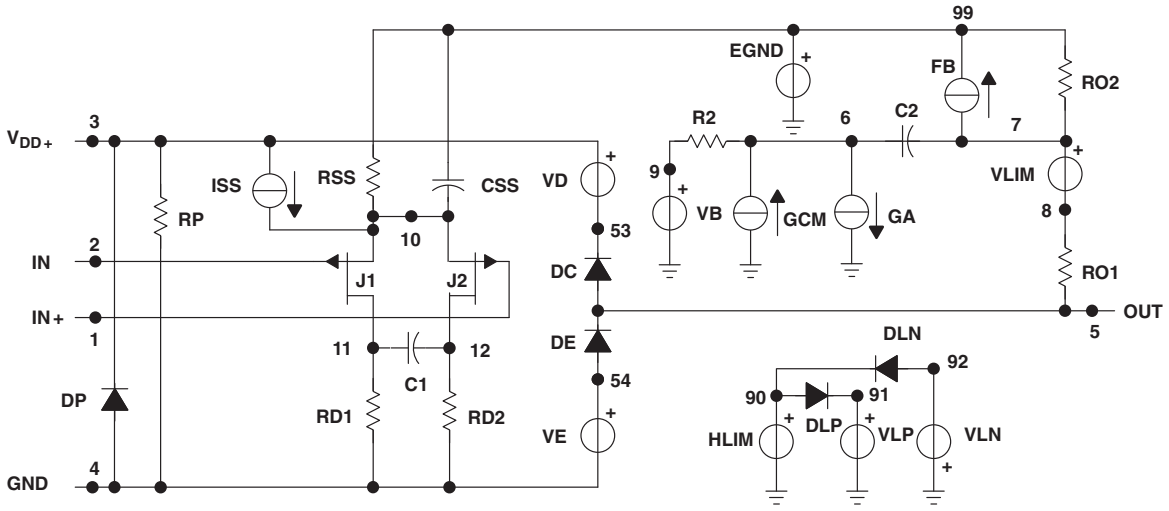
Figure 53. Maximum Power Dissipation vs Free-Air Temperature

Macromodel Information

Macromodel information provided was derived using Microsim Parts™ Release 8, the model generation software used with Microsim PSpice™. The Boyle macromodel(1) and subcircuit in Figure 54 were generated using the TLV246x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

(1) G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit




```
.SUBCKT TLV246X   1 2 3 4 5
C1        11    12    2.46034E-12
C2        6     7     10.0000E-12
CSS       10    99    443.21E-15
DC        5     53    DY
DE        54    5     DY
DLP       90    91    DX
DLN       92    90    DX
DP        4     3     DX
EGND      99    0     POLY (2) (3,0) (4,0) 0 .5 .5
FB        7     99    POLY (5) VB VC VE VLP
+ VLN 0 21.600E6 – 1E3 1E3 22E6 – 22E6
GA        6     0     11      12 345.26E- 6
GCM       0     6     10      99 15.4226E- 9
ISS       10    4     DC 18.850E- 6
HLIM      90    0     VLIM 1K
J1        11    2     10 JX1
J2        12    1     10 JX2
R2        6     9     100.00E3
RD1       3     11    2.8964E3
RD2       3     12    2.8964E3
R01       8     5     5.6000
R02       7     99    6.2000
RP        3     4     8.9127
RSS       10    99    10.610E6
VB        9     0     DC 0
VC        3     53    DC .7836
VE        54    4     DC .7436
VLIM      7     8     DC 0
VLP       91    0     DC 117
VLN       0     92    DC 117
.MODEL DX D (IS=800.00E–18)
.MODEL DY D (IS=800.00E–18 Rs = 1m Cjo=10p)
.MODEL JX1 NJF (IS=1.0000E–12 BETA=6.3239E–3
+ VTO=–1)
.MODEL JX2 NJF (IS=1.0000E–12 BETA=6.3239E–3
+ VTO=–1)
.ENDS
```

```
.subckt TLV_246Y 1 2 3 4 5 6
c1        11    12    2.4603E-12
c2        72    7     10.000E-12
css       10    99    443.21E-15
dc        70    53    dy
de        54    70    dy
dlp       90    91    dx
dln       92    90    dx
dp        4     3     dx
egnd      99    0     poly(2) (3,0) (4,0) 0 .5 .5
fb        7     99    poly(5) vb vc ve vlp vln 0
21.600E6 – 1E3 1E3 22E6 – 22E6
ga        72    0     11 12 345.26E- 6
gcm       0     72    10 99 15.422E- 9
iss       74    4     dc 18.850E- 6
hlim      90    0     vlim 1K
j1        11    2     10 jx1
j2        12    1     10 jx2
r2        72    9     100.00E3
rd1       3     11    2.8964E3
rd2       3     12    2.8964E3
ro1       8     70    5.6000
ro2       7     99    6.2000
rp        3     71    8.9127
rss       10    99    10.610E6
rs1       6     4     1G
rs2       6     4     1G
rs3       6     4     1G
rs4       6     4     1G
s1        71    4     6 4 s1x
s2        70    5     6 4 s1x
s3        10    74    6 4 s1x
s4        74    4     6 4 s2x
vb        9     0     dc 0
vc        3     53    dc .7836
ve        54    4     dc .7436
vlim      7     8     dc 0
vlp       91    0     dc 117
vln       0     92    dc 117
.model dx D(Is=800.00E–18)
.model dy D(Is=800.00E–18 Rs=1m Cjo=10p)
.model jx1 NJF(Is=1.0000E–12 Beta=6.3239E–3 Vto=–1)
.model jx2 NJF(Is=1.0000E–12 Beta=6.3239E–3 Vto=–1)
.model s1x VSWITCH(Roff=1E8 Ron=1.0 Voff=2.5 Von=0.0)
.model s2x  VSWITCH(Roff=1E8 Ron=1.0 Voff=0 Von=2.5)
.ends
```

Figure 54. Boyle Macromodel and Subcircuit

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Pea
TLV2460AQDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV2460AQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV2460AQPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV2460AQPWRQ1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV2460QDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV2460QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV2460QPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV2460QPWRQ1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV2461AQDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV2461AQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV2461AQPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV2461AQPWRQ1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV2461QDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV2461QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV2461QPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV2461QPWRQ1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV2462AQDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Pea
TLV2462AQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV2462AQPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV2462AQPWRQ1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV2462QDGKRQ1	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
TLV2462QDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV2462QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV2462QPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV2462QPWRQ1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV2463AQDRG4Q1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV2463AQDRQ1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV2463AQPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV2463AQPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260
TLV2463QDRG4Q1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV2463QDRQ1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV2463QPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV2463QPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260
TLV2464AQPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV2464AQPWRQ1	ACTIVE	TSSOP	PW	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250

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(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.
information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all
lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable fo
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package,
the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retard
in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical an
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for releas

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Cu

**OTHER QUALIFIED VERSIONS OF TLV2460-Q1, TLV2460A-Q1, TLV2461-Q1, TLV2461A-Q1, TLV2462-Q1, TLV2462A-Q1, TLV2463-Q1
TLV2464A-Q1 :**
- Catalog: TLV2460, TLV2460A, TLV2461, TLV2461A, TLV2462, TLV2462A, TLV2463, TLV2463A, TLV2464A
- Enhanced Product: TLV2462A-EP, TLV2464A-EP
- Military: TLV2460M, TLV2460AM, TLV2461M, TLV2461AM, TLV2462M, TLV2462AM, TLV2463M, TLV2463AM

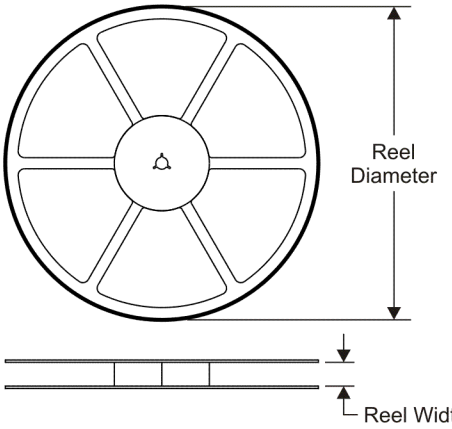
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

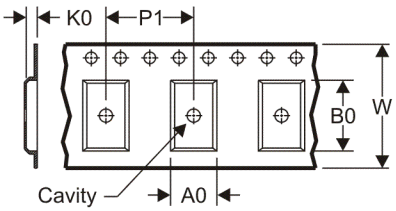
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

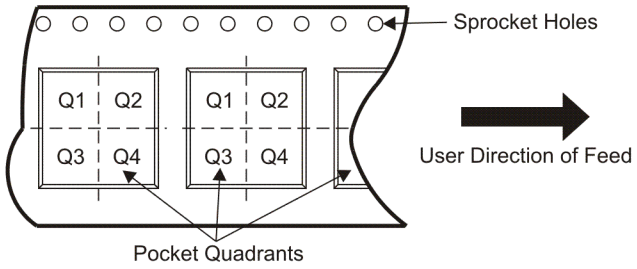


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

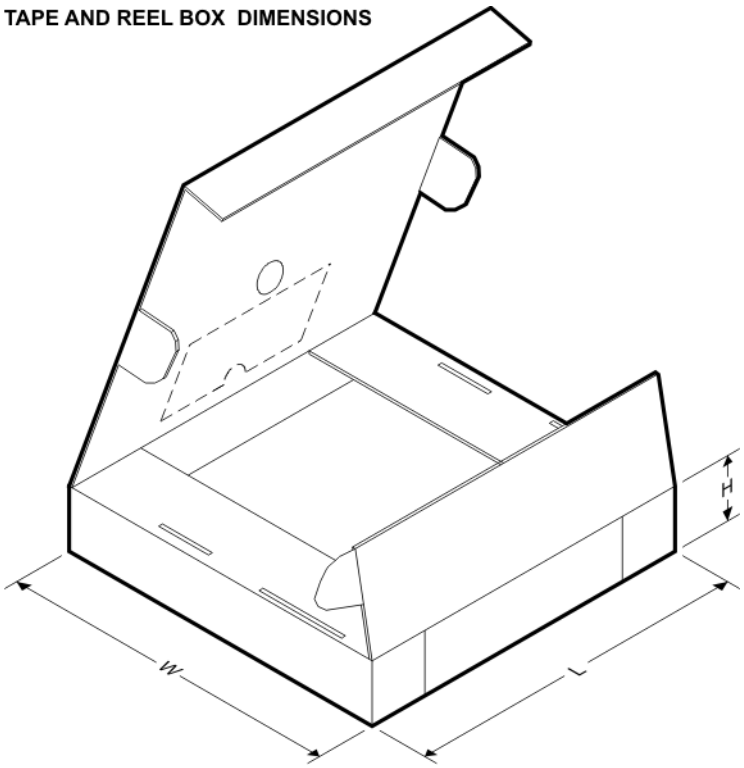
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2462QDGKRQ1	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

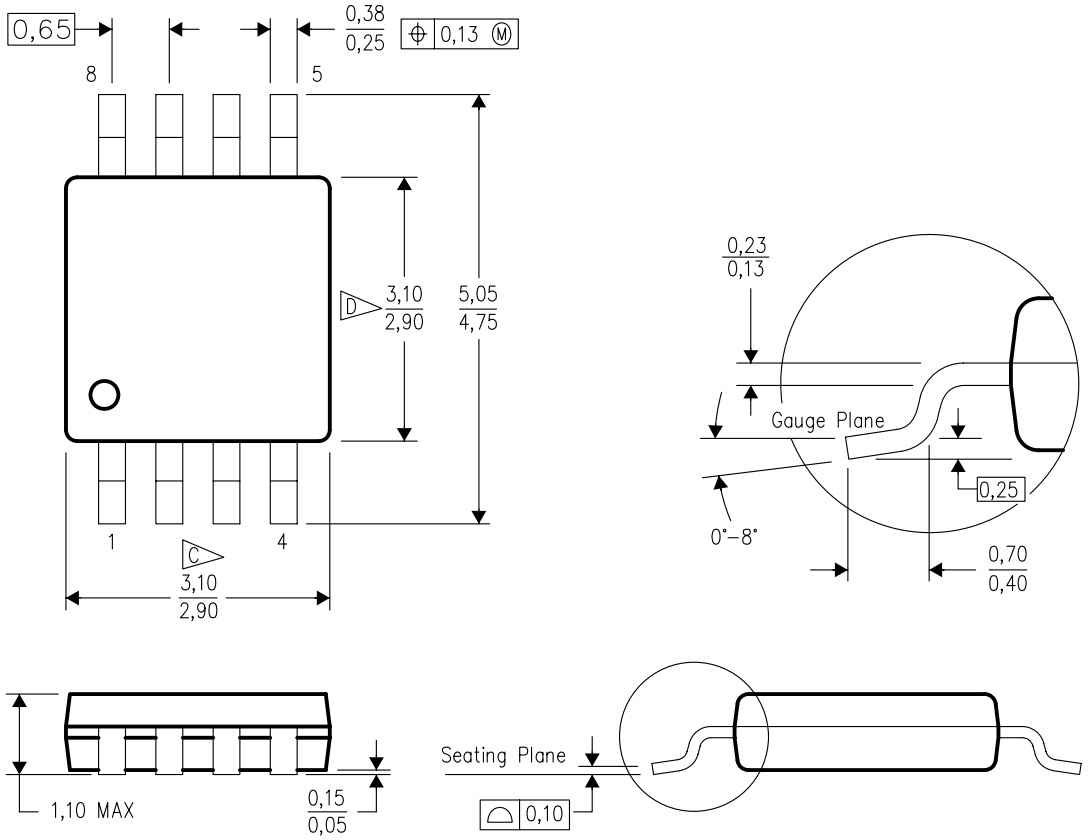
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2462QDGKRQ1	MSOP	DGK	8	2500	358.0	335.0	35.0

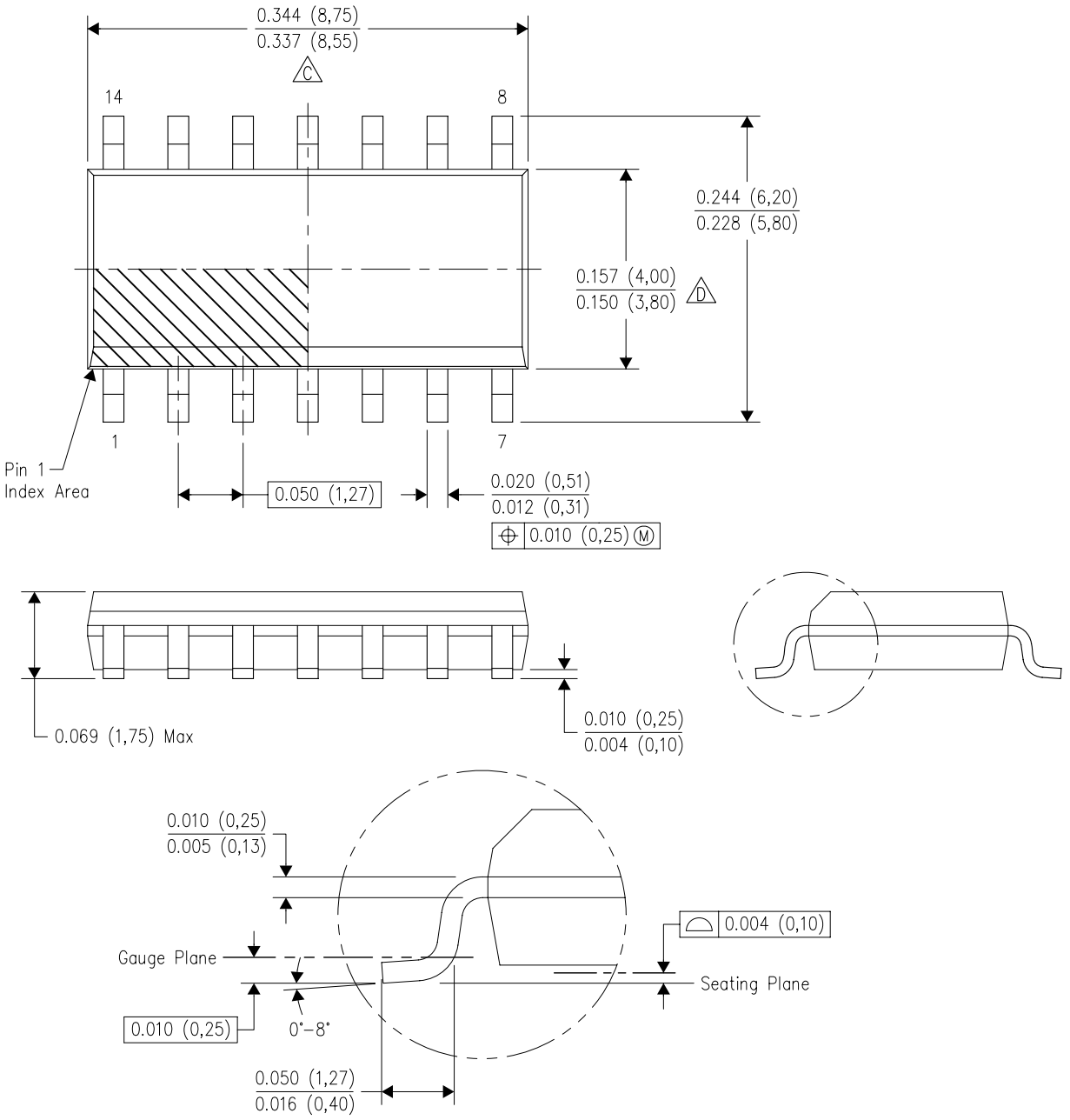
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

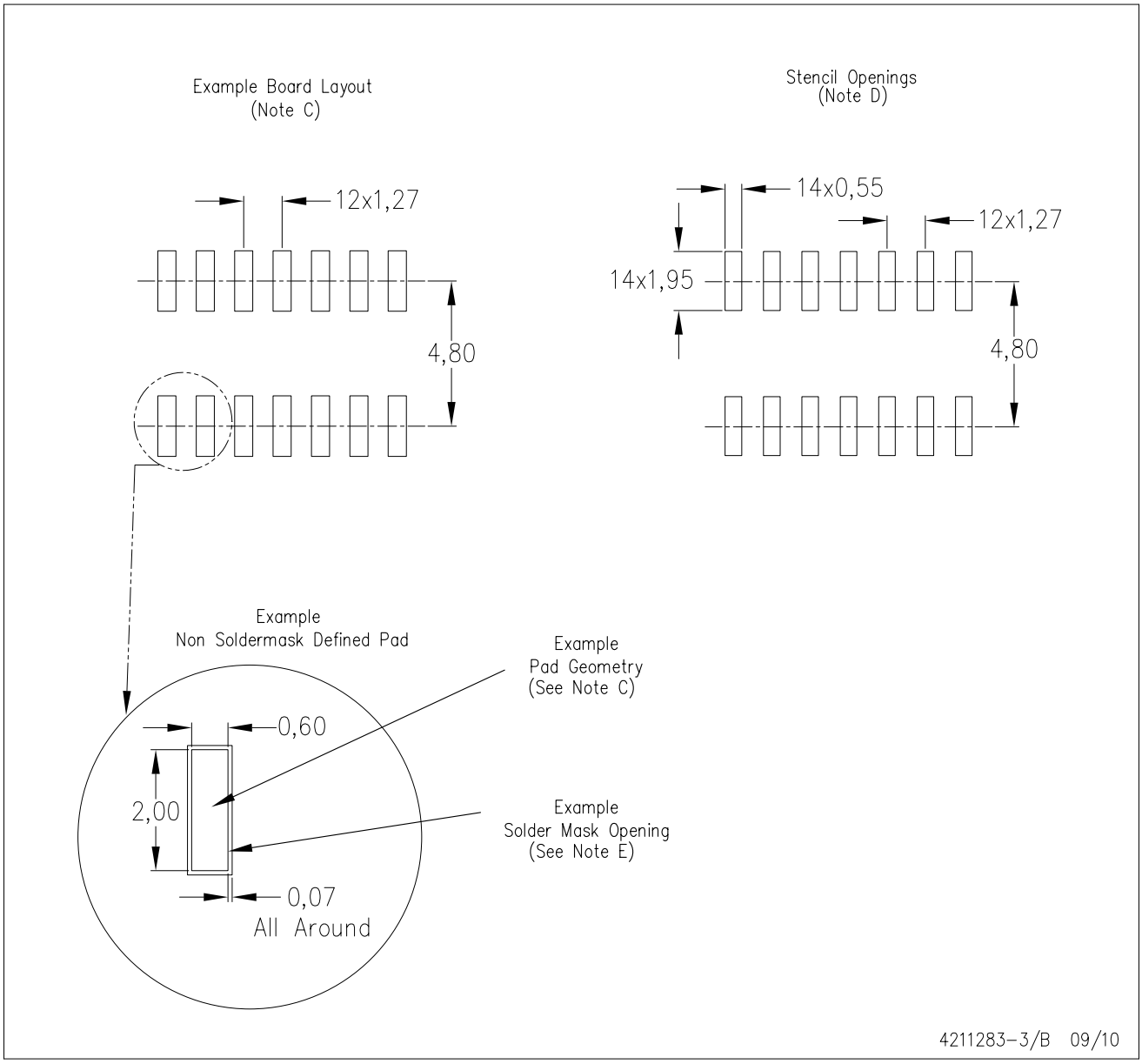
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



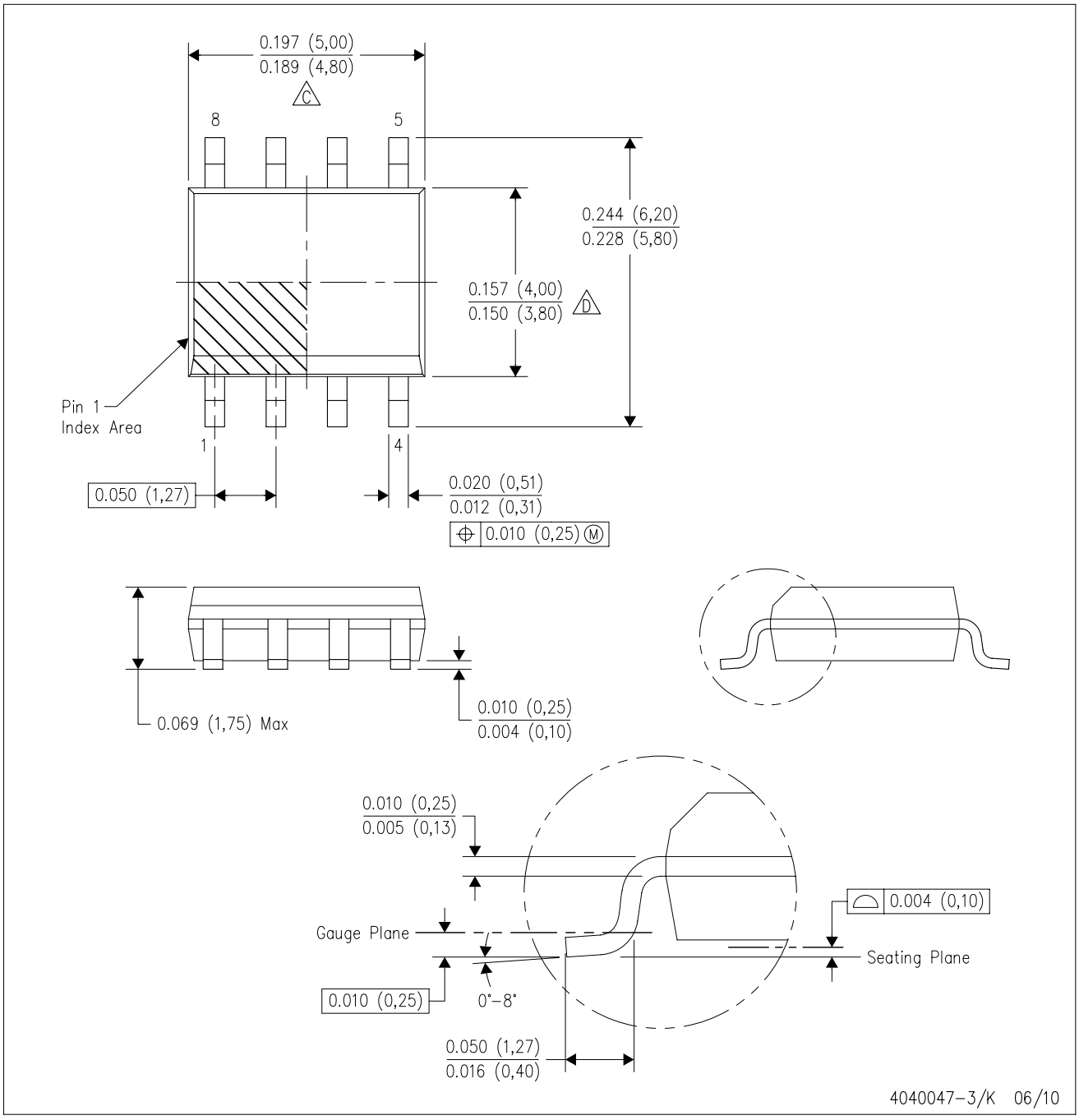
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



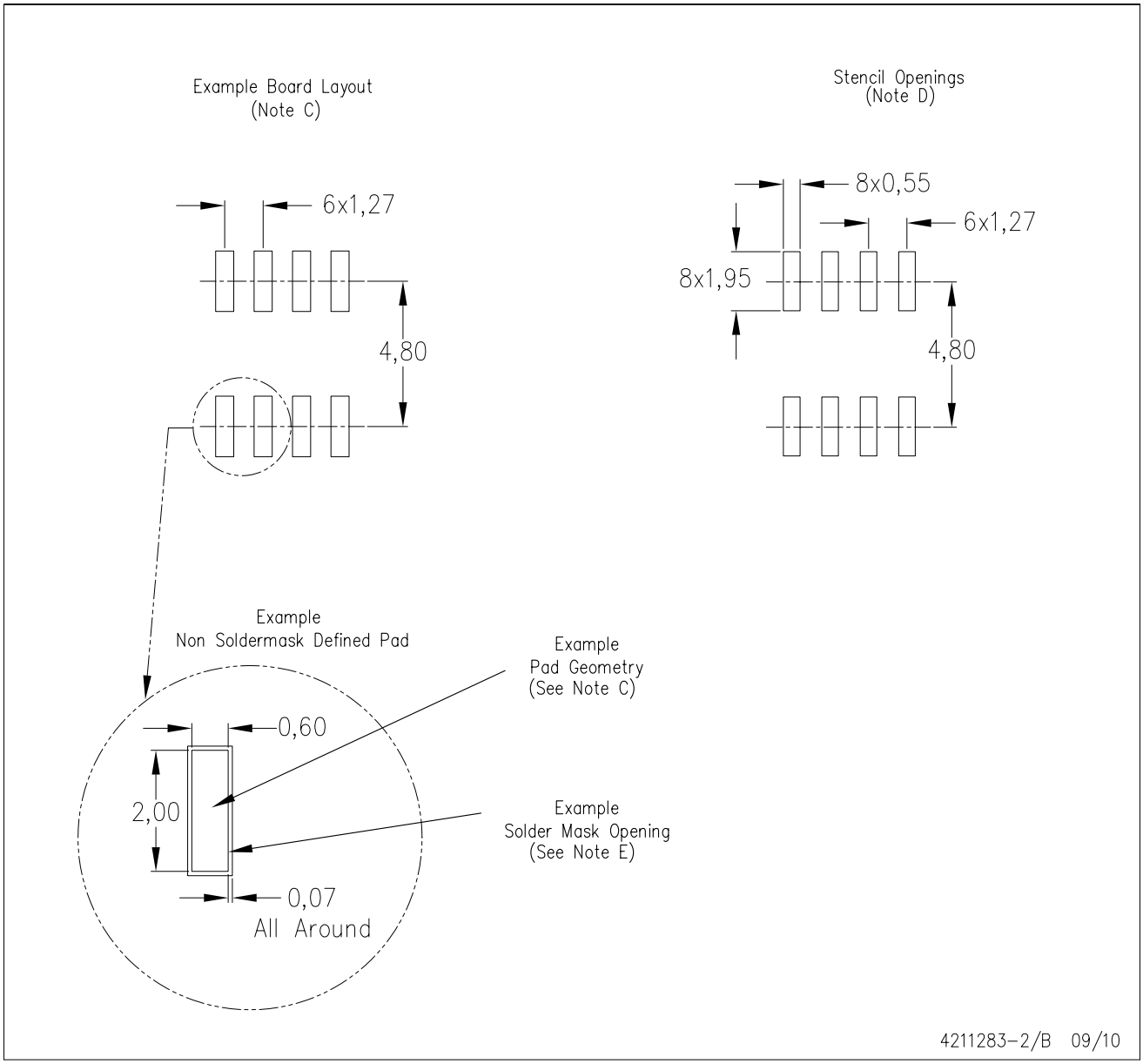
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

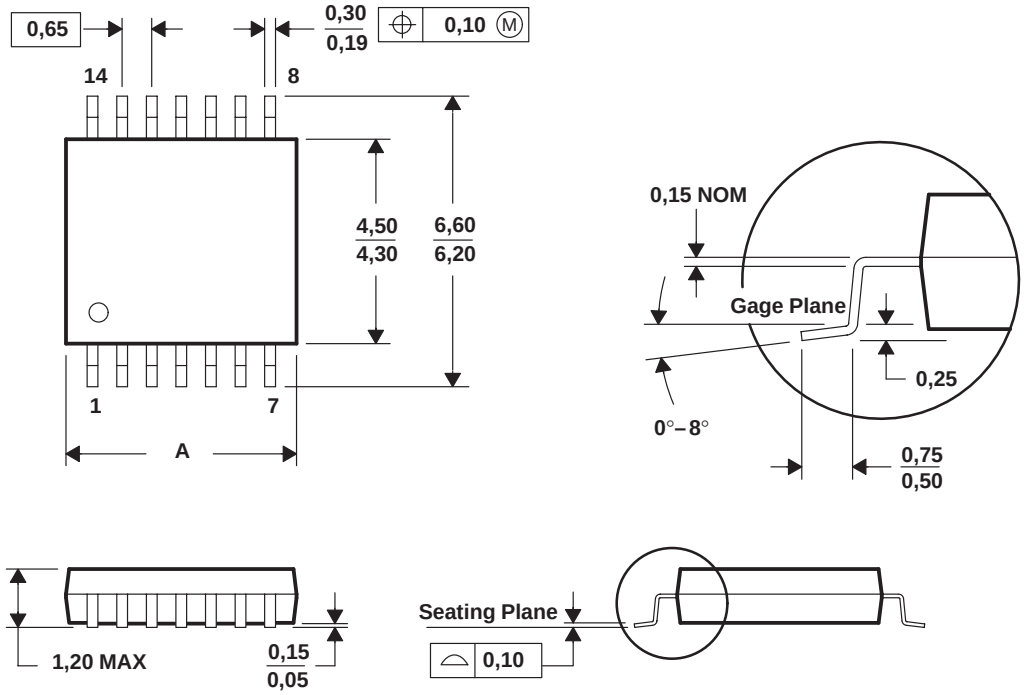
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

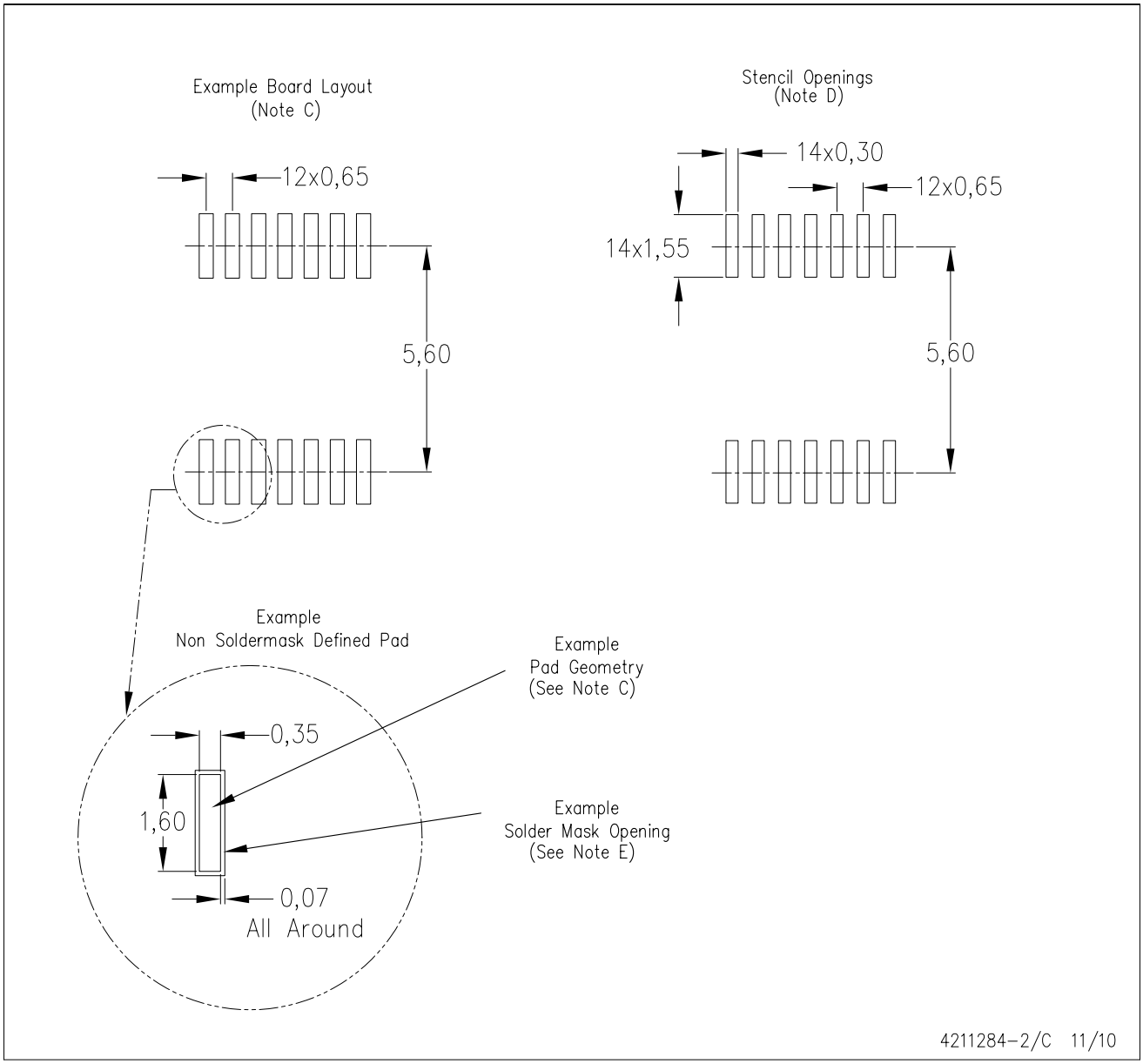


DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Space, Avionics & Defense	www.ti.com/space-avionics-defense
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video and Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless-apps

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