REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
	查询"5962-9232405MYX"供应商		

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22											

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
94-02-16

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 2K X 8 NON-VOLATILE STATIC RAM, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-92324
A	67268	

SHEET 1 OF 22

DESC FORM 193
JUL 91

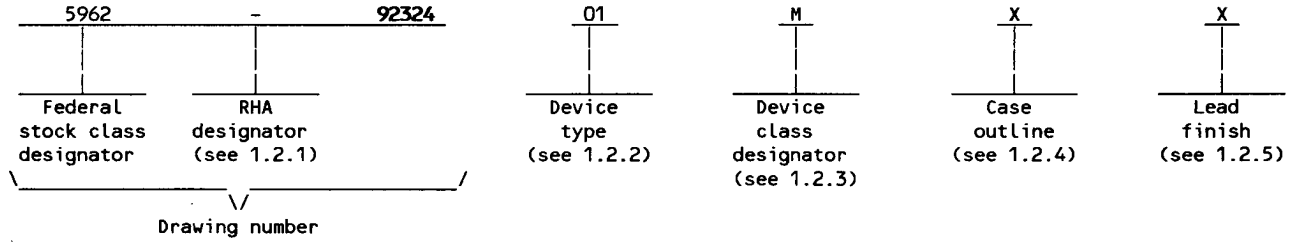
5962-E048-94

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access Time	Store Cycle	Recall Cycle	Endurance
01	11C68	8K X 8 NVSRAM	55 ns	12 ms	25 µs	10,000 cycles
02	11C68	8K X 8 NVSRAM	45 ns	12 ms	25 µs	10,000 cycles
03	11C68	8K X 8 NVSRAM	35 ns	12 ms	25 µs	10,000 cycles
04	11C68	8K X 8 NVSRAM	55 ns	12 ms	25 µs	100,000 cycles
05	11C68	8K X 8 NVSRAM	45 ns	12 ms	25 µs	100,000 cycles
06	11C68	8K X 8 NVSRAM	35 ns	12 ms	25 µs	100,000 cycles

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDIP3-T28 or GDIP4-T28	28	Dual In-Line
Y	CQCC3-N28	28	Rectangular Leadless Chip Carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1/ Generic numbers are listed on the Standardized Military Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-BUL-103 (see 6.7.2 herein).

1.3 Absolute maximum ratings. 2/ 3/

Supply voltage range (V_{CC})	-0.6 V dc to 7.0 V dc
Voltage on any ($O_{I/O}$) with outputs in high Z state	-0.5 V to (V_{CC} + 0.5 V)
Input Voltage Operating Range (V_{IH}, V_{IL})	-0.6 V dc to 7.0 V dc
Storage Temperature Range	-65°C to +150°C
Maximum Power Dissipation (P_D)	1.0 W
Maximum Output Current	15 mA
Lead Temperature (Soldering)	300°C
Junction Temperature (T_J) 4/	175°C
Thermal Resistance, Junction to Case (θ_{jc}): Cases X,Y	See MIL-STD-1835
Data Retention	10 Years to nonvolatile array (minimum)
Endurance (as Store cycles to non-volatile array)	Per 1.2.2

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Case Operating Temperature Range (T_C)	-55°C to +125°C
Input Voltage, low range (V_{IL})	V_{SS}-0.5 V dc to 0.8 V dc, all inputs
Input Voltage, high range (V_{IH})	2.2 V dc to V_{CC}+0.5 V dc, all inputs

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) . . . . . 5/ percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may affect reliability. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied.
3/ All voltages are referenced to V_{SS} (ground).
4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
5/ Values will be added when they become available.

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Pennsylvania Street, N.W., Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit will be provided when RHA product becomes available.

3.2.5 Functional tests. Various functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device class M, alternate test patterns shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes Q and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 41 (see MIL-I-38535, appendix A).

3.11 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This reprogrammability test shall be done for initial characterization and after any design or process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but shall guarantee the number of program/erase endurance cycles listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

3.12 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process changes which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V $4.5\ V \le V_{CC} \le 5.5\ V$ (unless otherwise specified) $I_{OUT} = 0$ mA	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input leakage current (any input)	I_{IL}	$V_{CC} = 5.5$ V $V_{IN} = V_{SS}$ to V_{CC}	1,2,3	All		±1	µA
High impedance output leakage current	I_{OL}	$V_{CC} = 5.5$ V $V_{IN} = V_{SS}$ to V_{CC}	1,2,3	All		±5	µA
Input logic "1" voltage	V_{IH}	All Inputs	1,2,3	All	2.2	V_{CC}+.5	V
Input logic "0" voltage	V_{IL}	All Inputs	1,2,3	All	V_{SS}-.5	0.8	V
Output logic "1" voltage	V_{OH}	$I_{OH} = -4$ mA	1,2,3	All	2.4		V
Output logic "0" voltage	V_{OL}	$I_{OL} = 8$ mA	1,2,3	All		0.4	V
V_{CC} current 1/	I_{CC1}	Addresses cycling at t_{AVAV}	1,2,3	01,04 02,05 03,06		70 75 80	mA
V_{CC} current 2/ during store cycle	I_{CC2}	$\overline{CE} \ge (V_{CC} - 0.2V)$; all other inputs $V_{IN} \le 0.2$ V or $\ge (V_{CC} - 0.2$ V)	1,2,3	All		50	mA
V_{CC} current (standby, cycling TTL input levels) 3/	I_{CC3}	$\overline{CE} \ge V_{IH}$; all others cycling	1,2,3	01,04 02,05 03,06		20 23 27	mA
V_{CC} DC current (standby, stable CMOS input levels) 2/	I_{CC4}	$\overline{CE} \ge (V_{CC} - 0.2$ V); all others $V_{IN} \le 0.2$ V or $\ge (V_{CC} - 0.2V)$	1,2,3	All		2	mA
Input capacitance 4/	C_{IN}	$V_{IN} = 0$ V $T_A = 25°C$, f = 1.0 MHz See 4.4.1e	4	All		5	pF
Output capacitance 4/	C_{OUT}	$V_{OUT} = 0$ V $T_A = 25°C$, f = 1.0 MHz See 4.4.1e	4	All		7	pF
Functional tests		See 4.4.1c	7,8A,8B	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{SS} = 0 V 4.5 V $\le V_{CC} \le$ 5.5 V (unless otherwise specified) I_{OUT} = 0 mA	Group A subgroups	Device type	Limits		Unit
					Min	Max	
READ CYCLES 1 & 2							
Chip enable access time	t_{ELQV}	See figures 3 and 4	9,10,11	01,04		55	ns
				02,05		45	
				03,06		35	
Read cycle time 5/	t_{AVAV}		9,10,11	01,04	55		ns
				02,05	45		
				03,06	35		
Address access time 6/	t_{AVQV}		9,10,11	01,04		55	ns
				02,05		45	
				03,06		35	
Output enable to data valid	t_{OLQV}		9,10,11	01,02, 04,05		25	ns
				03,06		20	
Output hold after address change	t_{AXQX}		9,10,11	All	5		ns
Chip enable to output active	t_{ELQX}		9,10,11	All	5		ns
Chip disable to output 7/ inactive	t_{EHQZ}		9,10,11	01,02, 04,05		25	ns
				03,06		20	
Output enable to output active	t_{OLQX}		9,10,11	All	0		ns
Output disable to output 7/ inactive	t_{OHQZ}		9,10,11	01,02, 04,05		25	ns
				03,06		20	
Chip enable to power 4/ active	t_{ELPU}		9,10,11	All	0		ns
Chip disable to power 3/ 4/ standby	t_{EHPD}		9,10,11	All		25	ns
Write recovery time	t_{WHQV}		9,10,11	01,04		65	ns
				02,05		55	
				03,06		45	
WRITE CYCLES 1 & 2							
Write cycle time	t_{AVAV}	See figures 3 and 4	9,10,11	01,04	55		ns
				02,03, 05,06	45		
Write pulse width	t_{WLWH} t_{WLEH}		9,10,11	01,04	45		ns
				02,03, 05,06	35		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{SS} = 0 V 4.5 V $\le V_{CC} \le$ 5.5 V (unless otherwise specified) I_{OUT} = 0 mA	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Chip enable to end of write	t_{ELWH} t_{ELEH}	See figures 3 and 4	9,10,11	01,04	45		ns
				02,03, 05,06	35		
Data set-up to end of write	t_{DVWH} t_{DVEH}		9,10,11	All	30		ns
Data hold after end of write	t_{WHDX} t_{EHDX}		9,10,11	All	0		ns
Address set-up to end of write	t_{AVWH} t_{AVEH}		9,10,11	01,04	45		ns
				02,03, 05,06	35		
Address set-up to start of write	t_{AVWL} t_{AVEL}		9,10,11	All	0		ns
Address hold after end of write	t_{WHAX} t_{EHAX}		9,10,11	All	0		ns
Write enable to output disable 7/ 8/	t_{WLQZ}		9,10,11	All		35	ns
Output active after end of write	t_{WHQX}		9,10,11	All	5		ns
STORE/RECALL CYCLE							
Store/recall initiation cycle time	t_{AVAV}	See figures 3 and 4	9,10,11	01,04	55		ms
				02,05	45		
				03,06	35		
Chip enable to output 9/ inactive	t_{ELQZ}		9,10,11	01,04		85	ns
				02,03, 05,06		75	
Store cycle time 10/	t_{STORE}		9,10,11	All		12	ms
Recall cycle time 11/	t_{RECALL}		9,10,11	All		25	µs
Address set-up to chip 12/ enable	t_{AVEL}		9,10,11	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V $4.5 \text{ V} \le V_{CC} \le 5.5$ V (unless otherwise specified) $I_{OUT} = 0$ mA	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Chip enable pulse width 12/ 13/	t_{ELEH}	See figures 3 and 4	9,10,11	01,04		45	ns
				02,05		35	
				03,06		25	
Chip disable to address change 12/	t_{EHAX}		9,10,11	All	0		ns

1/ I_{CC1} is dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.
2/ Bringing $\overline{CE} > V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out. See Figure 3.
3/ I_{CC2} is the current required for the duration of the store cycle (t_{STORE}) once a store has begun.
4/ These parameters are tested as part of initial device characterization, and after any design or process change that might affect that parameter. These parameters are not tested as part of lot by lot screening, but are guaranteed to the limits specified in Table I.
5/ For Read Cycles 1 and 2, $\overline{WE}$ is high for the entire cycle.
6/ The device is continuously selected with $\overline{CE}$ low and $\overline{OE}$ low.
7/ Measured ±200 mV from steady state output voltage.
8/ If $\overline{WE}$ is low when $\overline{CE}$ goes low, the outputs remain in the high impedance state.
9/ Once the software STORE or RECALL cycle is initiated, it completes automatically, ignoring all inputs.
9/ Once the software STORE or RECALL cycle is initiated, it completes automatically, ignoring all inputs.
10/ Note that STORE cycles, but not RECALL cycles, are aborted by $V_{CC} < 3.8$ V (STORE inhibit).
11/ A RECALL cycle is initiated automatically at power up when V_{CC} exceeds 3.8 V. t_{RECALL} is measured from the point at which V_{CC} exceeds 4.5 V.
12/ Noise on the $\overline{CE}$ pin may trigger multiple read cycles from the same address and abort the address sequence.
13/ If the $\overline{CE}$ pulse width is less than t_{ELQV}, but greater than or equal to t_{ELEH}, then the data may not be valid at the end of the low pulse. However, the STORE or RECALL will still be initiated.

Device types	All
Case outlines	X,Y
Terminal number	Terminal symbol
1	NC
2	A_{12}
3	A_7
4	A_6
5	A_5
6	A_4
7	A_3
8	A_2
9	A_1
10	A_0
11	DQ_0
12	DQ_1
13	DQ_2
14	V_{SS}
15	DQ_3
16	DQ_4
17	DQ_5
18	DQ_6
19	$\overline{DQ}_7$
20	$\overline{CE}$
21	A_{10}
22	$\overline{OE}$
23	A_{11}
24	A_9
25	A_8
26	$\overline{NC}$
27	$\overline{WE}$
28	V_{CC}

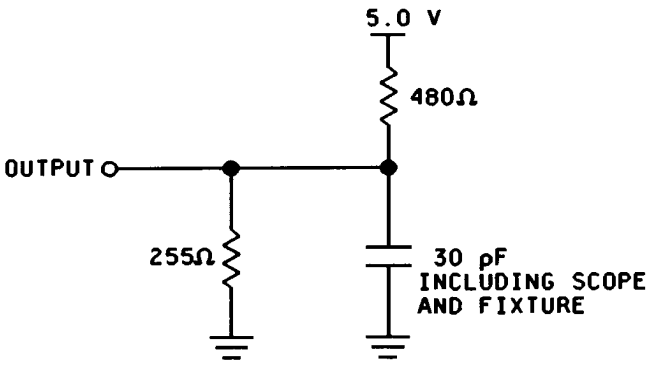
FIGURE 1. Terminal connections.

$\overline{CE}$	$\overline{WE}$	$A_{12} - A_0$ (HEX)	MODE	I/O	POWER
H	X	X	Not Selected	Output high Z	Standby
L	H	X	Read SRAM	Output data	Active
L	L	X	Write SRAM	Input data	Active
L	H	0000 1/ 1555 1/ 0AAA 1/ 1FFF 1/ 1010 1/ 0F0F 1/	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile store	Output data 2/ Output data 2/ Output data 2/ Output data 2/ Output data 2/ Output high Z	Active I_{CC2}
L	H	0000 1/ 1555 1/ 0AAA 1/ 1FFF 1/ 1010 1/ 0F0E 1/	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile recall	Output data 2/ Output data 2/ Output data 2/ Output data 2/ Output data 2/ Output high Z 2/	Active

1/ The six consecutive addresses must be in the order listed - (0000, 1555, 0AAA, 1FFF, 10F0, 0F0F) for a STORE cycle, or (0000, 1555, 0AAA, 1FFF, 10F0, 0F0E) for a RECALL cycle. WE must be high during all six consecutive cycles. See figure 4.

2/ I/O state assumes that $\overline{OE}$ is $\leq V_{IL}$. Initiation and operation of nonvolatile cycles do not depend on the state of OE.

FIGURE 2. Truth Table.



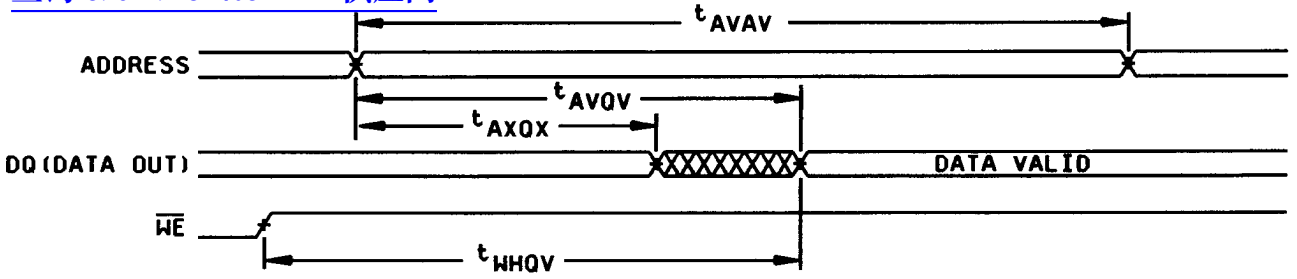
AC TEST CONDITIONS 1/

TEST CONDITION	VALUES
Input pulse levels	Gnd to 3V
Input rise & fall time	≤ 5 ns
Input timing reference levels	1.5V dc
Output reference levels	1.5V dc

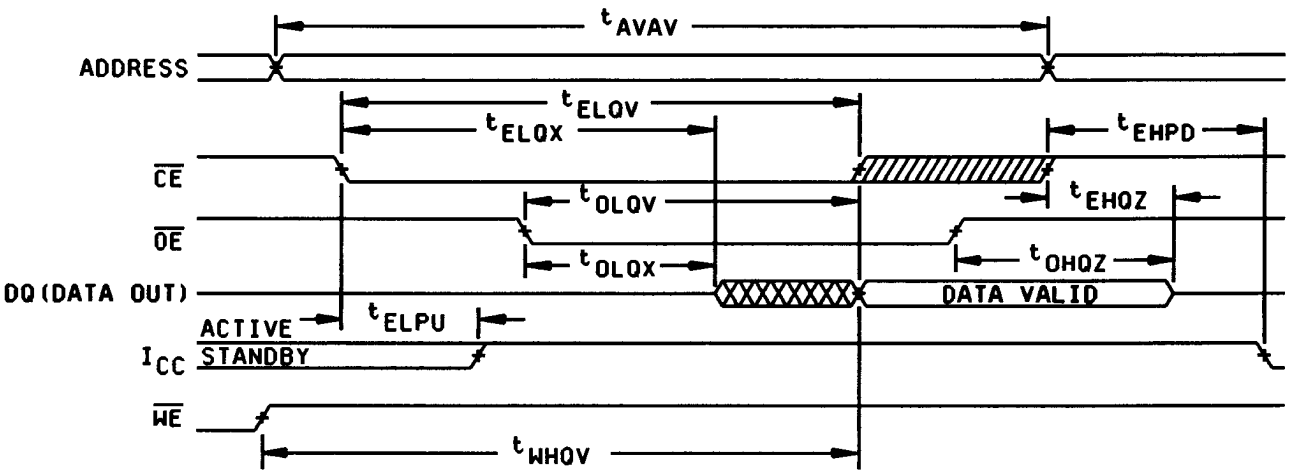
1/ All voltages are referenced to V_{SS} (ground).

FIGURE 3. Output load circuits.

Read cycle 1 (see notes 1 and 2)



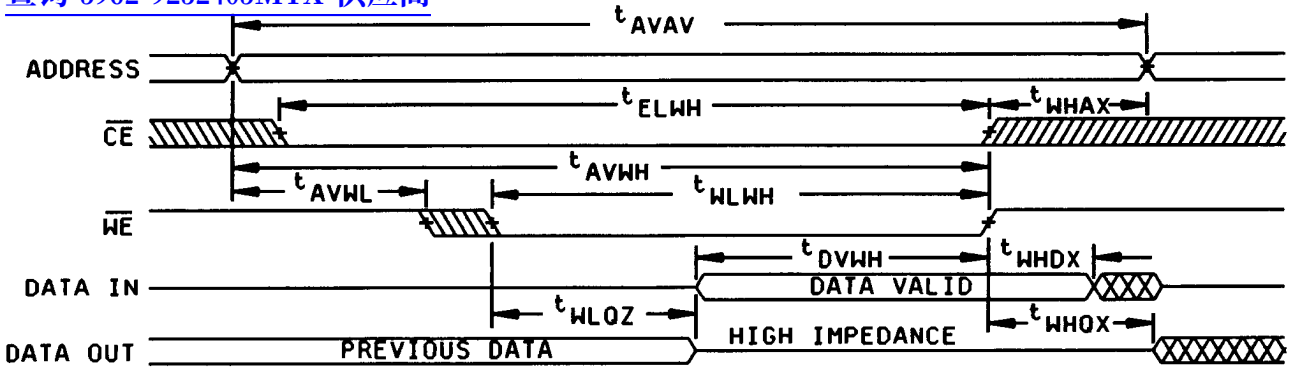
Read cycle 2 (see notes 1 and 2)



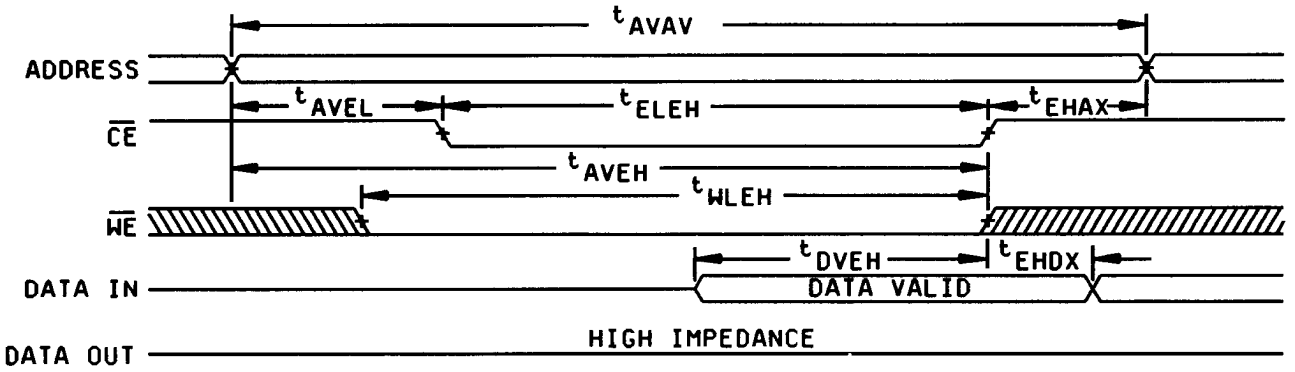
Notes:
1. The device is continuously selected with $\overline{CE}$ low and $\overline{OE}$ low.
2. For READ CYCLE 1 and 2, $\overline{WE}$ must be high for entire cycle.

Figure 4. Timing waveforms.

Write cycle 1: $\overline{WE}$ controlled (see note)



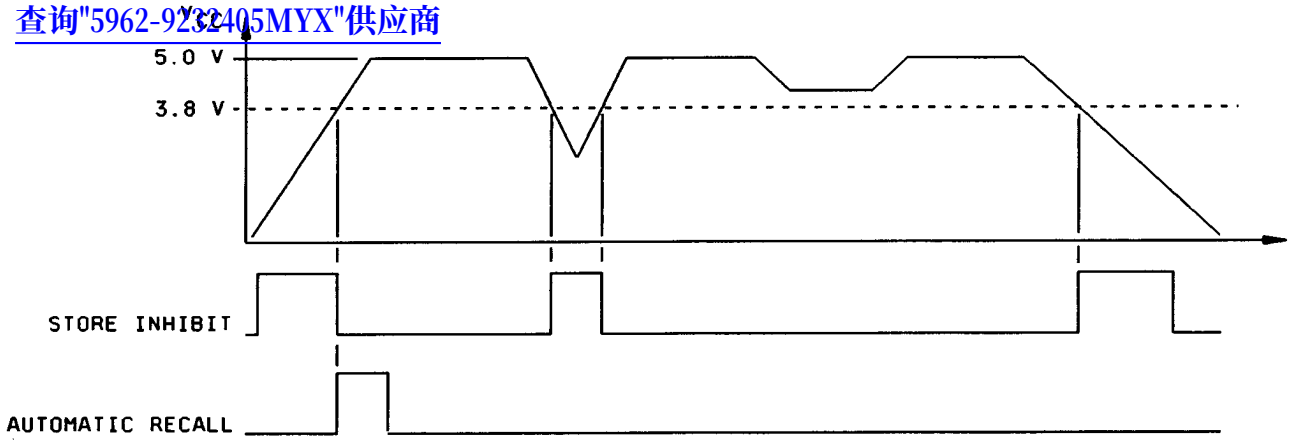
Write cycle 2: $\overline{CE}$ controlled (see note)



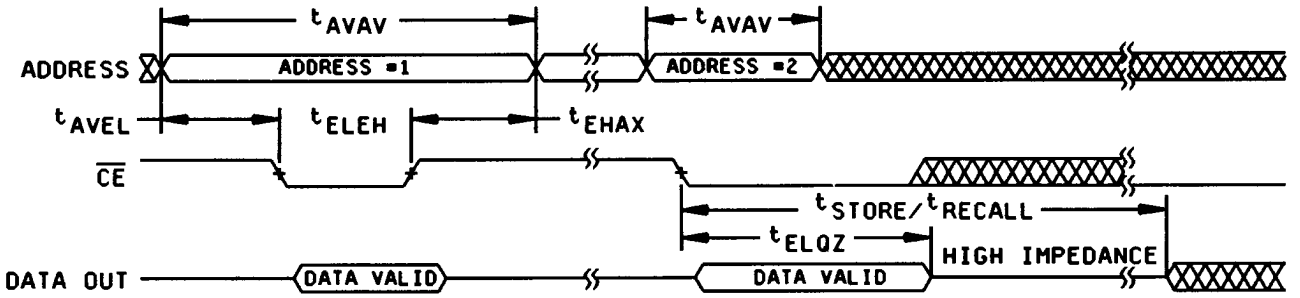
Note: $\overline{CE}$ or $\overline{WE}$ must be ≥ V_{IH} during address transitions.

Figure 4. Timing waveforms - continued.

Store inhibit and automatic power-up recall



Store/recall cycle (see note 3)



Notes:
1. For read cycles 1 and 2, $\overline{WE}$ is high for the entire cycle.
2. The device is continuously selected with CE and $\overline{OE}$ low.
3. $\overline{WE}$ must be high when CE is low during the address sequence in order to initiate a nonvolatile cycle. $\overline{OE}$ may be either high or low throughout. Addresses A_1 through A_6 are found in the mode selection table. Address A_6 determines whether the device performs a STORE or RECALL.

Figure 4. Timing waveforms - continued.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class M, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in for device class M (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC standard number 17 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1,7,9	1,7,9
2	Static burn-in I and II (method 1015)	Not required	Not required	Required
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9, 10,11
7	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
8	Group C end-point electrical parameters	2,3,7, 8A,8B	1,2,3,7, 8A,8B Δ	1,2,3,7, 8A,8B,9, 10,11 Δ
9	Group D end-point electrical parameters	2,3, 8A,8B	2,3, 8A,8B	2,3, 8A,8B
10	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{CC4} standby	±10% value in table I
I_{IL}, I_{OL}	±10% value in table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table IIB herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device classes Q, and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

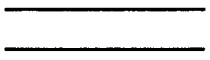
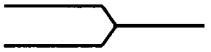
6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38535, MIL-STD-1331, and as follows:

C_{IN}	Input terminal capacitance.
C_{OUT}	Output terminal capacitance.
GND	Ground zero voltage potential.
I_{CC}	Supply current.
I_{IH}	Input high current.
I_{IL}	Input low current.
T_C	Case temperature.
T_A	Ambient temperature
V_{CC}	Ground zero voltage potential.
O/V	Latch-up over-voltage

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

APPENDIX

FUNCTIONAL ALGORITHMS

10. SCOPE

10.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. ALGORITHMS

30.1 Algorithm A (pattern 1).

30.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

30.2 Algorithm B (pattern 2).

30.2.1 March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

30.3 Algorithm C (pattern 3).

30.3.1 XY March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.

30.3.1 XY March - Continued.

Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

30.4 Algorithm D (pattern 4).

30.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.