Si5020 Micro PCB with S3050 Footprint

Features

- Supports substitution of the Si5020 in systems designed for AMCC S3050 footprint
- Simplifies evaluation of the Si5020 device
- DSPLL™ technology eliminates external loop filter components
- Excellent jitter generation performance: 3.0 mUIrms (typical)
- Low power consumption: 108 mA at OC-48 (typical)
- Wide supply voltage range: 3 to 6 V

Ordering Information:

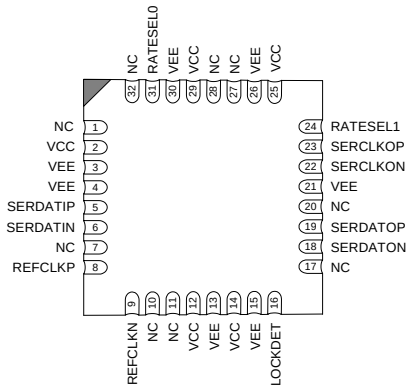
See page 11.

Applications

- Replacement for S3050
- In-system evaluation of the Si5020 SiPHY™ multi-rate SONET/SDH clock and data recovery IC

Pin Assignments

Si5020C-BA



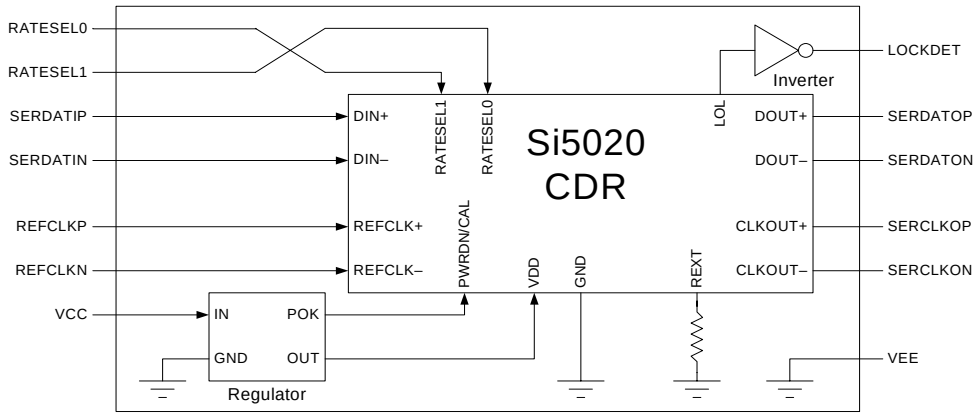
Top View

Description

The Si5020C-BA is a micro printed circuit board (PCB) that allows use of the Si5020 clock and data recovery (CDR) device in communications systems originally designed for the AMCC S3050. No system circuit board changes are necessary because the micro PCB is pin-compatible with the S3050.

The Si5020 device offers significant advantages in jitter performance, power dissipation, ease of use, and size over competing CDRs. The Si5020 incorporates Silicon Laboratories' DSPLL™ technology for improved performance and ease of use. DSPLL technology eliminates external loop filter components and their associated noise entry points, thus making the Si5020 CDR less susceptible to board-level interaction and helping to ensure optimal jitter performance.

Functional Block Diagram



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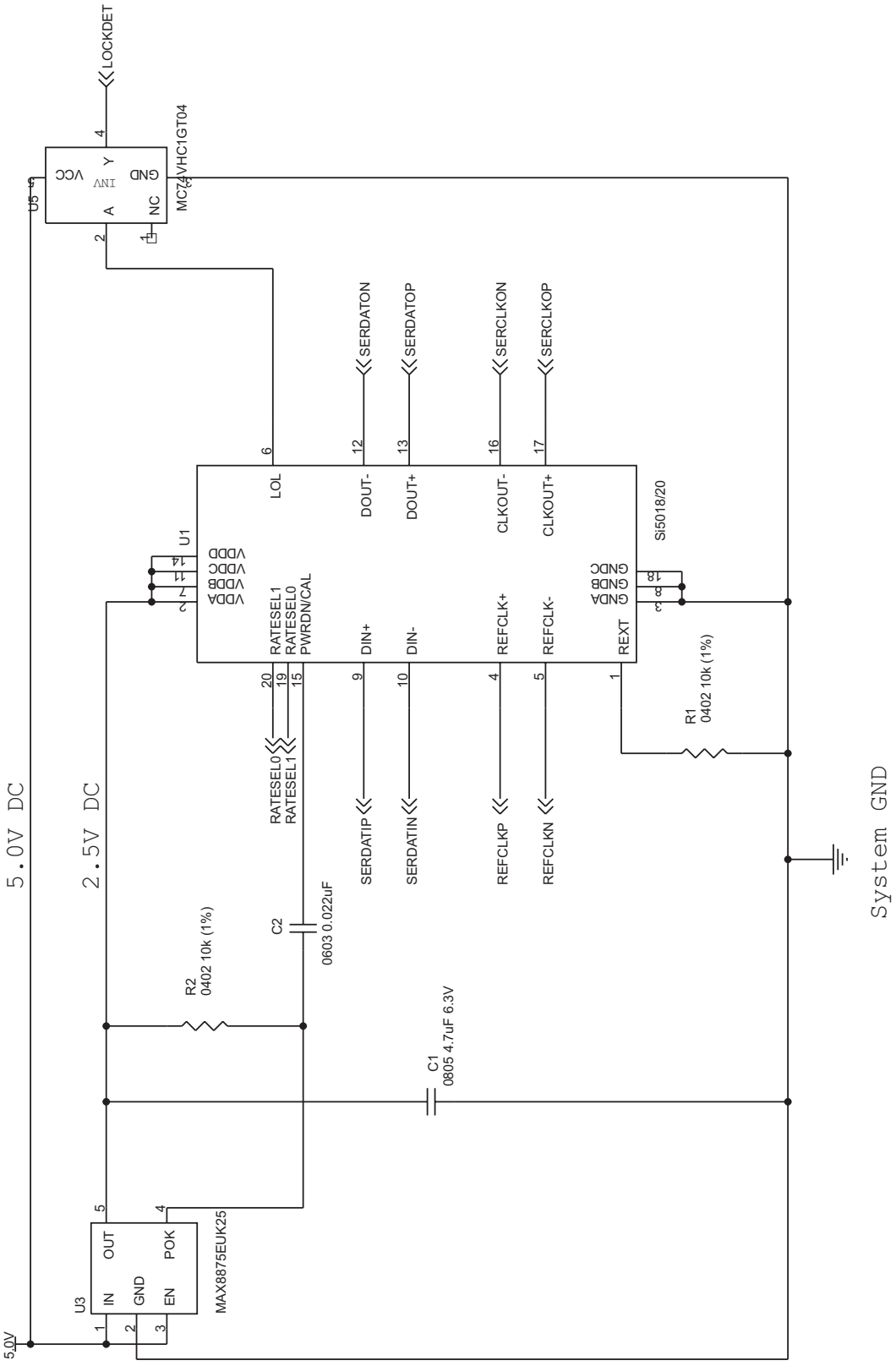
Si5020C-BA Schematic Diagram



Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min[1]	Typ	Max[1]	Unit
Ambient Temperature	T_A		–40	25	85	°C
Si5020C-BA Supply Voltage[2]	V_{CC}		3.0	5.0	6.0	V

Notes:
1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25°C unless otherwise stated.
2. The Si5020C-BA specifications are guaranteed when using the recommended application circuit (including component tolerance) of "Typical Application Schematic" on page 6.

Table 2. DC Characteristics

(V_{CC} = 5.0 V ±5%, T_A = –40 to 85 °C)

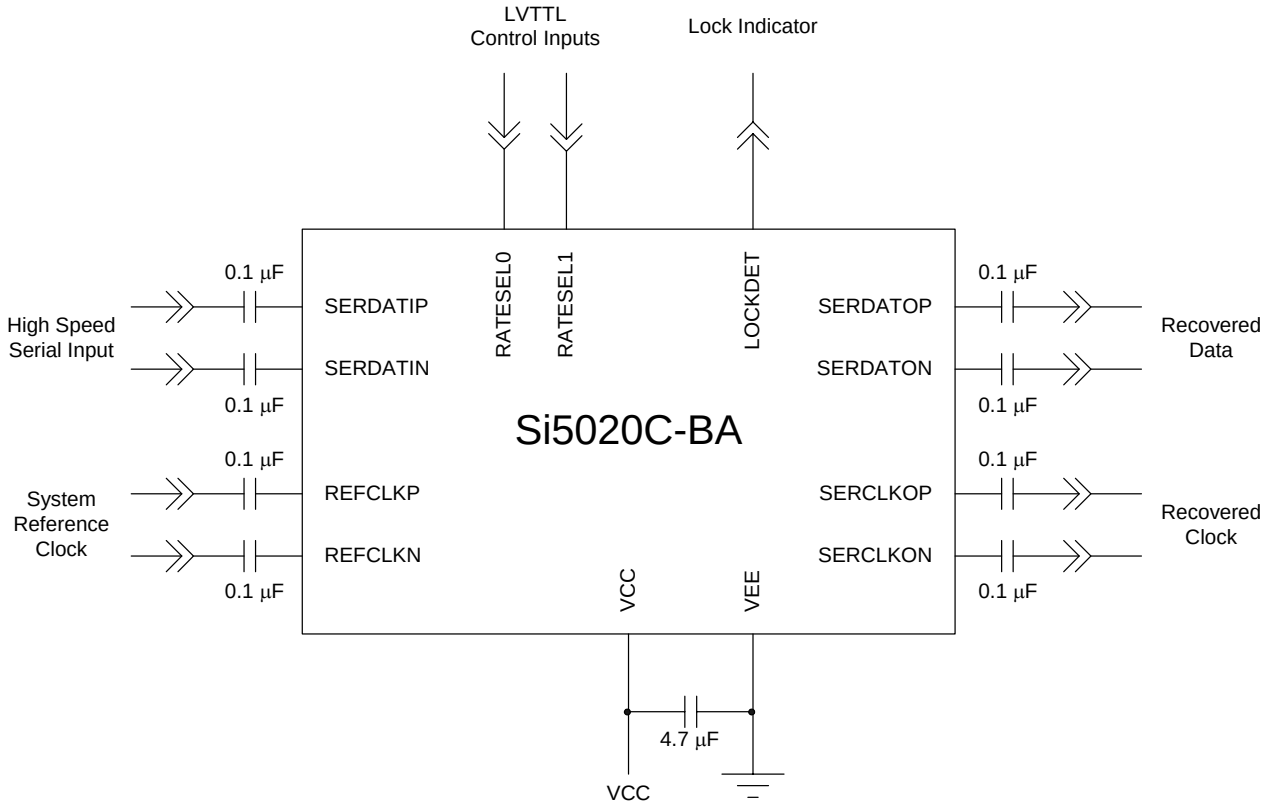
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current	I_{CC}					
OC-48			—	108	—	mA
GbE			—	113	—	
OC-12			—	117	—	
OC-3			—	124	—	
Power Dissipation						
OC-48			—	540	—	mW
GbE			—	566	—	
OC-12			—	586	—	
OC-3			—	620	—	

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	–0.5 to 7.0	V
LVTTL Input Voltage	V_{DIG}	–0.3 to 3.6	V
Storage Temperature Range	T_{STG}	–55 to 150	°C
Lead Temperature (soldering 10 s)		300	°C
ESD HBM Tolerance (100 pf, 1.5 kΩ)		1	kV

Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Typical Application Schematic



Functional Description

The Si5020C-BA is a micro PCB that adapts the Si5020 device to meet the footprint and essential functionality of the AMCC S3050 device. It allows substitution of the Si5020 device in systems designed for the S3050. The Si5020C-BA board is comprised of the Si5020 CDR device and support circuitry for voltage regulation, initiation of calibration, and lock detect signal polarity inversion. A schematic diagram for the Si5020C-BA is given in the "Si5020C-BA Schematic Diagram" on page 4.

Si5020 CDR Device

Please refer to the Si5020 data sheet for detailed operation and performance data for the Si5020 CDR device.

Voltage Regulator Circuit

To account for the power supply requirement differences between the S3050 and the Si5020, a low-dropout linear voltage regulator is used to regulate the Si5020C-BA board's 5 V supply input down to the 2.5 V supply used for the Si5020.

Generation of the PWRDN/CAL Signal

To achieve optimal jitter performance, the Si5020 device provides an internal self-calibration capability. Self-calibration optimizes loop gain parameters within the Si5020 DSPLL. Self-calibration is initiated by the falling edge of the Si5020 device PWRDN/CAL input signal. On the Si5020C-BA board, the Si5020 PWRDN/CAL signal is driven from the voltage regulator POK output signal through series capacitor C2. This circuit is identical to one described within Silicon Laboratories' application note AN42: "Controlling DSPLL™ Self-calibration for the Si5020/5018/5010 CDR Devices and Si531x Clock Multiplier/Regenerator Devices"

Rate Select Inputs

The RATESEL pins are used to set operating data rates for the Si5020C-BA. These pins set internal frequency dividers in the Si5020 device. The RATESEL pin settings for each data rate are given in Table 4

Table 4. Multi-Rate Configuration

RATESEL [1:0]	SONET/ SDH	Gigabit Ethernet	OC-48 w/ 15/14 FEC
00	2.488 Gbps	—	2.67 Gbps
10	1.244 Gbps	1.25 Gbps	—
01	622.08 Mbps	—	—
11	155.52 Mbps	—	—

Relative to the Si5020, the S3050 RATESEL pins are reversed such that RATESEL0 on the Si5020 corresponds to RATESEL1 on the S3050. This swapped mapping is handled on the Si5020C-BA such that the RATESEL inputs on the S3050-BA board match those of the S3050 device.

Lock Detect Output

Lock detection is performed by the Si5020 device. The LOL signal from the Si5020 device has an inverted polarity relative to that of the S3050. An inverting/level-shifting buffer is utilized on the Si5020C-BA to provide a TTL compatible LOCKDET output from the board that matches the S3050 output signal polarity. This signal will go high when the Si5020C-BA locks to the incoming serial data.

Reference Clock Input

The reference clock inputs (REFCLKP/N) provide coarse frequency information to the Si5020. This frequency information is used to identify the incoming serial data frequency and provide lock detection.

The supported frequencies for OC-48/12/3 are 155.52, 77.76, and 19.44 MHz. These frequencies are automatically detected within the Si5020 and no digital control inputs are required for clock frequency selection.

The REFCLKP/N inputs are internally biased to an input common mode voltage of 2.0 V and provide 100 Ω line-to-line termination. AC coupling is recommended as the simplest coupling approach. (See "Typical Application Schematic" on page 6.) Full details on the REFCLKP/N pins can be found in the Si5020 data sheet REFCLK± pin descriptions.

High-Speed Serial Input

The high-speed serial data inputs (SERDATIP/N) provide data to the Si5020 for clock and data recovery.

The SERDATIP/N inputs are internally biased to an input common mode voltage of 2.0 V and provide 100 Ω line-to-line termination. AC coupling is recommended as the simplest coupling approach. (See "Typical Application Schematic" on page 6.) Full details on the SERDATIP/N pins can be found in the Si5020 data sheet DIN± pin descriptions.

Recovered Data Output

The recovered data outputs (SERDATOP/N) transmit the recovered serial data. These outputs are time aligned to the recovered clock outputs.

The SERDATOP/N outputs are current mode logic (CML) outputs. AC coupling is recommended as the simplest coupling approach. (See "Typical Application Schematic" on page 6.) Full details on the SERDATOP/N pins can be found in the Si5020 data sheet DOUT± pin descriptions.

Recovered Clock Output

The recovered clock outputs (SERCLKOP/N) transmit the clock recovered from the serial data. These outputs are time aligned to the recovered data outputs.

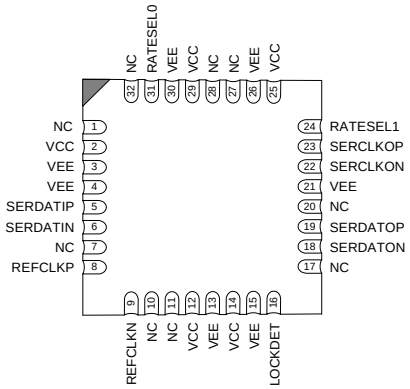
The SERCLKOP/N outputs are CML outputs. AC coupling is recommended as the simplest coupling approach. (See "Typical Application Schematic" on page 6.) Full details on the SERCLKOP/N pins can be found in the Si5020 data sheet CLKOUT± pin descriptions.

Soldering/Assembly

The Si5020C-BA employs a minimal lead length which is significantly different from a QFP lead. Despite the lead differences, handling of the Si5020C-BA is similar to handling of a QFP. Automation of the alignment and soldering processes will simplify the attachment. Alignment can be accomplished using standard pick-and-place machines. Set the pick point to the center of the Si5020 device; this point is marked within the mechanical drawing. (See Figure 2 on page 12.) Once aligned, soldering the Si5020C-BA to another PCB is best accomplished using solder paste and a reflow chamber. Once the Si5020C-BA is placed upon the solder paste the reflow process can occur.

The Si5020C-BA evaluation board itself has been assembled using 220 °C solder in order maintain the locations of the Si5020 device, voltage regulator, inverter, and passive components on the board during the reflow process.

Pin Descriptions: Si5020C-BA



Top View

Figure 1. Si5020C-BA Pin Configuration

Pin #	Pin Name	I/O	Signal Level	Description
1, 7, 10, 11, 17, 20, 27, 28, 32	NC			**No Connect.** These pins are not used by the Si5020C-BA board. The pins are not connected to circuitry on the board.
2, 12, 14, 25, 29	VCC		5 VDC	**Supply Voltage.** Nominally 5.0 VDC.
3, 4, 13, 15, 21, 26, 30	VEE		GND	**Supply Ground.** Nominally 0.0 VDC.
5, 6	SERDATIP, SERDATIN	I	*See note.	**Serial Data Input.** Equivalent to Si5020 DIN+ and DIN–, respectively.*
8, 9	REFCLKP, REFCLKN	I	*See note.	**Reference Clock Input.** Equivalent to Si5020 REFCLK+ and REFCLK–, respectively.*
16	LOCKDET	O	TTL	**Lock Detect Output.** Driven high when Si5020 is locked to serial data input signal. Driven low when out of lock. This signal is an inverted and level shifted version of the Si5020 LOL output.*
18, 19	SERDATON, SERDATOP	O	*See note.	**Serial Data Output.** Equivalent to Si5020 DOUT– and DOUT+, respectively.*
22, 23	SERCLKON, SERCLKOP	O	*See note.	**Serial Clock Output.** Equivalent to Si5020 CLKOUT– and CLKOUT+, respectively.*

Pin #	Pin Name	I/O	Signal Level	Description
24	RATESEL1	I	LVTTL	**Rate Select 1.** Equivalent to Si5020 RATESEL0 input. The RATESEL0 and RATESEL1 pins on the Si5020C-BA board are swapped with respect to those on the Si5020 device.*
31	RATESEL0	I	LVTTL	**Rate Select 0.** Equivalent to Si5020 RATESEL1 input. The RATESEL0 and RATESEL1 pins on the Si5020C-BA board are swapped with respect to those on the Si5020 device.*
***Note:** Refer to the Si5020 data sheet for details.				

Ordering Guide

Table 5. Ordering Guide

Part Number	Package	Temperature
Si5020C-BA	See Package Outline	–40 to 85 °C

Package Outline: Si5020C-BA

Figure 2 illustrates the package details for the Si5020C-BA. Table 6 lists the values for the dimensions shown in the illustration.

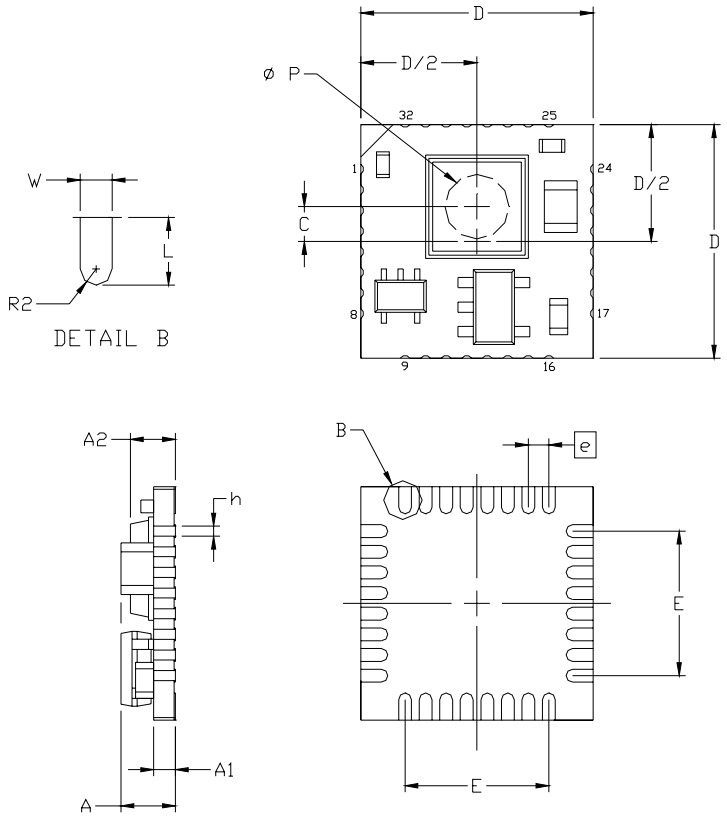


Figure 2. Si5020C-BA Mechanical Drawing

Table 6. Package Diagram Dimensions (mm)

Dimension	Description	Minimum	Nominal	Maximum
A	Total Card Height	1.97	2.12	2.27
A1	Card Thickness	0.80	0.85	0.90
A2	Height to Pick Point	1.65	1.75	1.85
C	Offset to Pick Point	1.32	1.35	1.38
D	Body Size	8.95	9.05	9.15
e	Pad Pitch		0.80 BSC.	
E	Total Pad Pitch		5.60 REF.	
h	Castellation Width	0.34	0.39	0.44
L	Pad Length	1.10	1.20	1.30
P	Diameter of Pick Area	—	3.50	—
R2	Pad Radius	0.23	0.25	0.27
W	Pad Width	0.45	0.50	0.55

Document Change List

Revision 0.81 to Revision 0.9

- Removed all references to Si5020-BA.
- Changed reference of in-system evaluation board to micro PCB.
- Front Page:
  - Micro PCB graphic updated.
  - Pin assignment drawing updated.
  - Features, Applications, and Description sections updated.
- "Functional Description" on page 7 updated.
- "Voltage Regulator Circuit" on page 7 updated.

Revision 0.90 to Revision 1.0

- Updated "Package Outline: Si5020C-BA" on page 12.

Contact Information

Silicon Laboratories Inc.

4635 Boston Lane
Austin, TX 78735
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Email: productinfo@silabs.com
Internet: www.silabs.com