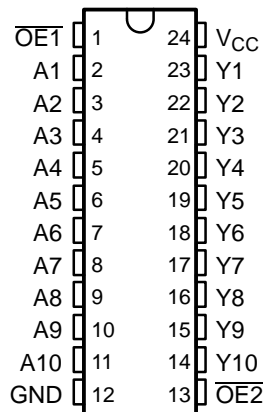


## FEATURES

- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 6.7 ns at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  
 $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  
 $>2$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

DB, DGV, DW, NS, OR PW PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

This 10-bit buffer/bus driver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74LVC827A provides a high-performance bus interface for wide data paths or buses carrying parity.

The 3-state control gate is a 2-input AND gate with active-low inputs so that, if either output-enable ( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all ten outputs are in the high-impedance state. The SN74LVC827A provides true data at its outputs.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## ORDERING INFORMATION

$T_A$	PACKAGE (1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – DW	Tube of 25	SN74LVC827ADW	LVC827A
		Reel of 2000	SN74LVC827ADWR	
	SOP – NS	Reel of 2000	SN74LVC827ANSR	LVC827A
	SSOP – DB	Reel of 2000	SN74LVC827ADBR	LC827A
	TSSOP – PW	Tube of 60	SN74LVC827APW	LC827A
		Reel of 2000	SN74LVC827APWR	
		Reel of 250	SN74LVC827APWT	
	TVSOP – DGV	Reel of 2000	SN74LVC827ADGVR	LC827A

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# SN74LVC827A 10-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

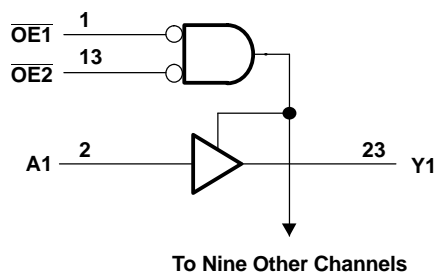
SG-AS396J—MARCH 1993—REVISED FEBRUARY 2005

[查询"SN74LVC827A"供应商](#)

**FUNCTION TABLE**

INPUTS			OUTPUT Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

**LOGIC DIAGRAM (POSITIVE LOGIC)**



## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	−0.5	6.5	V
$V_I$	Input voltage range <sup>(2)</sup>	−0.5	6.5	V
$V_O$	Voltage range, applied to any output in the high-impedance or power-off state <sup>(2)</sup>	−0.5	6.5	V
$V_O$	Voltage range, applied to any output in the high or low state <sup>(2)(3)</sup>	−0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$		−50 mA
$I_{OK}$	Output clamp current	$V_O < 0$		−50 mA
$I_O$	Continuous output current		±50	mA
	Continuous current through $V_{CC}$ or GND		±100	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DB package	63	°C/W
		DGV package	86	
		DW package	46	
		NS package	65	
		PW package	88	
$T_{stg}$	Storage temperature range	−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of  $V_{CC}$  is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	Operating	1.65	3.6
		Data retention only	1.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2	
$V_{IL}$	Low-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0.7	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	0.8	
$V_I$	Input voltage	0	5.5	V
$V_O$	Output voltage	High or low state	0	$V_{CC}$
		3-state	0	5.5
$I_{OH}$	High-level output current	$V_{CC} = 1.65 \text{ V}$	−4	mA
		$V_{CC} = 2.3 \text{ V}$	−8	
		$V_{CC} = 2.7 \text{ V}$	−12	
		$V_{CC} = 3 \text{ V}$	−24	
$I_{OL}$	Low-level output current	$V_{CC} = 1.65 \text{ V}$	4	mA
		$V_{CC} = 2.3 \text{ V}$	8	
		$V_{CC} = 2.7 \text{ V}$	12	
		$V_{CC} = 3 \text{ V}$	24	
$\Delta t/\Delta v$	Input transition rise or fall rate		10	ns/V
$T_A$	Operating free-air temperature	−40	85	°C

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN74LVC827A

## 10-BIT BUFFER/DRIVER

### WITH 3-STATE OUTPUTS

SCAS396J – MARCH 1993 – REVISED FEBRUARY 2005

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OH</sub>			I <sub>OH</sub> = −100 μA	1.65 V to 3.6 V	V <sub>CC</sub> − 0.2			V
			I <sub>OH</sub> = −4 mA	1.65 V	1.2			
			I <sub>OH</sub> = −8 mA	2.3 V	1.7			
			I <sub>OH</sub> = −12 mA	2.7 V	2.2			
				3 V	2.4			
			I <sub>OH</sub> = −24 mA	3 V	2.2			
V <sub>OL</sub>			I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V	0.2			V
			I <sub>OL</sub> = 4 mA	1.65 V	0.45			
			I <sub>OL</sub> = 8 mA	2.3 V	0.7			
			I <sub>OL</sub> = 12 mA	2.7 V	0.4			
			I <sub>OL</sub> = 24 mA	3 V	0.55			
I <sub>I</sub>		V <sub>I</sub> = 0 to 5.5 V		3.6 V			±5	μA
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 5.5 V		0			±10	μA
I <sub>OZ</sub>		V <sub>O</sub> = 0 to 5.5 V		3.6 V			±10	μA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND		3.6 V			10	μA
		3.6 V ≤ V <sub>I</sub> ≤ 5.5 V <sup>(2)</sup>					10	
ΔI <sub>CC</sub>		One input at V <sub>CC</sub> − 0.6 V,    Other inputs at V <sub>CC</sub> or GND		2.7 V to 3.6 V			500	μA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND		3.3 V			5	pF
	Data inputs						4	
C <sub>O</sub>		V <sub>O</sub> = V <sub>CC</sub> or GND		3.3 V			7	pF

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

(2) This applies in the disabled state only.

## Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	(1)	(1)	(1)	(1)	7.1		1	6.7	ns
t <sub>en</sub>	$\overline{\text{OE}}$	Y	(1)	(1)	(1)	(1)	8.5		1	7.3	ns
t <sub>dis</sub>	$\overline{\text{OE}}$	Y	(1)	(1)	(1)	(1)	7.3		1.8	6.7	ns
t <sub>sk(o)</sub>									1		ns

(1) This information was not available at the time of publication.

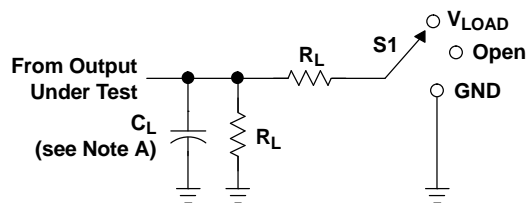
## Operating Characteristics

T<sub>A</sub> = 25°C

PARAMETER			TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	UNIT
				TYP	TYP	TYP	
C <sub>pd</sub>	Power dissipation capacitance per buffer/driver	Outputs enabled	f = 10 MHz	(1)	(1)	24	pF
		Outputs disabled		(1)	(1)	5	

(1) This information was not available at the time of publication.

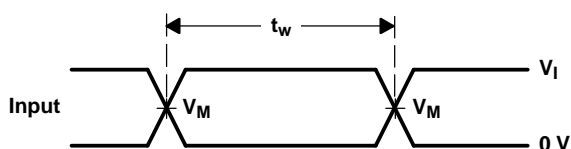
## PARAMETER MEASUREMENT INFORMATION



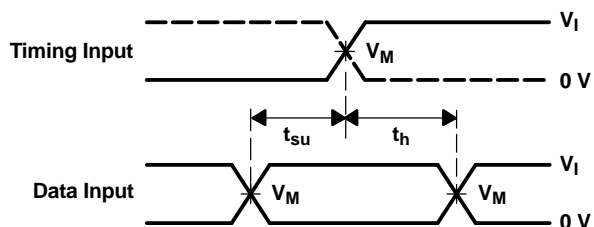
LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

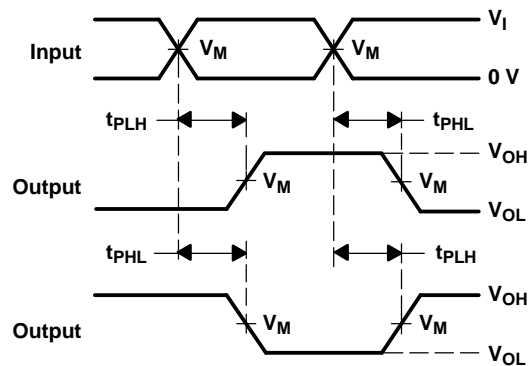
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



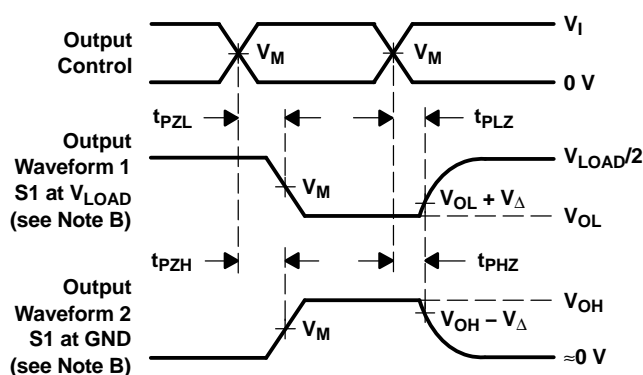
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LVC827ADBLE	OBSOLETE	SSOP	DB	24		TBD	Call TI	Call TI
SN74LVC827ADBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC827ADBRE4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC827ADGVR	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC827ADGVRE4	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC827ADW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC827ADWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC827ADWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC827ADWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC827ANSR	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC827ANSRE4	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC827APW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC827APWE4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC827APWLE	OBSOLETE	TSSOP	PW	24		TBD	Call TI	Call TI
SN74LVC827APWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC827APWRE4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC827APWT	ACTIVE	TSSOP	PW	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC827APWTE4	ACTIVE	TSSOP	PW	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

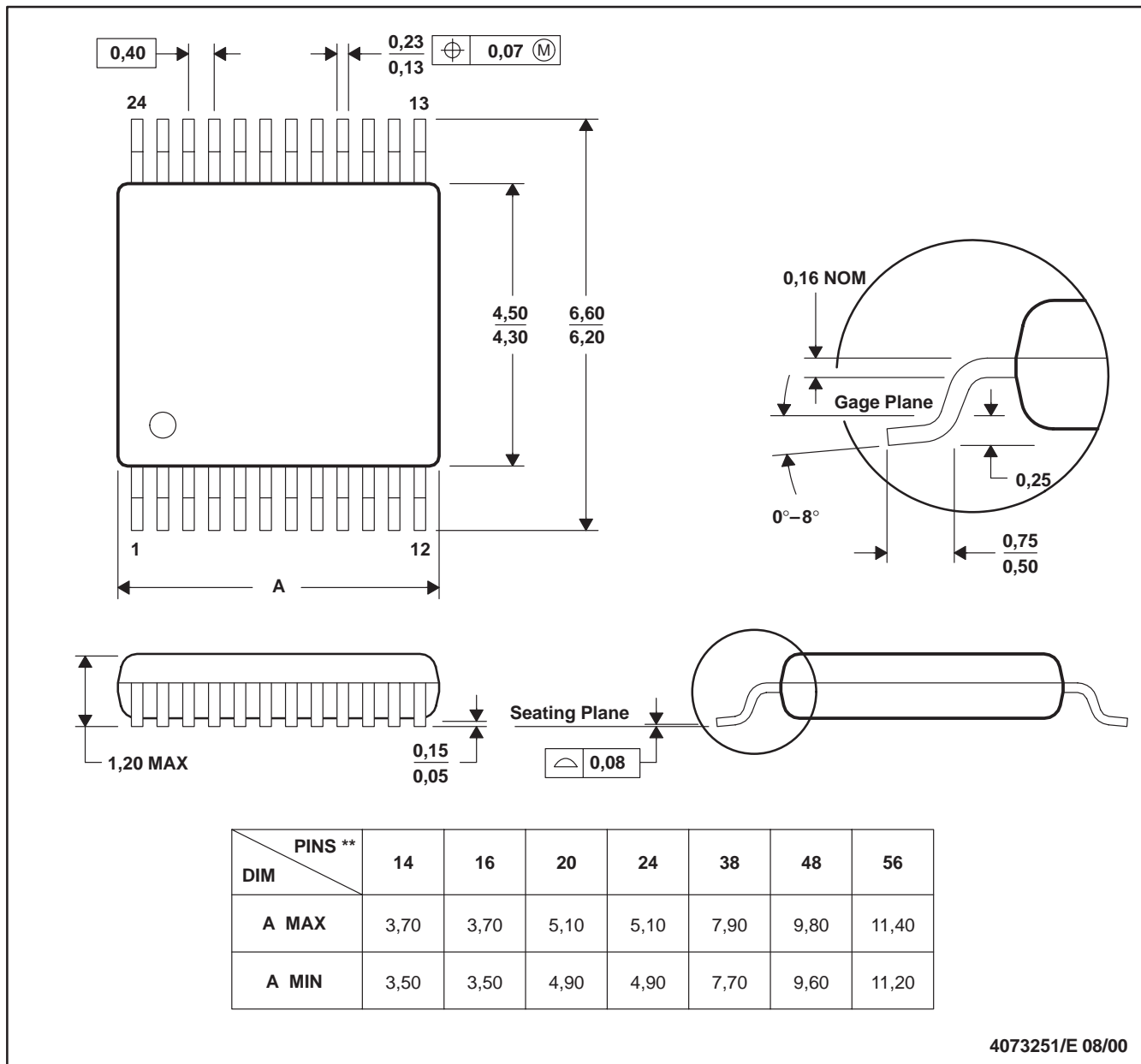
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DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

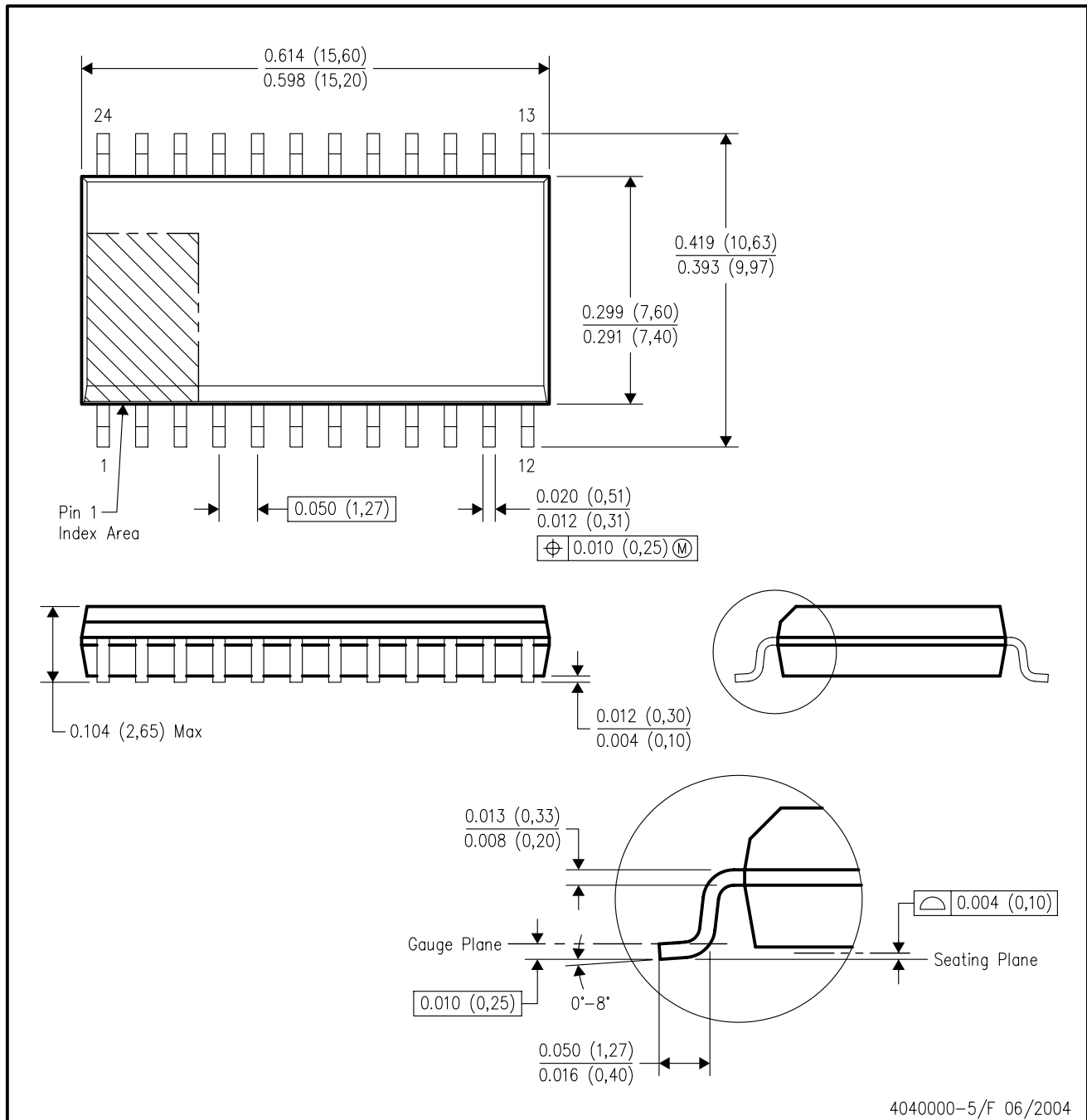


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194



## DW (R-PDSO-G24)

## PLASTIC SMALL-OUTLINE PACKAGE

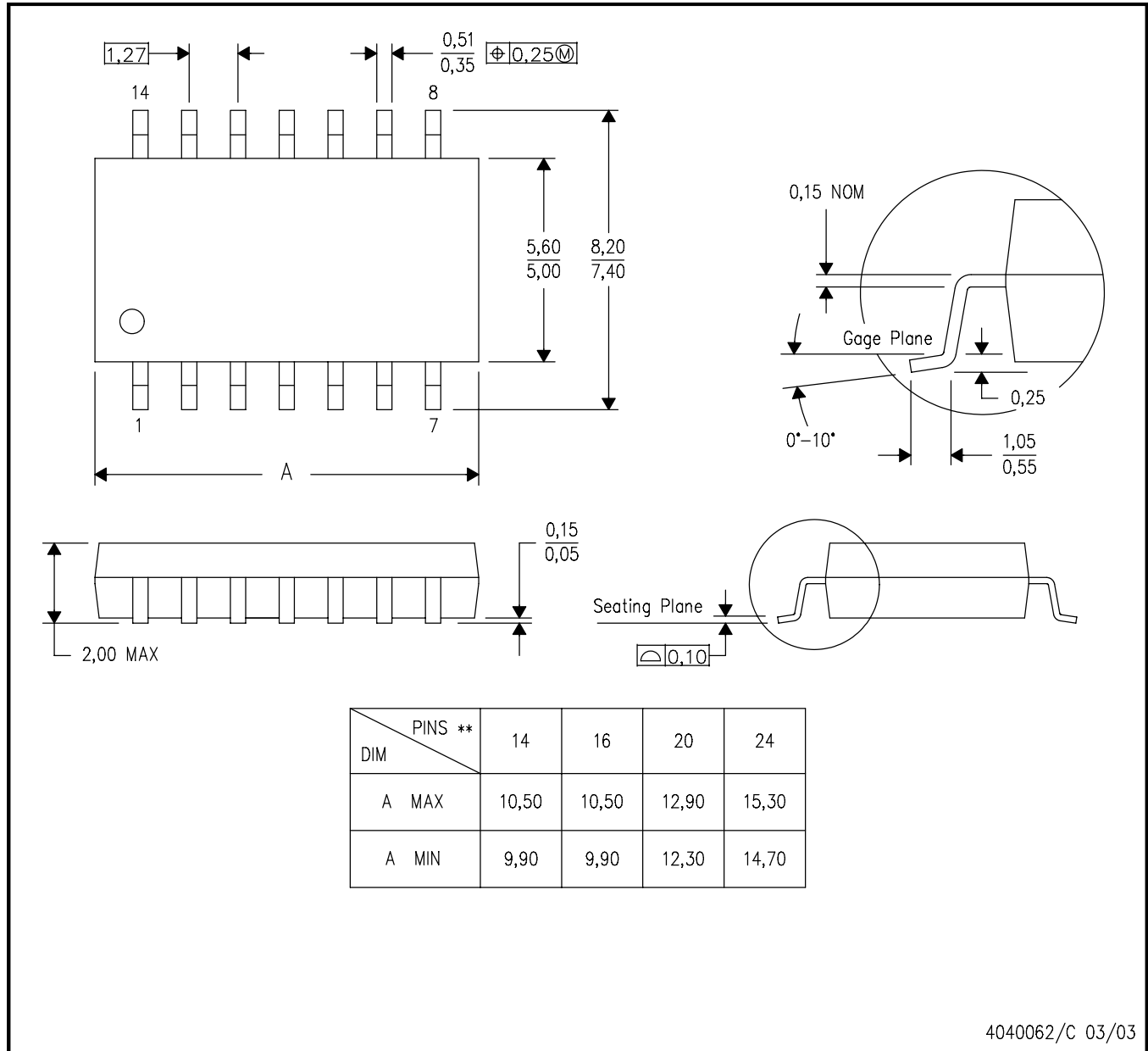


# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

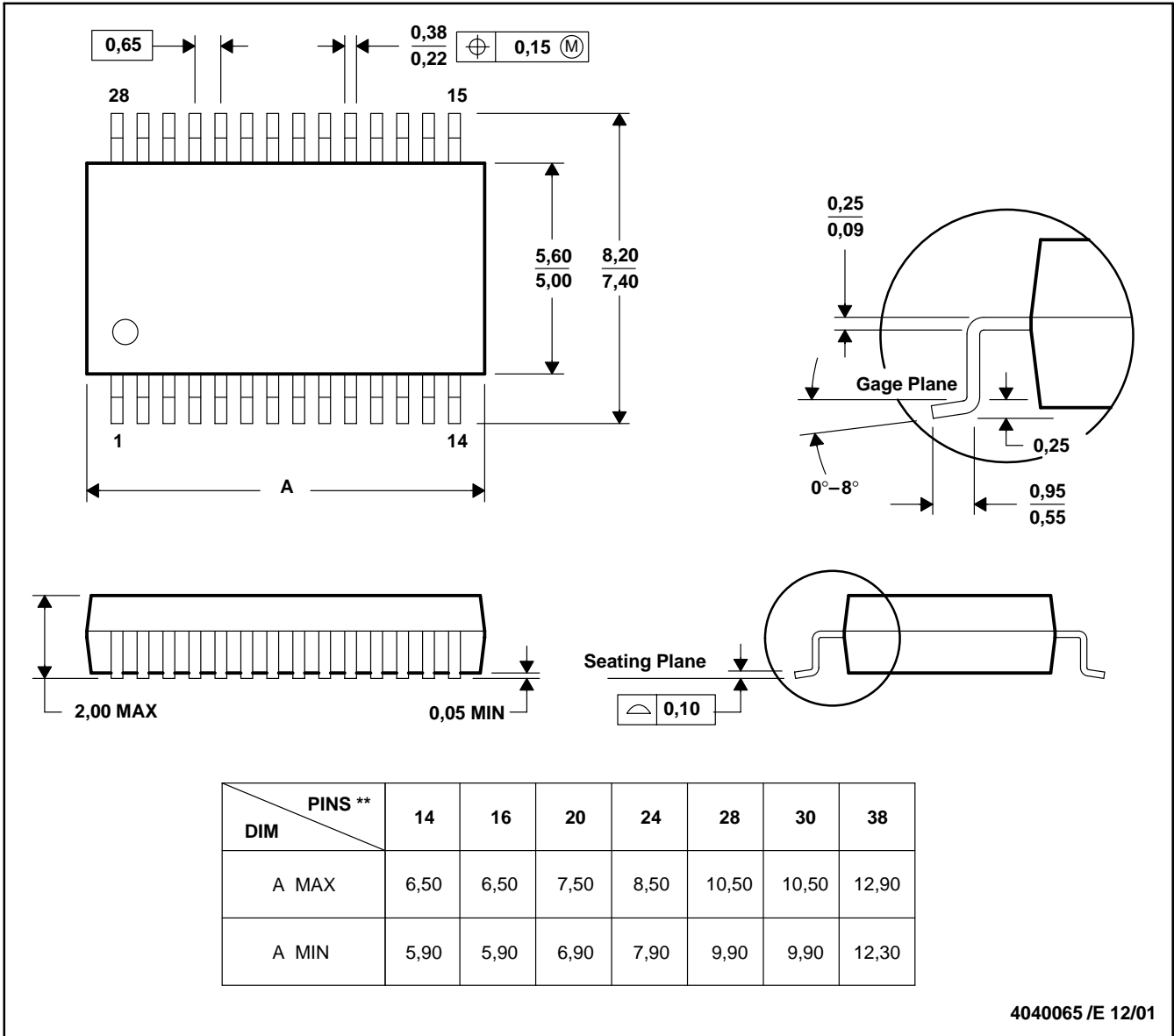


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
D. Falls within JEDEC MO-150

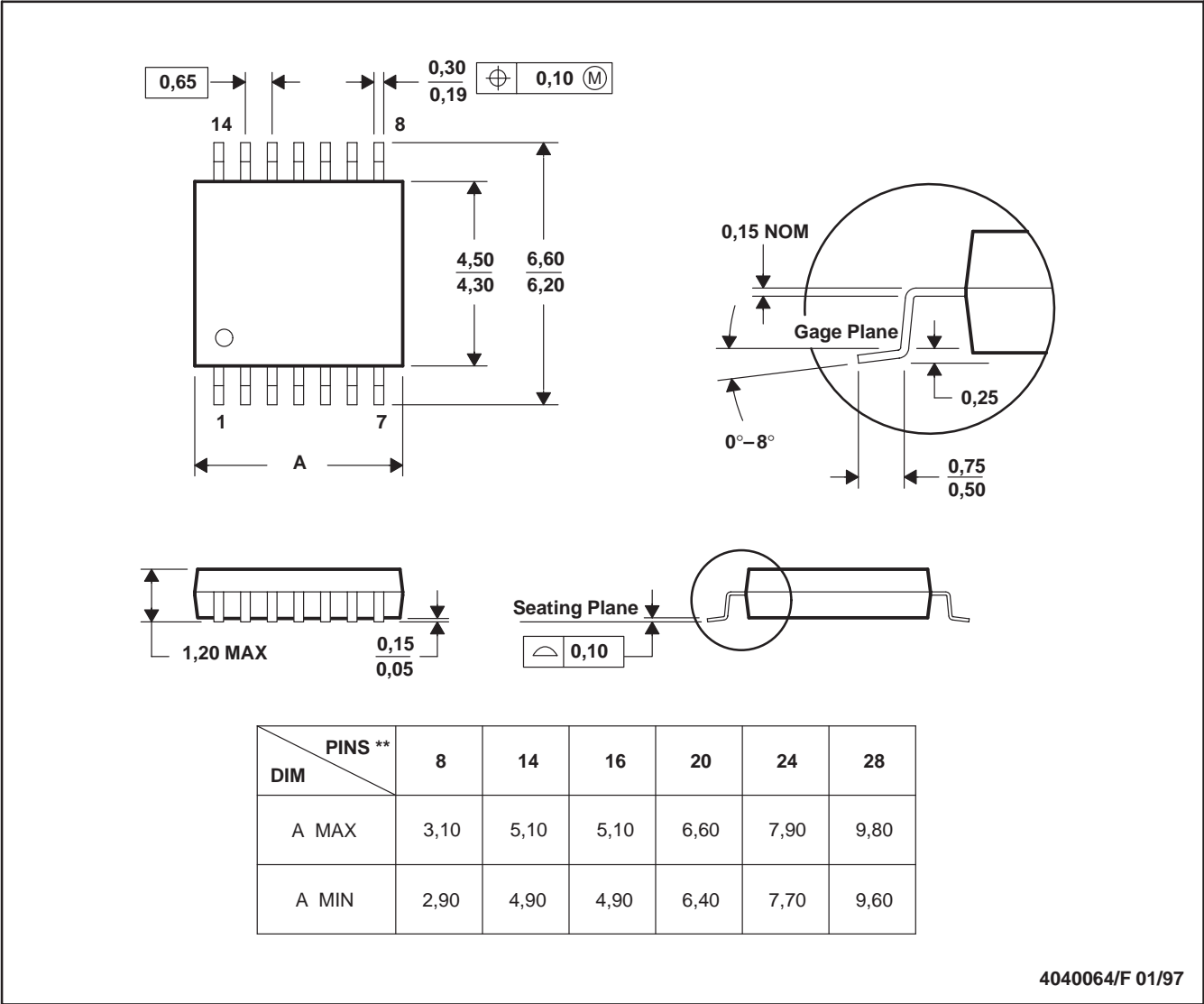
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MTSS001C – JANUARY 1995 – REVISED FEBRUARY 1999

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
D. Falls within JEDEC MO-153

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