9-CHANNEL RS-422 / RS-485 TRANSCEIVER

FEATURES

- **Designed to Operate at up to 20 Million Data Transfers per Second on Each RS-422/RS-485 Channel**
- **SN65HVD09 Packaged in Thin Shrink Small-Outline Package with 0.5-mm Pin Pitch**
- **ESD Protection on Bus Pins Exceeds 12kV**
- **Low Disabled Supply Current 8 mA Typ**
- **Thermal Shutdown Protection**
- **Positive- and Negative-Current Limiting**
- **Power-Up/Down Glitch Protection**

DESCRIPTION

The SN65HVD09 is a 9-channel RS-422 / RS-485 transceiver suitable for industrial applications. It offers improved switching performance, a small package, and high ESD protection. The precise skew limits ensures that the propagation delay times, not only from channel-to-channel but from device-to-device, are closely matched for the tight skew budgets associated with high-speed parallel data buses.

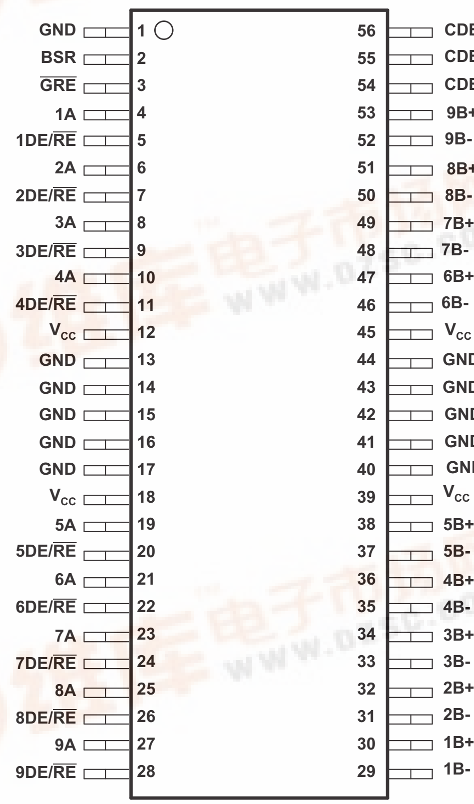
Patented thermal enhancements are used in the thin shrink, small-outline package (TSSOP), allowing operation over the industrial temperature range. The TSSOP package offers very small board area requirements while reducing the package height to 1 mm. This provides more board area and allows component mounting to both sides of the printed circuit boards for low-profile, space-restricted applications such as small form-factor hard disk drives.

The HVD09 can withstand electrostatic discharges exceeding 12 kV using the human-body model, and 600 V using the machine model on the RS-485 I/O terminals. This provides protection from the noise that can be coupled into external cables. The other terminals of the device can withstand discharges exceeding 4 kV and 400 V respectively.

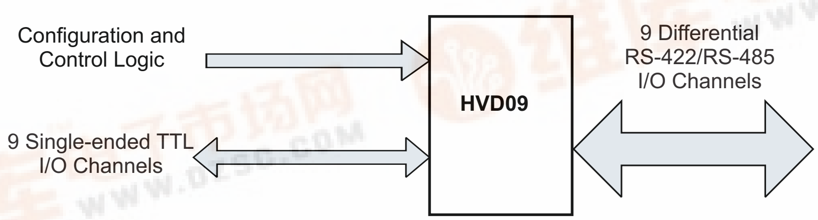
Each of the nine half-duplex channels of the HVD09 is designed to operate with either RS-422 or RS-485 communication networks.

The SN65HVD09 is characterized for operation over an ambient air temperature range of –40°C to 85°C.

SN65HVD09 DGG
(TOP VIEW)



Terminals 13 through 17, and 40 through 44 are connected together to the package lead frame and signal ground.



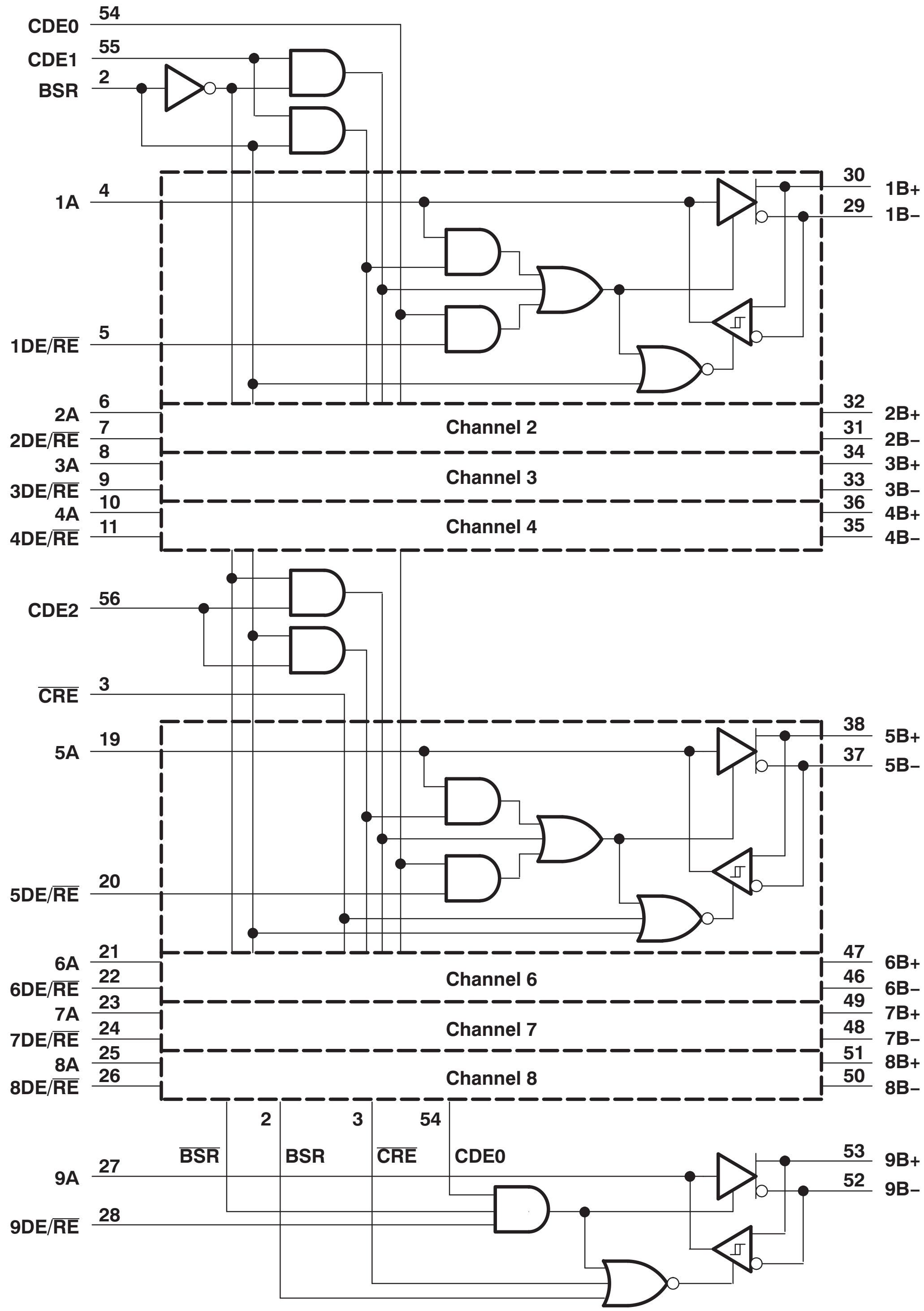
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PIN FUNCTIONS

PIN		LOGIC LEVEL	I/O	TERMINATION	DESCRIPTION
NAME	NO.				
1A to 9A	4,6,8,10, 19,21,23, 25,27	TTL	I/O	Pullup	1A to 9A carry data to and from the communication controller.
1B– to 9B–	29,31,33, 35,37,.46 , 48,50,52	RS-485	I/O	Pulldown	1B– to 9B– are the inverted data signals of the balanced pair to/from the bus.
1B+ to 9B+	30,32,34, 36,38,47, 49,51,53	RS-485	I/O	Pullup	1B+ to 9B+ are the noninverted data signals of the balanced pair to/from the bus.
BSR	2	TTL	Input	Pullup	BSR is the bit significant response. BSR disables receivers 1 through 8 and enables wired-OR drivers when BSR and DE/$\overline{RE}$ and CDE1 or CDE2 are high. Channel 9 is placed in a high-impedance state with BSR high.
CDE0	54	TTL	Input	Pulldown	CDE0 is the common driver enable 0. Its input signal enables all drivers when CDE0 and 1DE/$\overline{RE}$ – 9DE/$\overline{RE}$ are high.
CDE1	55	TTL	Input	Pulldown	CDE1 is the common driver enable 1. Its input signal enables drivers 1 to 4 when CDE1 is high and BSR is low.
CDE2	56	TTL	Input	Pulldown	CDE2 is the common driver enable 2. When CDE2 is high and BSR is low, drivers 5 to 8 are enabled.
$\overline{CRE}$	3	TTL	Input	Pullup	$\overline{CRE}$ is the common receiver enable. When high, CRE disables receiver channels 5 to 9.
1DE/$\overline{RE}$ to 9DE/$\overline{RE}$	5,7,9,11, 20,22,24, 26,28	TTL	Input	Pullup	1DE/$\overline{RE}$–9DE/$\overline{RE}$ are direction controls that transmit data to the bus when it and CDE0 are high. Data is received from the bus when 1DE/$\overline{RE}$–9DE/$\overline{RE}$ and CRE and BSR are low and CDE1 and CDE2 are low.
GND	1,13,14, 15,16,17, 40,41,42, 43,44	NA	Power	NA	GND is the circuit ground. All GND terminals except terminal 1 are physically tied to the die pad for improved thermal conductivity.(1)
V_{CC}	12,18,39, 45	NA	Power	NA	Supply voltage

(1) Terminal 1 must be connected to signal ground for proper operation.

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS[1]

			VALUE	UNIT
V_{CC}	Supply voltage range[2]		–0.3 to 6	V
	Bus voltage range		–10 to 15	V
	Data I/O and control (A side) voltage range		–0.3 to V_{CC} +0.5	V
I_O	Receiver output current		±40	mA
	Electrostatic discharge	B side and GND, Class 3, A[3]	12	kV
		B side and GND, Class 3, B[3]	400	V
		All terminals, Class 3, A	4	kV
		All terminals, Class 3, B	400	V
	Continuous total power dissipation [4]		Internally Limited	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.r
(2) All voltage values are with respect to the GND terminals.
(3) This absolute maximum rating is tested in accordance with MIL-PRF-38535, Method 3015.7.
(4) The maximum operating junction temperature is internally limited. Use the Dissipation Rating Table to operate below this temperature.

DISSIPATION RATINGS

PACKAGE	TA ≤ 25°C	OPERATING FACTOR[1] ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DGG	2500 mW	20 mW/°C	1600 mW	1300 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

PACKAGE THERMAL CHARACTERISTICS

			MIN	NOM	MAX	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	DGG, board-mounted, no air flow		50		°C/W
θ_{JC}	Junction-to-case thermal resistance	DGG		27		°C/W
T_{SD}	Thermal shutdown temperature			165		°C

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	Except nB+, nB–[1]	2			V
V_{IL}	Low-level input voltage				0.8	V
V_O, V_I, or V_{IC}	Voltage at any bus terminal (separately or common-mode)	nB+ or nB–	–7		12	V
I_O	Output current	Driver	–60		60	mA
		Receiver	–8		8	mA
T_A	Ambient temperature	SN65HVD09	–40		85	°C

(1) n = 1 - 9

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			SN65HVD09			UNIT
					MIN	TYP[(1)]	MAX	
$\lvert V_{OD} \rvert$	Driver differential output voltage magnitude	RS-422 load,	R_L = 100 Ω	See Figure 1	1	1.6		V
		RS-485 load,	R_L = 54 Ω	See Figure 1		1.4		V
		Pull-Up Pull-Down Load		See Figure 2	1	1.5		V
V_{OH}	High-level output voltage	A side, I_{OH} = –8 mA, V_{ID} = 200 mV,		See Figure 4	4	4.5		V
		B side,		See Figure 2		3		V
V_{OL}	Low-level output voltage	A side, I_{OH} = 8 mA, V_{ID} = –200 mV,		See Figure 4		0.6	0.8	V
		B side,		See Figure 2		1		V
V_{IT+}	Receiver positive-going differential input threshold voltages	I_{OH} = –8 mA,		See Figure 4			0.2	V
V_{IT-}	Receiver negativegoing differential input threshold voltage	I_{OL} = 8 mA,		SeeFigure 4	–0.2			V
V_{hys}	Receiver input hysteresis ($V_{IT+} - V_{IT-}$)	V_{CC} = 5 V,	T_A = 25°C		24	45		mV
I_I	Bus input current	V_{IH} = 12 V	V_{CC} = 5 V,	Other input at 0 V			1	mA
		V_{IH} = 12 V	V_{CC} = 0,	Other input at 0 V			1	mA
		V_{IH} = –7 V	V_{CC} = 5 V,	Other input at 0 V	–0.8	–0.4		mA
		V_{IH} = –7 V	V_{CC} = 0,	Other input at 0 V	–0.8	–0.3		mA
I_{IH}	High-level input current	nA, BSR, DE/$\overline{RE}$, and $\overline{CRE}$,		V_{IH} = 2 V	–100			µA
		CDE0, CDE1, and CDE2,		V_{IH} = 2V			100	µA
I_{IL}	Low-level input current	nA, BSR, DE/$\overline{RE}$, and $\overline{CRE}$,		V_{IL} = 0.8 V	–100			µA
		CDE1, CDE1, and CDE2,		V_{IL} = 0.8 V			100	µA
I_{OS}	Short circuit output current	nB+ or nB–					±260	mA
I_{OZ}	High-impedance-state output current	nA				See I_{IH} and I_{IL}		
		nB+ or nB–				See I_{II}		
I_{CC}	Supply current	Disabled					10	mA
		All drivers enabled, no load					60	mA
		All receivers enabled, no load					45	mA
C_O	Output capacitance	nB+ or nB– to GND				18	25	pF
C_{pd}	Power dissipation capacitance [(2)]	Receiver				40		pF
		Driver				100		pF

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) C_{pd} determines the no-load dynamic supply current consumption, $I_S = C_{PD} \times V_{CC} \times f + I_{CC}$

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN65HVD09			UNIT
			MIN	TYP(1)	MAX	
t_{pd}	Propagation delay time, t_{PHL} or t_{PLH} (see Figure 2 and Figure 3)		2.5		13.5	ns
$t_{sk(p)}$	Pulse skew, $\|t_{PHL} – t_{PLH}\|$				4	ns
t_f	Fall time	S1 to B, See Figure 3		4		ns
t_r	Rise time	See Figure 3		8		ns
t_{en}	Enable time, control inputs to active output				50	ns
t_{dis}	Disable time, control inputs to high-impedance output				100	ns
t_{PHZ}	Propagation delay time, high-level to high-impedance output	See Figure 6 and Figure 7		17	100	ns
t_{PLZ}	Propagation delay time, low-level to high-impedance output			25	100	ns
t_{PZH}	Propagation delay time, high-impedance to high-level output			17	50	ns
t_{PZL}	Propagation delay time, high-impedance to low-level output			17	50	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN65HVD09			UNIT
			MIN	TYP(1)	MAX	
t_{pd}	Propagation delay time, t_{PHL} or t_{PLH} (see Figure 2 and Figure 3)		8.5		14.5	ns
$t_{sk(lim)}$	Skew limit, maximum t_{pd} – minimum t_{pd} (2)				5	ns
$t_{sk(p)}$	Pulse skew, $\|t_{PHL} – t_{PLH}\|$			0.6	4	ns
t_t	Transition time (t_r or t_f)	See Figure 5		2		ns
t_{en}	Enable time, control inputs to active output				50	ns
t_{dis}	Disable time, control inputs to high-impedance output				60	ns
t_{PHZ}	Propagation delay time, high-level to high-impedance output	See Figure 8 and Figure 9			60	ns
t_{PLZ}	Propagation delay time, low-level to high-impedance output				50	ns
t_{PZH}	Propagation delay time, high-impedance to high-level output				50	ns
t_{PZL}	Propagation delay time, high-impedance to low-level output				50	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) This parameter is applicable at one V_{CC} and operating temperature within the recommended operating conditions and to any two devices.

PARAMETER MEASUREMENT INFORMATION

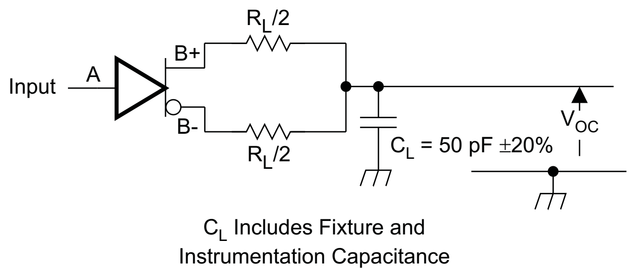
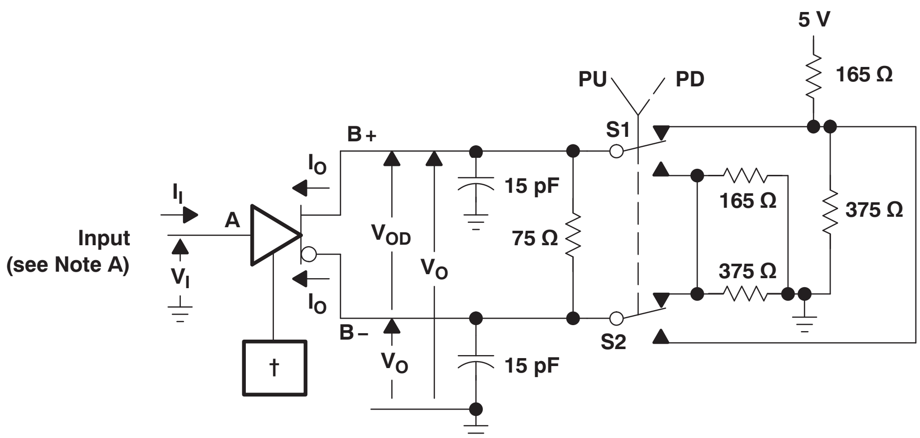


Figure 1. Driver Test Circuit, RS-422 and RS-485 Loading



† CDEO and DE/$\overline{RE}$ are at 2 V, BSR is at 0.8V, and all others are open.
‡ All nine drivers are enabled, similarly loaded, and switching.

Figure 2. Driver Test Circuit, Pull-Up and Pull-Down Loading‡

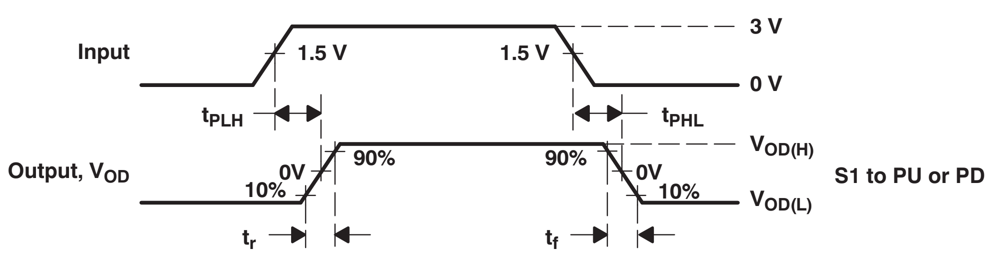
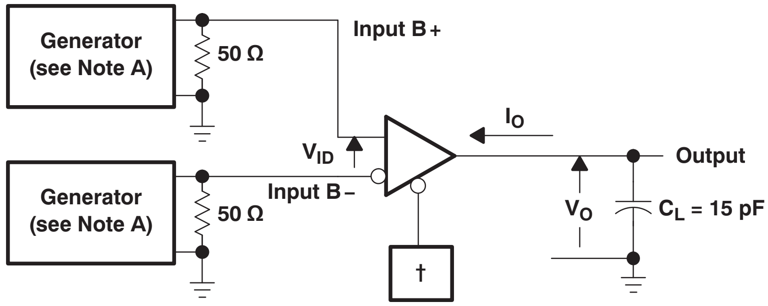


Figure 3. Driver Delay and Transition Time Test Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



† CDEO, CDE1, CDE2, BSR, CRE, and DE/RE at 0.8 V
‡ All nine receivers are enabled and switching.

Figure 4. Receiver Propagation Delay and Transition Time Test Circuit

A. All input pulses are supplied by a generator having the following characteristics: $t_r \le 6$ ns, $t_f \le 6$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50\ \Omega$.

B. All resistances are in Ω and ±5%, unless otherwise indicated.

C. All capacitances are in pF and ±10%, unless otherwise indicated.

D. All indicated voltages are ±10 mV.

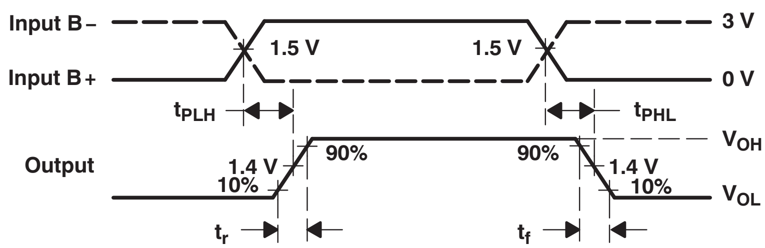
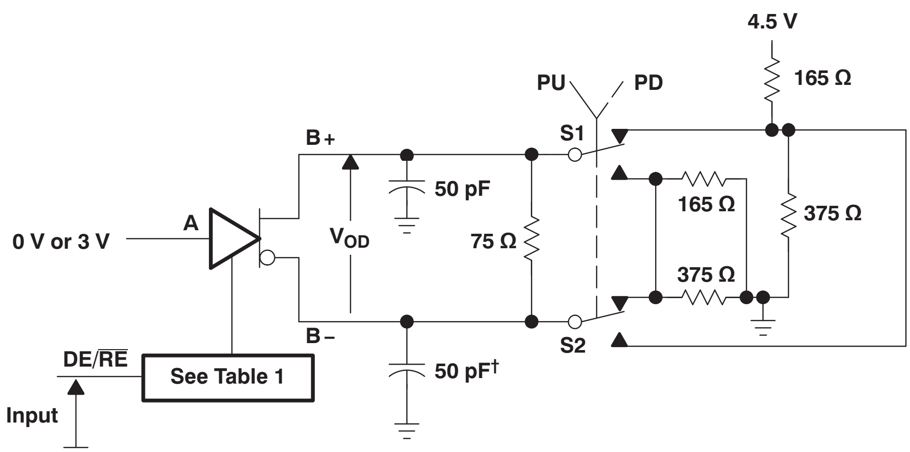


Figure 5. Receiver Delay and Transition Time Waveforms



† Includes probe and jig capacitance in two places.

Figure 6. Driver Enable and Disable Time Test Circuit

Table 1. Enabling for Driver Enable and Disable Time

DRIVER	BSR	CDE0	CDE1	CDE2	$\overline{CRE}$
1–8	H	H	L	L	X
9	L	H	H	H	H

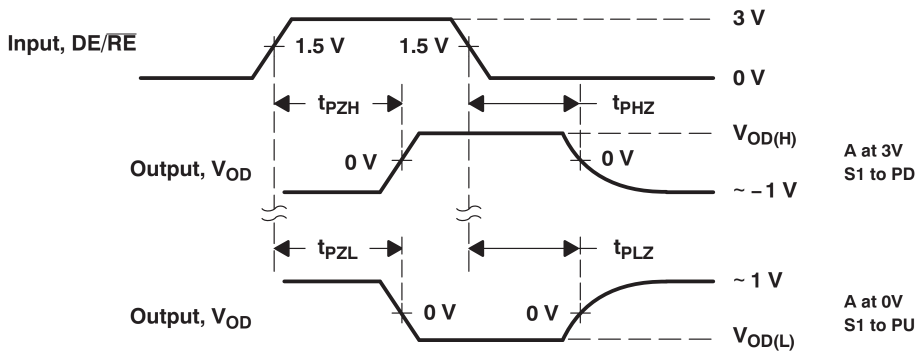


Figure 7. Driver Enable Time Waveforms

NOTES:
- A. All input pulses are supplied by a generator having the following characteristics: $t_r \leq 6$ ns, $t_f \leq 6$ ns, PRR ≤ 1 MHz, duty cycle = 50%, Z_O = 50 Ω.
- B. All resistances are in Ω and ±5%, unless otherwise indicated.
- C. All capacitances are in pF and ±10%, unless otherwise indicated.
- D. All indicated voltages are ±10 mV.

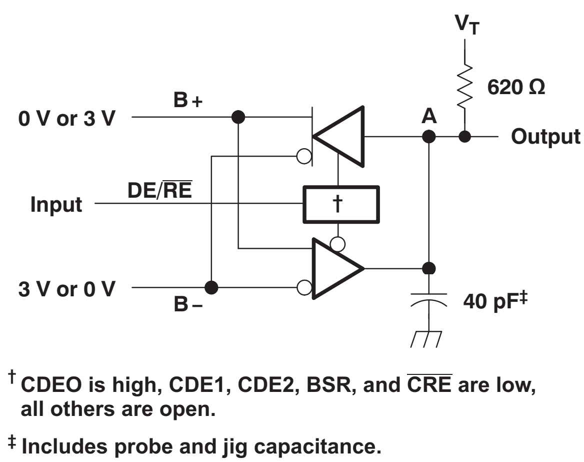


Figure 8. Receiver Enable and Disable Time Test Circuit

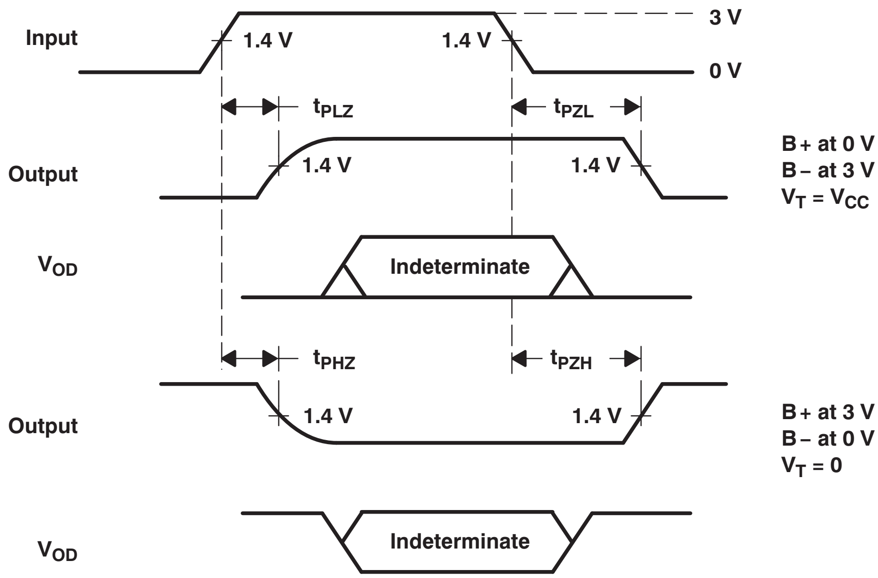


Figure 9. Receiver Enable and Disable Time Waveforms

NOTES:

A. All input pulses are supplied by a generator having the following characteristics: $t_r \le 6$ ns, $t_f \le 6$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50\ \Omega$.

B. All resistances are in Ω and ±5%, unless otherwise indicated.

C. All capacitances are in pF and ±10%, unless otherwise indicated.

D. All indicated voltages are ±10 mV.

TYPICAL CHARACTERISTICS

AVERAGE SUPPLY CURRENT
vs
FREQUENCY

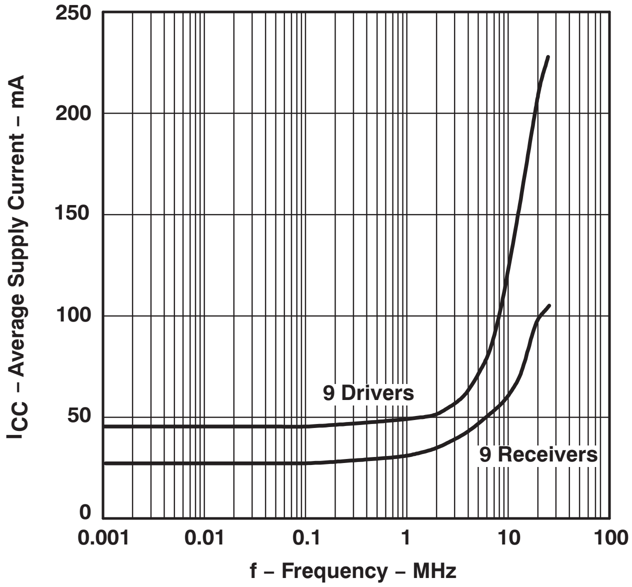


Figure 10.

LOGIC INPUT CURRENT
vs
INPUT VOLTAGE

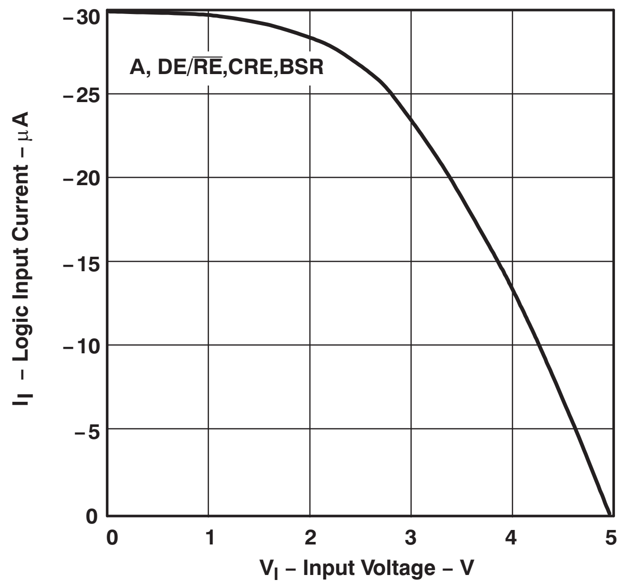


Figure 11.

BUS
INPUT CURRENT
vs
INPUT VOLTAGE

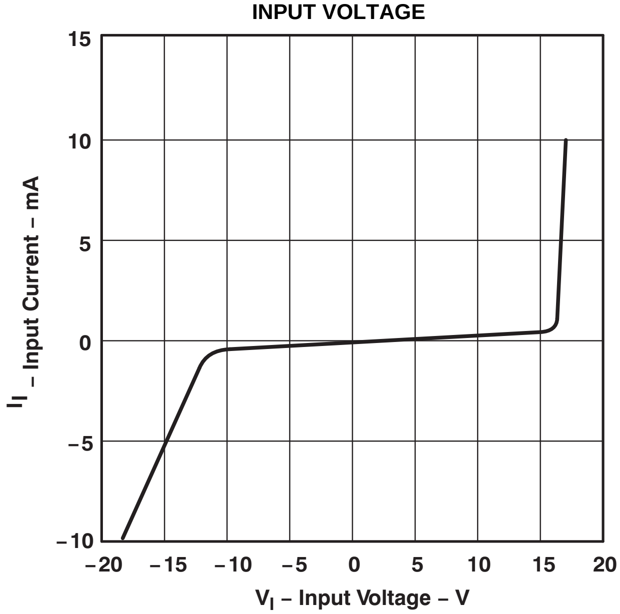


Figure 12.

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

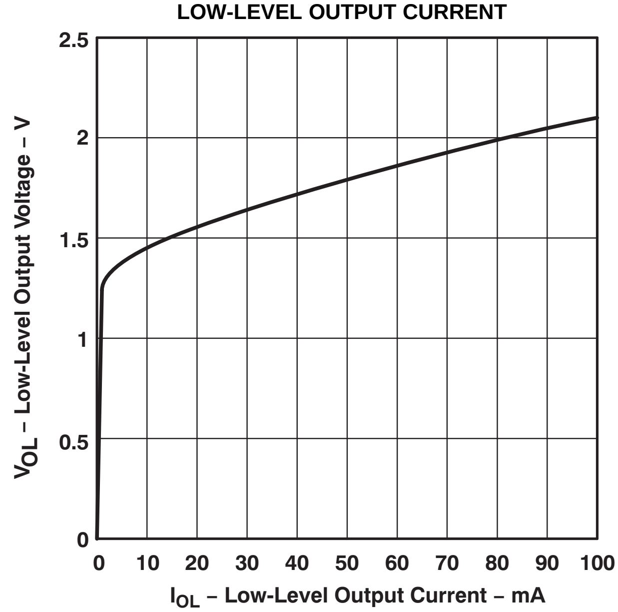


Figure 13.

TYPICAL CHARACTERISTICS (continued)

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

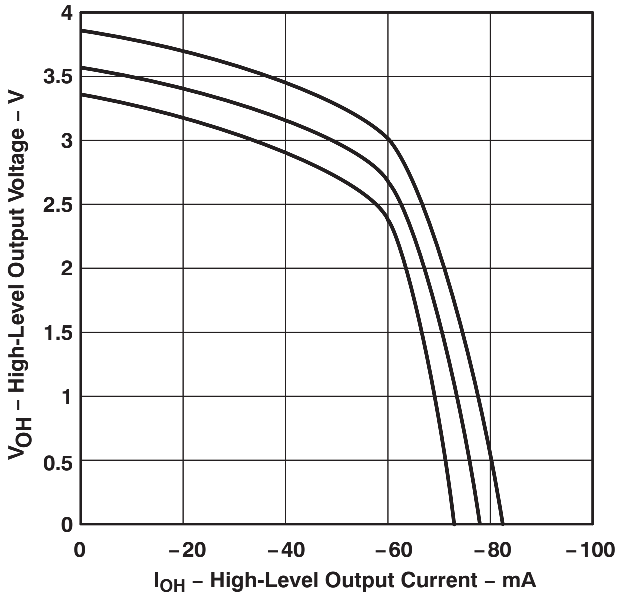


Figure 14.

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
TEMPERATURE

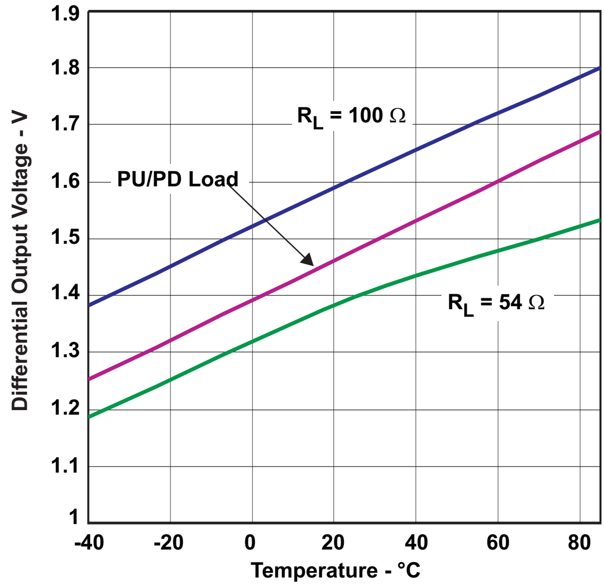


Figure 15.

RECEIVER
PROPAGATION DELAY TIME
vs
TEMPERATURE

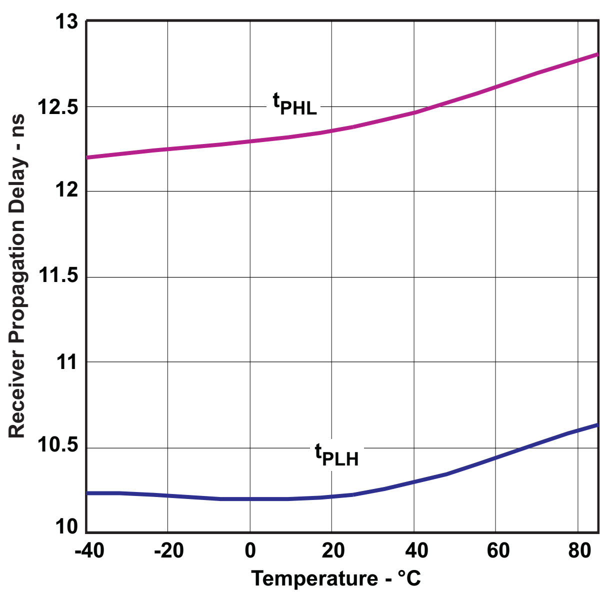


Figure 16.

DRIVER
PROPAGATION DELAY TIME
vs
TEMPERATURE

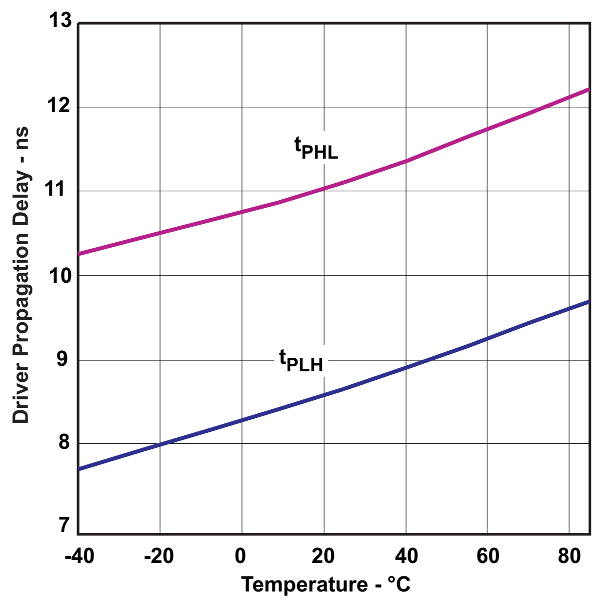


Figure 17.

TYPICAL CHARACTERISTICS (continued)

DRIVER
OUTPUT CURRENT
vs
SUPPLY VOLTAGE

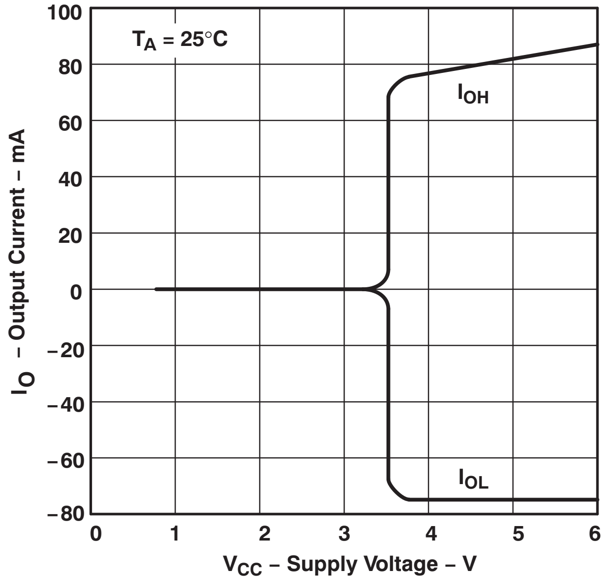
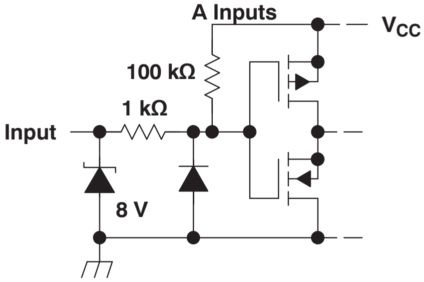


Figure 18.

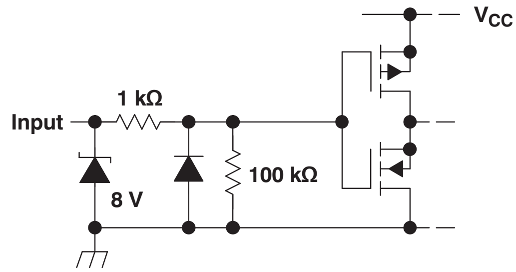
TYPICAL CHARACTERISTICS (continued)

SCHEMATICS OF INPUTS AND OUTPUTS

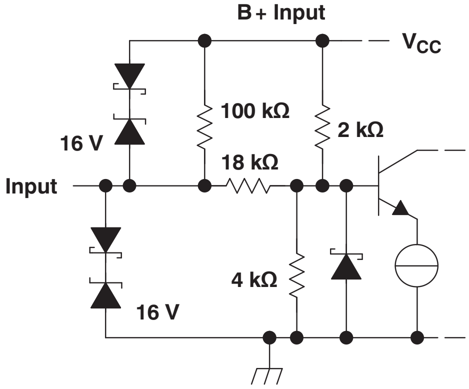
DE/$\overline{RE}$, $\overline{CRE}$, BSR, AND A Inputs



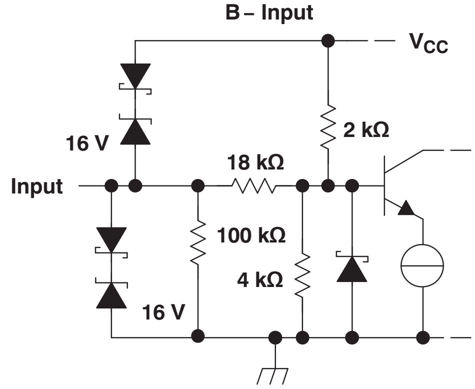
CDE0, CDE1, AND CDE2 Inputs



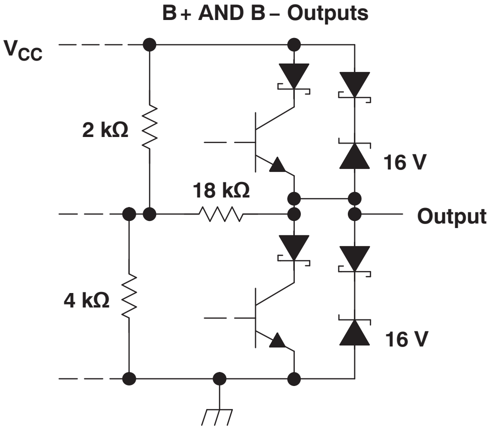
B+ Input



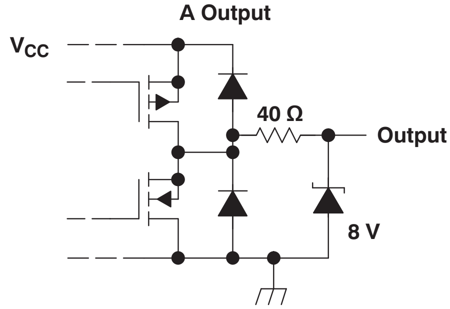
B– Input



B+ AND B– Outputs



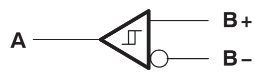
A Output



APPLICATION INFORMATION

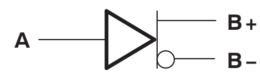
FUNCTION TABLES

RECEIVER



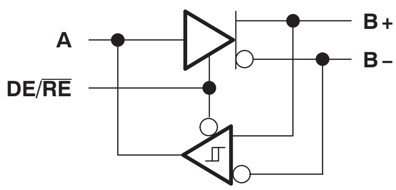
INPUTS		OUTPUT
B+[1]	B–[1]	A
L	H	L
H	L	H

DRIVER



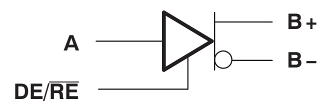
INPUT	OUTPUTS	
A	B+	B–
L	L	H
H	H	L

TRANSCEIVER



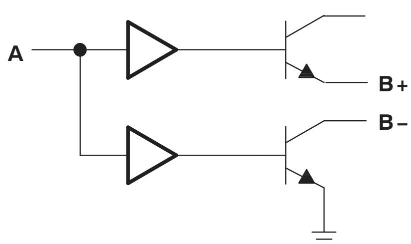
INPUTS				OUTPUTS		
DE/RE	A	B+[1]	B–[1]	A	B+	B–
L	–	L	H	L	–	–
L	–	H	L	H	–	–
H	L	–	–	–	L	H
H	H	–	–	–	H	L

DRIVER WITH ENABLE



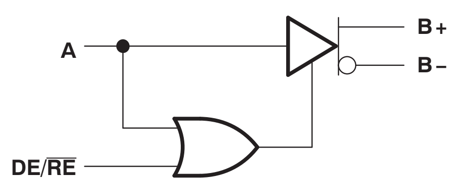
INPUTS		OUTPUTS	
DE/RE	A	B+	B–
L	L	Z	Z
L	H	Z	Z
H	L	L	H
H	H	H	L

WIRED-OR DRIVER



INPUT	OUTPUTS	
A	B+	B–
L	Z	Z
H	H	L

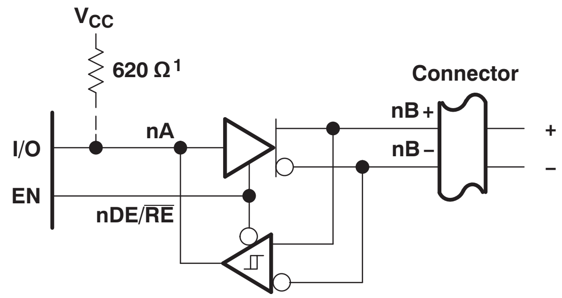
TWO-ENABLE INPUT DRIVER



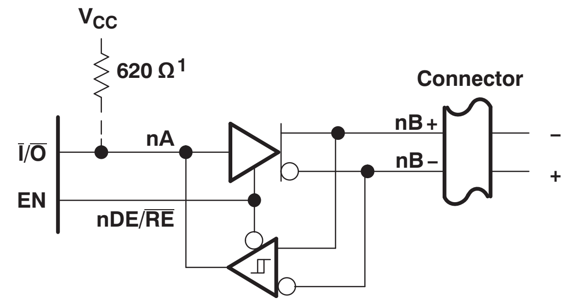
INPUTS		OUTPUTS	
DE/RE	A	B+	B–
L	L	Z	Z
L	H	H	L
H	L	L	H
H	H	H	L

NOTE: H = high level, L = low level, X = irrelevant, Z = high impedance (off)

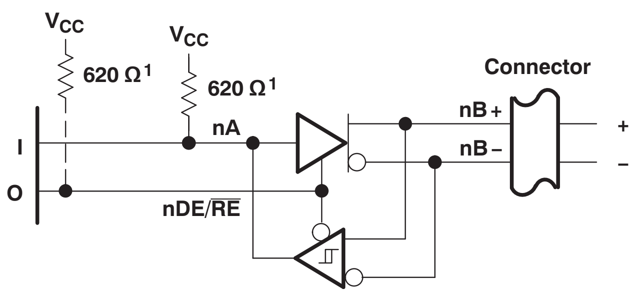
(1) An H in this column represents a voltage of 200 mV or higher than the other bus input. An L represents a voltage of 200 mV or lower than the other bus input. Any voltage less than 200 mV results in an indeterminate receiver output.



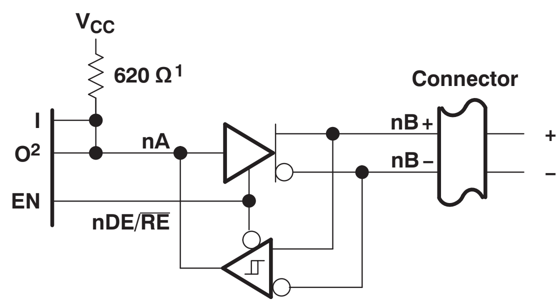
(a) ACTIVE-HIGH BIDIRECTIONAL I/O WITH SEPARATE ENABLE



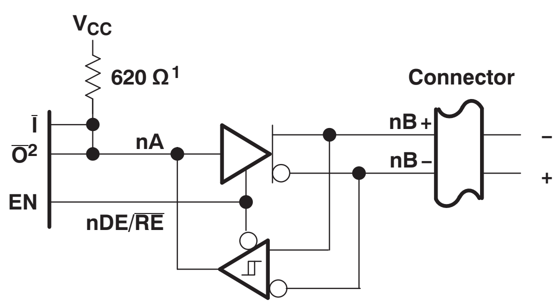
(b) ACTIVE-LOW BIDIRECTIONAL I/O WITH SEPARATE ENABLE



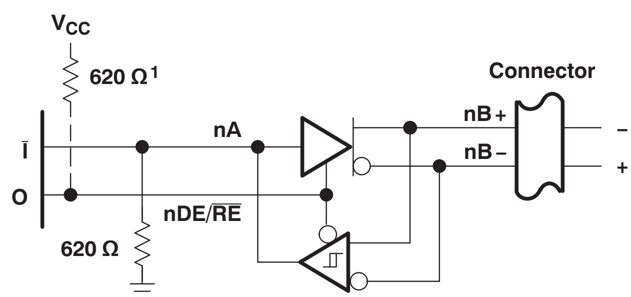
(c) WIRED-OR DRIVER AND ACTIVE-HIGH INPUT



(d) SEPARATE ACTIVE-HIGH INPUT, OUTPUT, AND ENABLE



(e) SEPARATE ACTIVE-LOW INPUT AND OUTPUT AND ACTIVE-HIGH ENABLE



(f) WIRED-OR DRIVER AND ACTIVE-LOW INPUT

1: When 0 is open drain
2: Must be open-drain or 3-state output

(1) When 0 is open drain

(2) Must be open-drain or 3-state output

NOTE: The BSR, $\overline{CRE}$, A, and DE/$\overline{RE}$ inputs have internal pullup resistors. CDE0, CDE1, and CDE2 have internal pulldown resistors.

Figure 19. Typical Transceiver Connections

CHANNEL LOGIC CONFIGURATIONS WITH CONTROL INPUT LOGIC

The following logic diagrams show the positive-logic representation for all combinations of control inputs. The control inputs are from MSB to LSB; the BSR, CDE0, CDE1, CDE2, and $\overline{CRE}$ bit values are shown below the diagrams. Channel 1 is at the top of the logic diagrams; channel 9 is at the bottom of the logic diagrams.

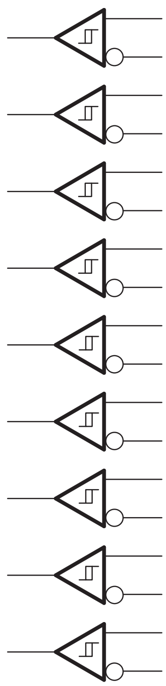


Figure 19. 00000

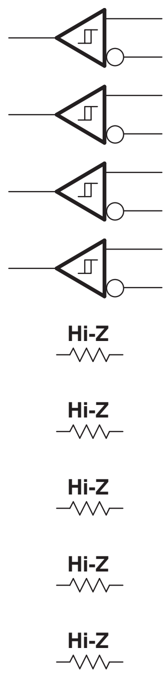


Figure 20. 00001

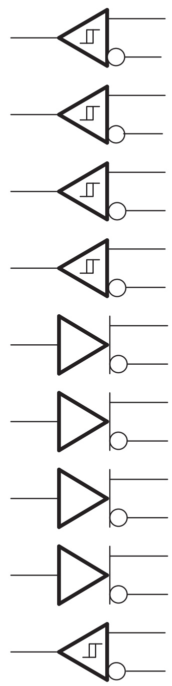


Figure 21. 00010

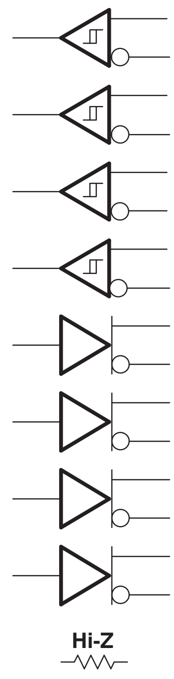


Figure 22. 00011

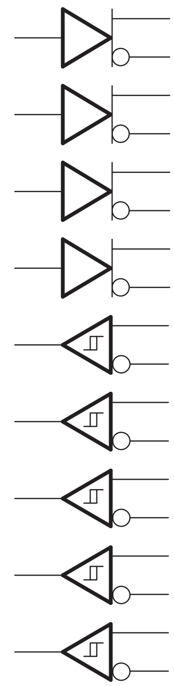


Figure 23. 00100

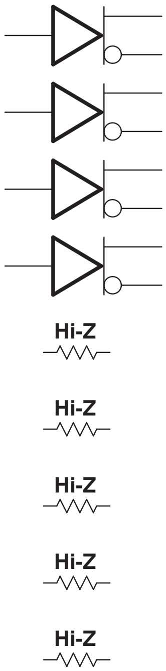


Figure 24. 00101

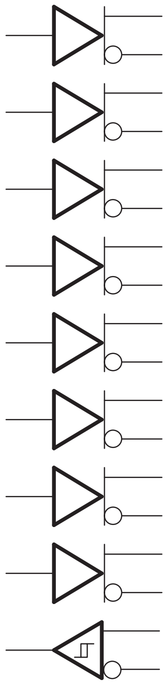


Figure 25. 00110

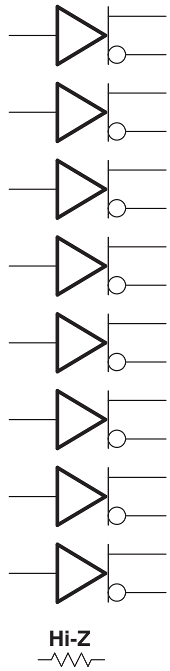


Figure 26. 00111

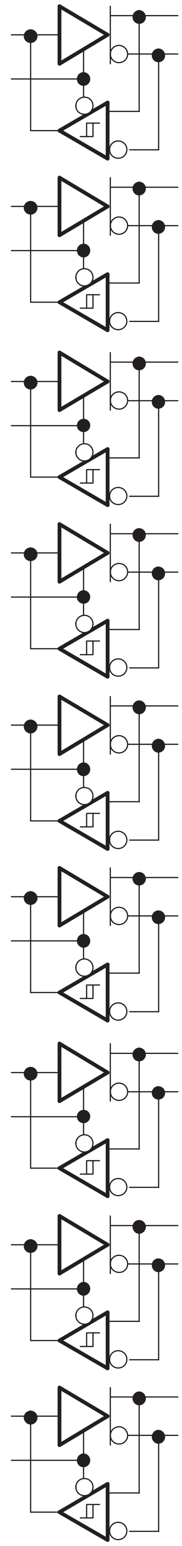


Figure 27. 01000

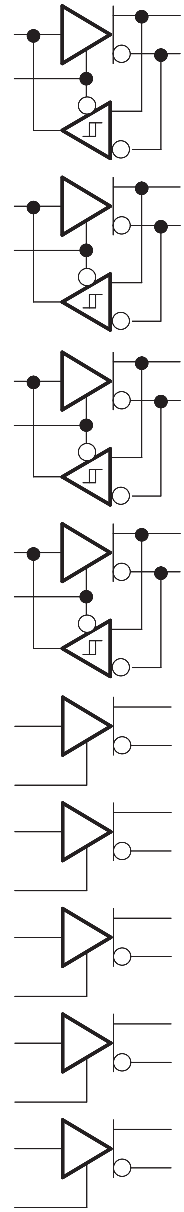


Figure 28. 01001

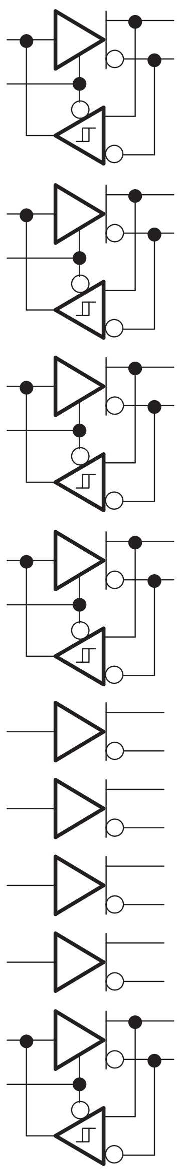


Figure 29. 01010

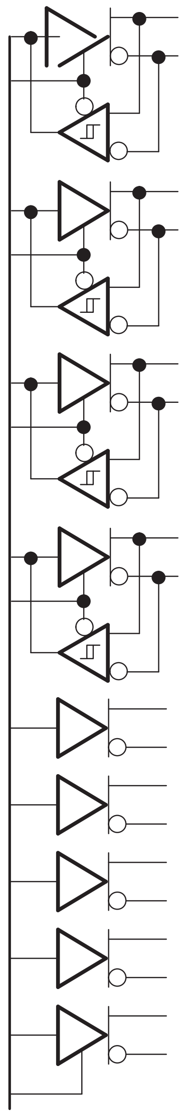


Figure 30. 01011

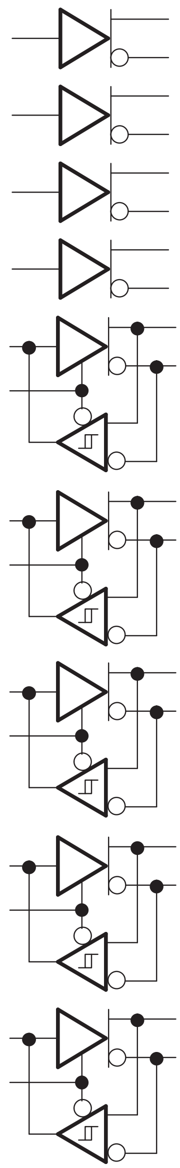


Figure 31. 01100

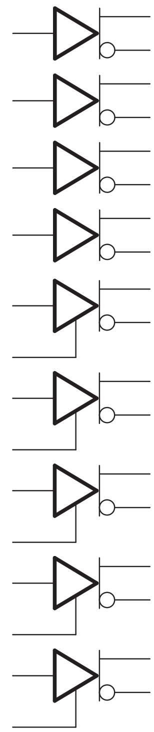


Figure 32. 01101

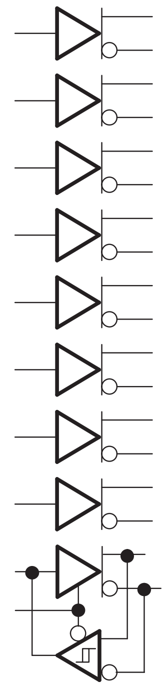


Figure 33. 01110

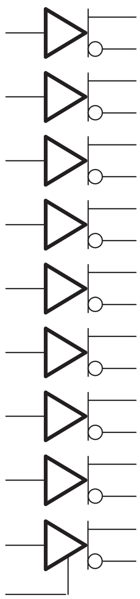


Figure 34. 01111

Figure 35. 10000 and 10001

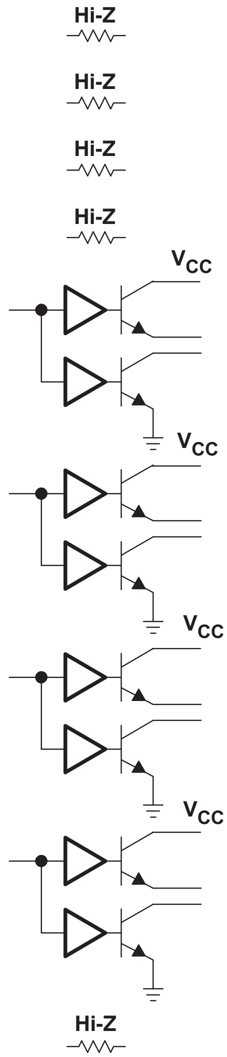


Figure 36. 10010 and 10011

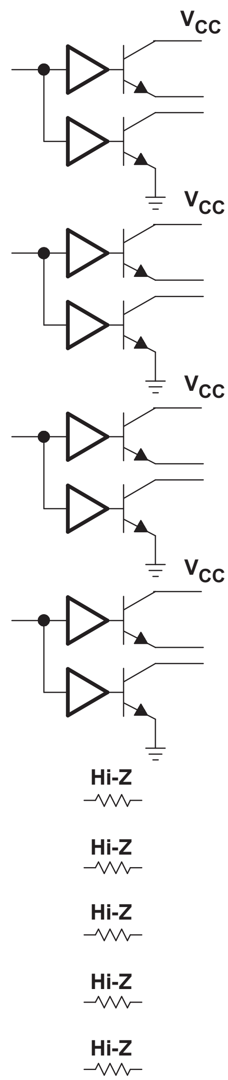


Figure 37. 10100 and 10101

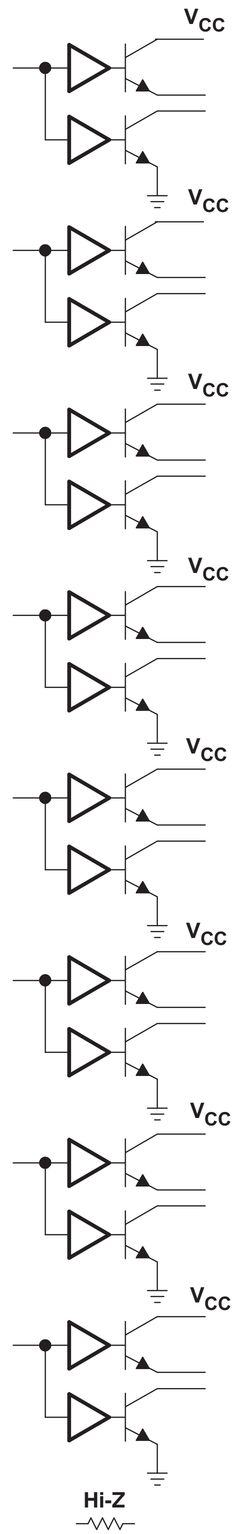


Figure 38. 10110 and 10111

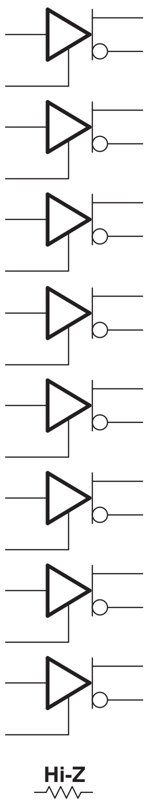


Figure 39. 11000 and 11001

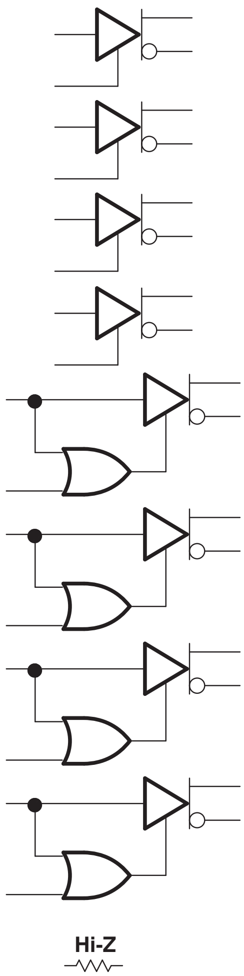


Figure 40. 11010 and 11011

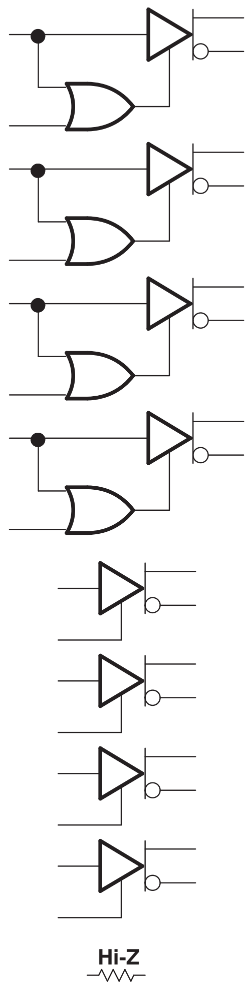


Figure 41. 11100 and 11101

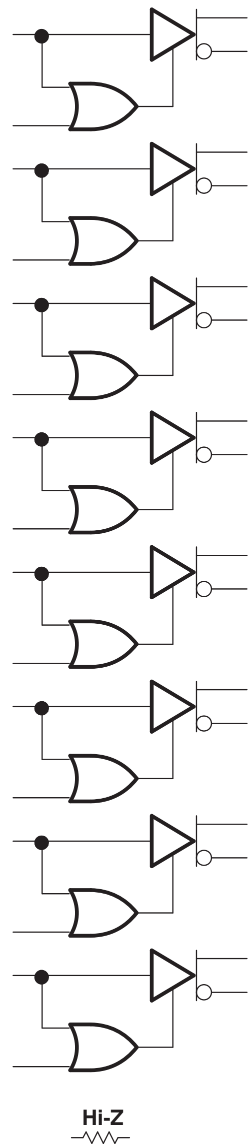
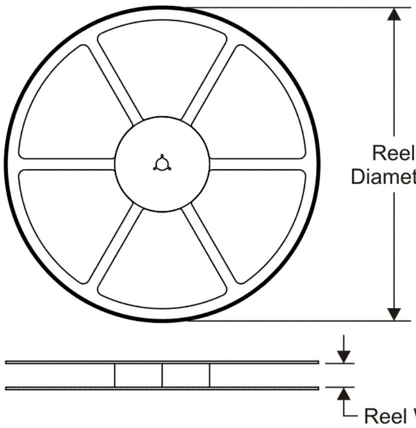
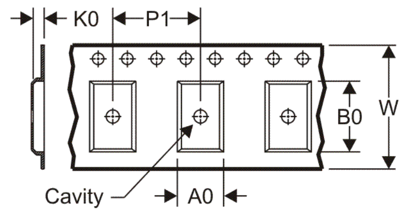


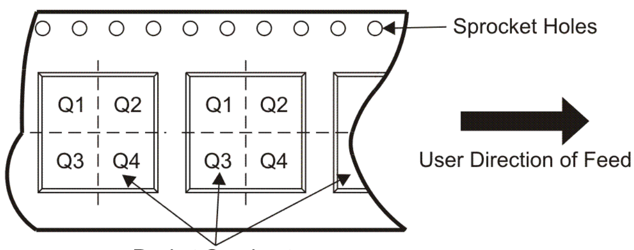
Figure 42. 11110 and 11111

TAPE AND REEL INFORMATION



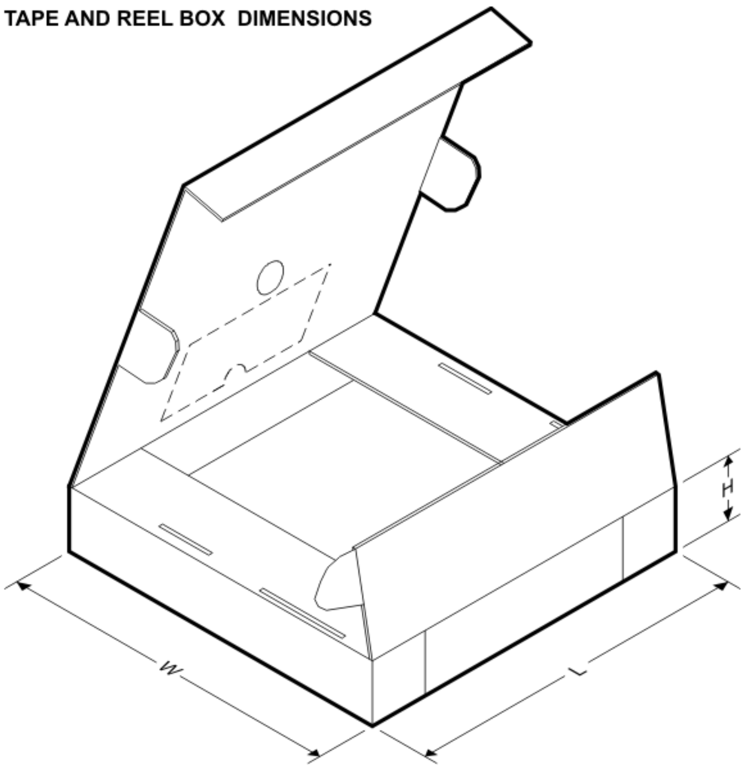


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD09DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

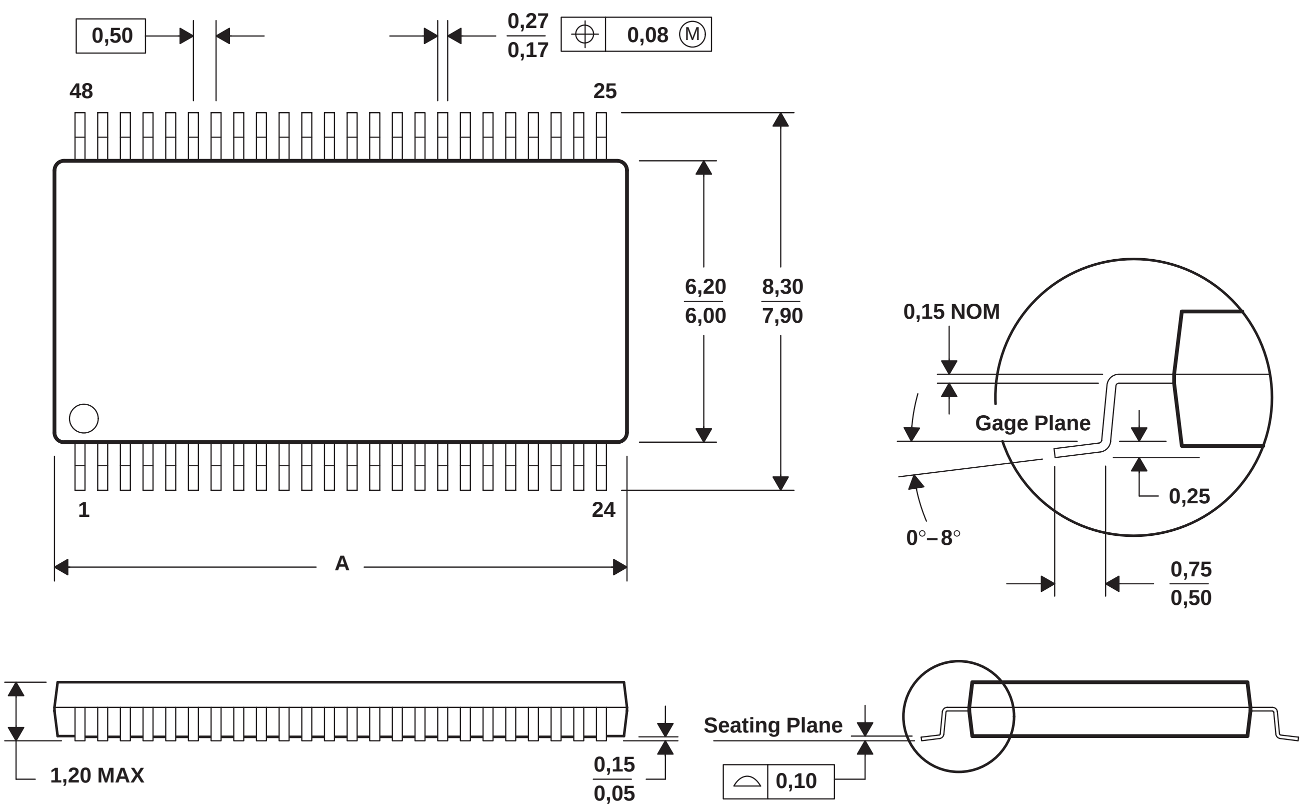


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD09DGGR	TSSOP	DGG	56	2000	346.0	346.0	41.0

DGG (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



PINS ** / DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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