

P-Channel 12 V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
- 12	0.0175 at $V_{GS} = - 4.5$ V	- 8	28.3 nC
	0.023 at $V_{GS} = - 2.5$ V	- 8	
	0.033 at $V_{GS} = - 1.8$ V	- 8	

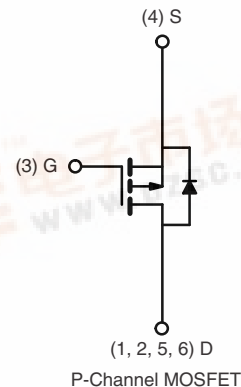
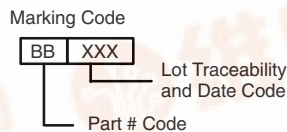
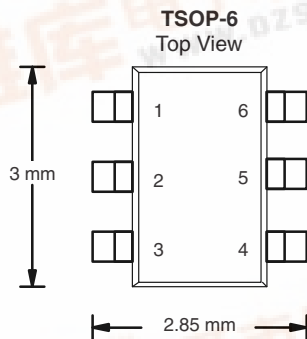
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- PWM Optimized
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC


RoHS
 COMPLIANT
 HALOGEN
FREE

APPLICATIONS

- Load Switch
- DC/DC Converters



Ordering Information: Si3477DV-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V_{DS}	- 12	V	
Gate-Source Voltage	V_{GS}	± 10		
Continuous Drain Current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	- 8 ^a	A
		$T_C = 70$ °C	- 8 ^a	
		$T_A = 25$ °C	- 8 ^{a, b, c}	
		$T_A = 70$ °C	- 7.2 ^{b, c}	
Pulsed Drain Current	I_{DM}	- 40		
Continuous Source-Drain Diode Current	I_S	$T_C = 25$ °C	- 3.5	
		$T_A = 25$ °C	- 1.67 ^{b, c}	
Maximum Power Dissipation	P_D	$T_C = 25$ °C	4.2	W
		$T_C = 70$ °C	2.7	
		$T_A = 25$ °C	2.0 ^{b, c}	
		$T_A = 70$ °C	1.3 ^{b, c}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	R_{thJA}	50	62.5	°C/W
Maximum Junction-to-Foot (Drain)	R_{thJF}	22	30	

Notes:

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- $t = 5$ s.
- Maximum under steady state conditions is 110 °C/W.

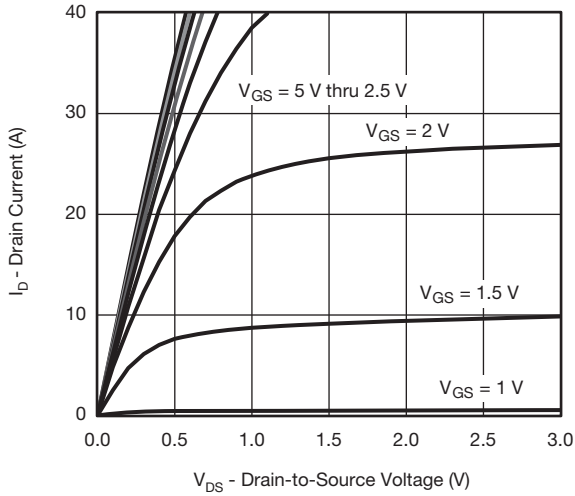
SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-12			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\ \mu\text{A}$		-4.1		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			2.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-0.4		-1.0	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 10\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -12\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = -12\text{ V}, V_{GS} = 0\text{ V}, T_J = 85^\circ\text{C}$			-10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$	-20			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -9\text{ A}$		0.014	0.0175	Ω
		$V_{GS} = -2.5\text{ V}, I_D = -7.9\text{ A}$		0.019	0.023	
		$V_{GS} = -1.8\text{ V}, I_D = -2.2\text{ A}$		0.026	0.033	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -6\text{ V}, I_D = -9\text{ A}$		30		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -6\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		2600		pF
Output Capacitance	C_{oss}			620		
Reverse Transfer Capacitance	C_{riss}			625		
Total Gate Charge	Q_g	$V_{DS} = -6\text{ V}, V_{GS} = -10\text{ V}, I_D = -9\text{ A}$		58	90	nC
				28.3	45	
Gate-Source Charge	Q_{gs}	$V_{DS} = -6\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -9\text{ A}$		4.2		
Gate-Drain Charge	Q_{gd}			7.8		
Gate Resistance	R_g	$f = 1\text{ MHz}$	0.9	4.5	9.0	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -6\text{ V}, R_L = 0.83\ \Omega$ $I_D \cong -7.2\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\ \Omega$		25	40	ns
Rise Time	t_r			30	45	
Turn-Off Delay Time	$t_{d(off)}$			65	100	
Fall Time	t_f			35	55	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -6\text{ V}, R_L = 0.83\ \Omega$ $I_D \cong -7.2\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\ \Omega$		10	15	
Rise Time	t_r			10	15	
Turn-Off Delay Time	$t_{d(off)}$			65	100	
Fall Time	t_f			30	45	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$			-3.5	A
Pulse Diode Forward Current ^a	I_{SM}				-40	
Body Diode Voltage	V_{SD}	$I_S = -7.2\text{ A}$		-0.8	-1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -7.2\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}, T_J = 25^\circ\text{C}$		50	75	ns
Body Diode Reverse Recovery Charge	Q_{rr}			30	45	nC
Reverse Recovery Fall Time	t_a			21		ns
Reverse Recovery Rise Time	t_b			29		

Notes:

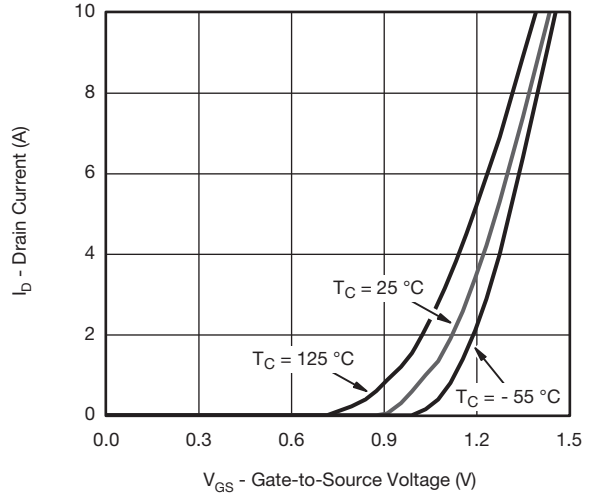
- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

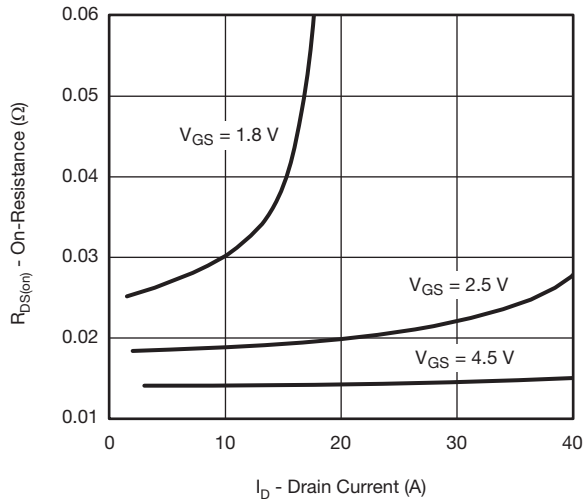
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



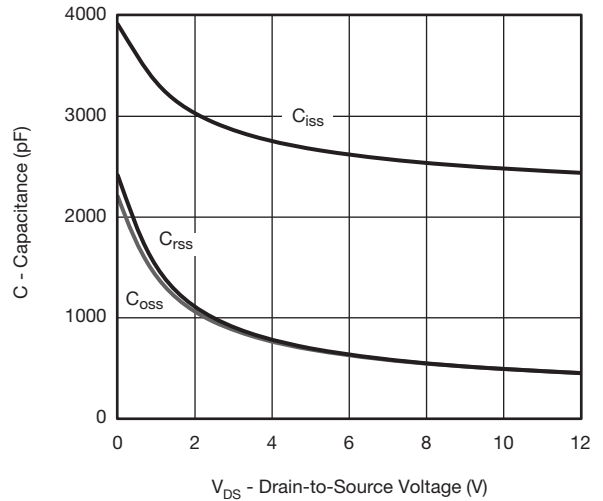
Output Characteristics



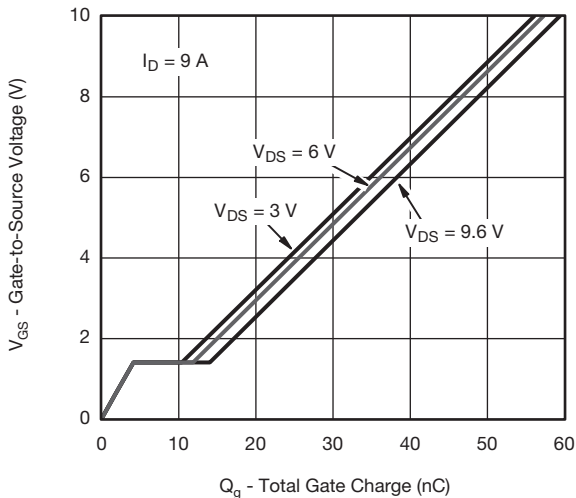
Transfer Characteristics



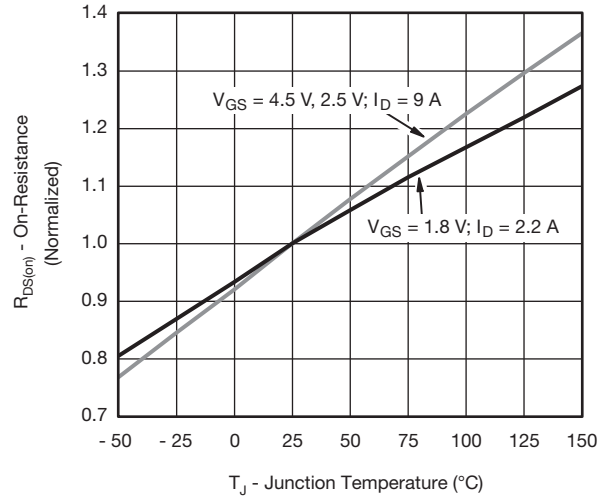
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



Gate Charge



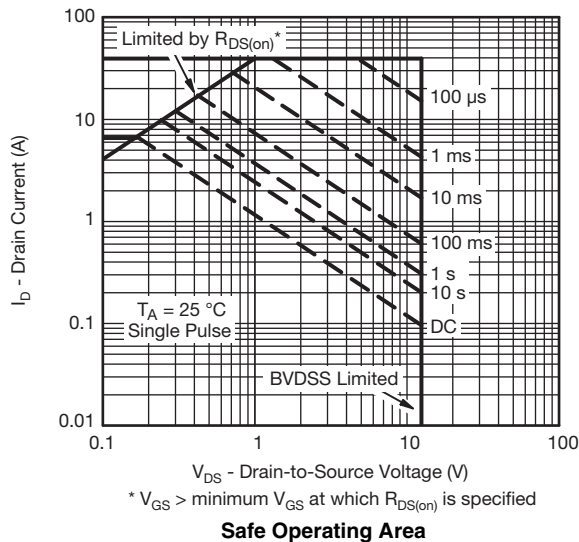
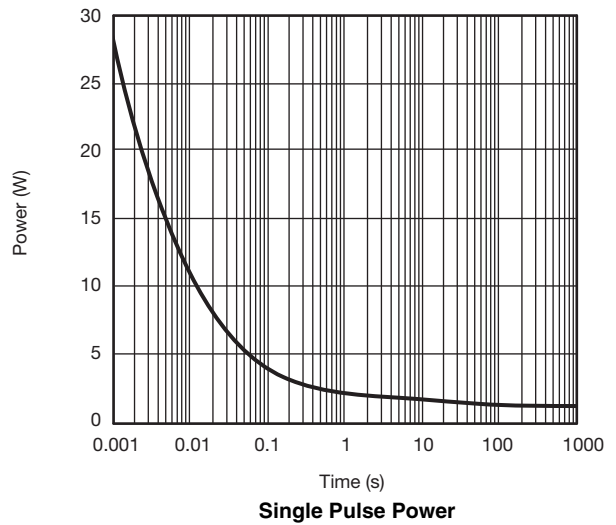
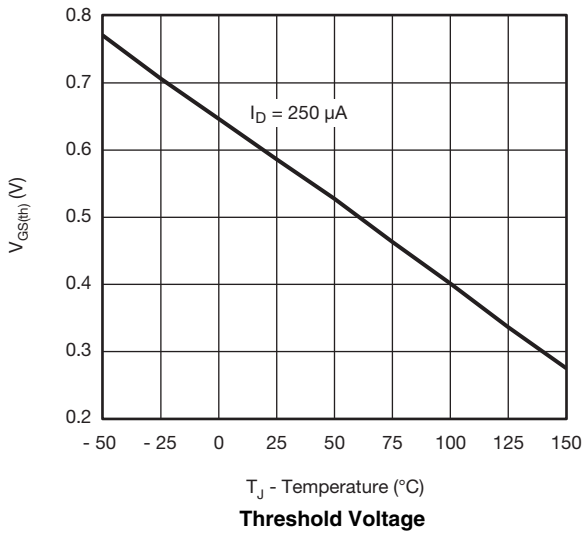
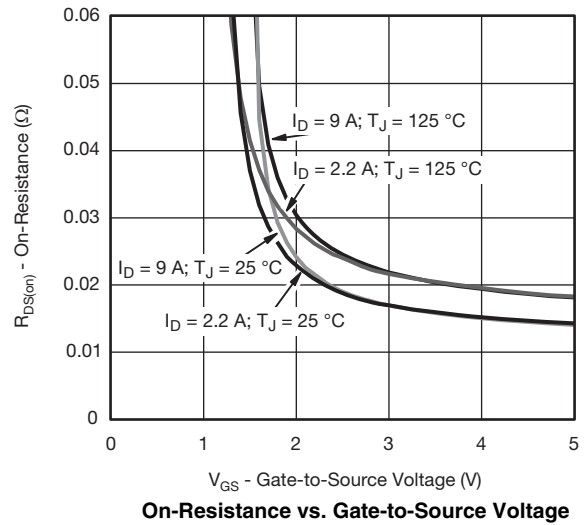
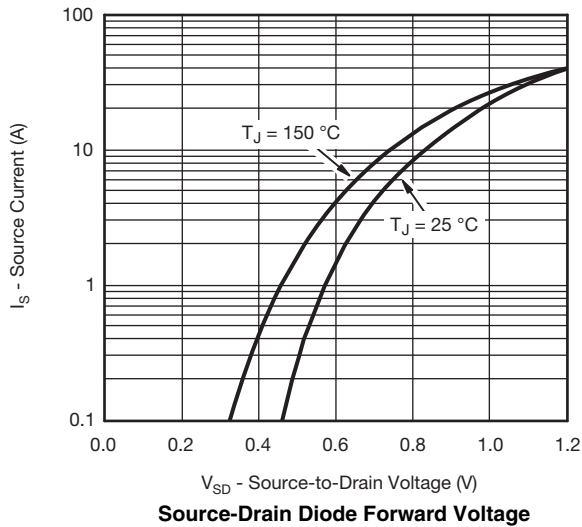
On-Resistance vs. Junction Temperature

Si3477DV

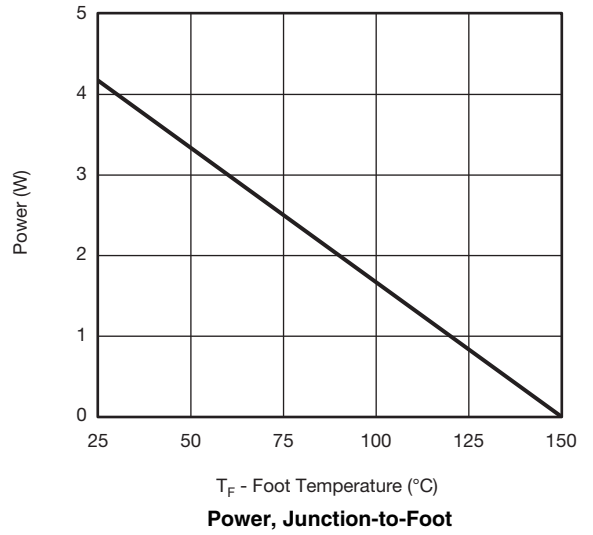
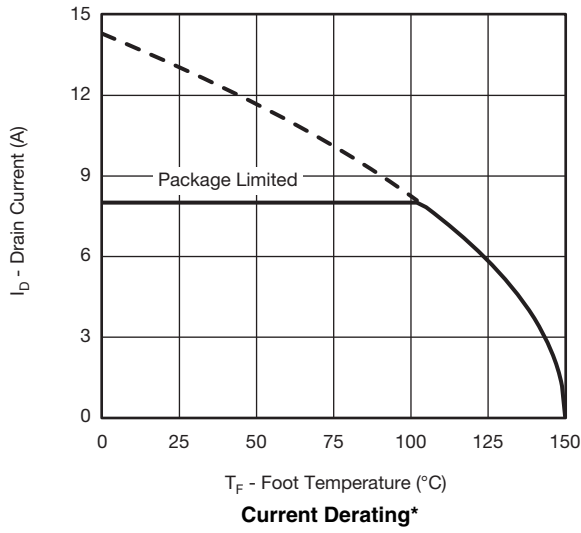
Vishay Siliconix 供应商



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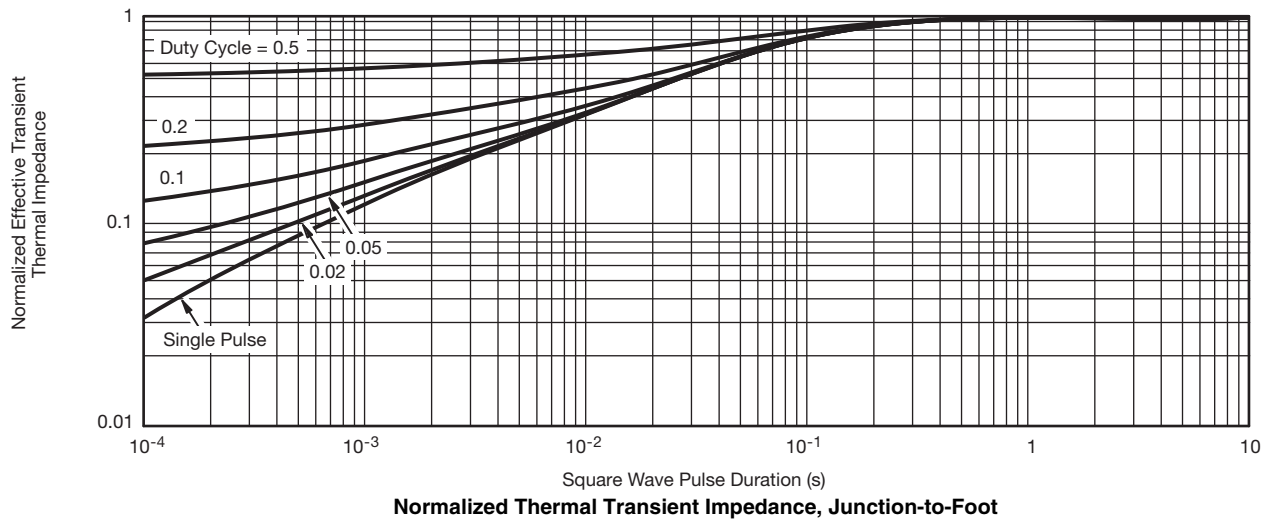
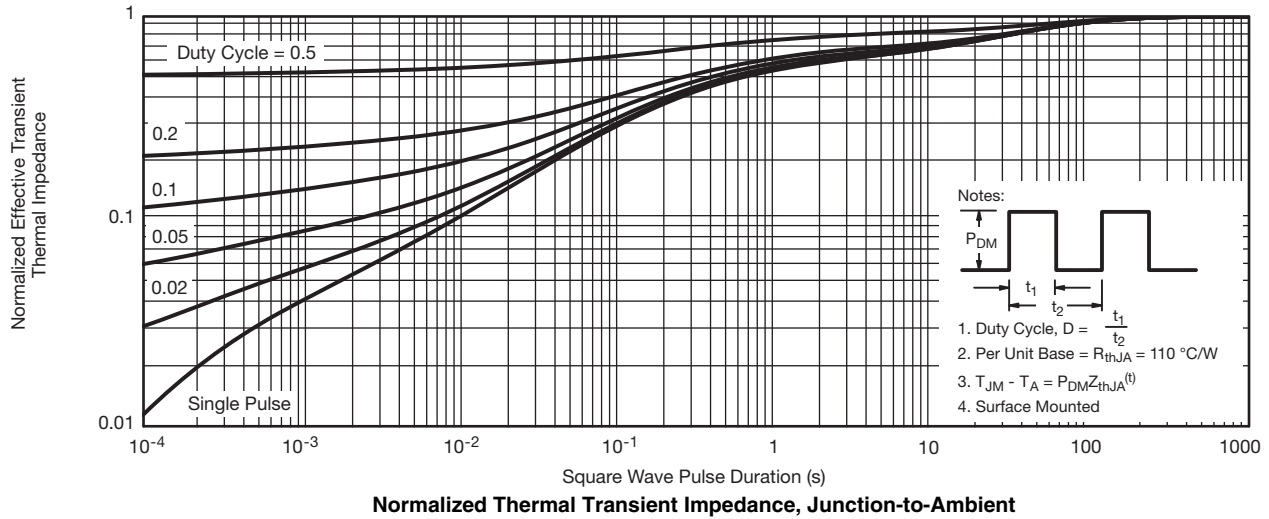
* The power dissipation P_D is based on $T_{J(max)} = 150\text{ °C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

Si3477DV



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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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