16-Channel, Constant-Current LED Driver

Check for Samples: TLC59281

FEATURES

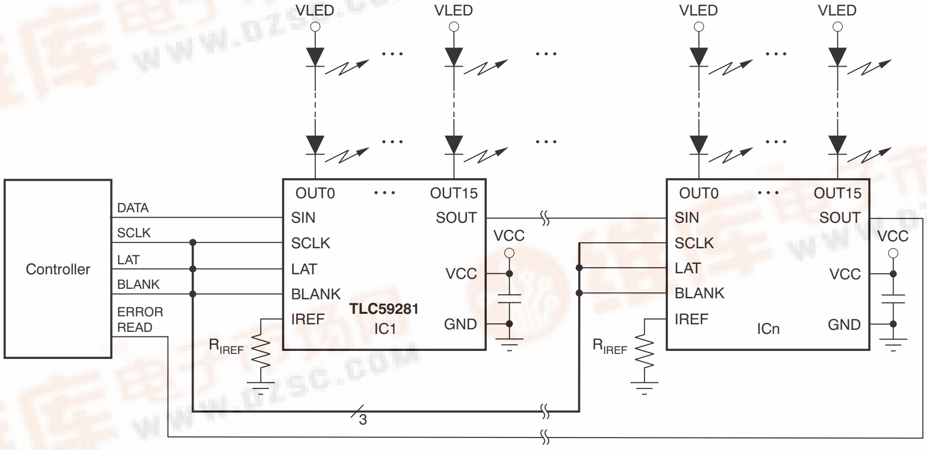
- **16 Channels, Constant-Current Sink Output with On/Off Control**
- **35-mA Capability (Constant-Current Sink)**
- **10-ns High-Speed Constant-Current Switching Transient Time**
- **Low On-Time Error**
- **LED Power-Supply Voltage up to 17 V**
- **V_{CC} = 3.0 V to 5.5 V**
- **Constant-Current Accuracy:**
  - **Channel-to-Channel = ±1%**
  - **Device-to-Device = ±1%**
- **CMOS Logic Level I/O**
- **35-MHz Data Transfer Rate**
- **20-ns BLANK Pulse Width**
- **Operating Temperature: –40°C to +85°C**

APPLICATIONS

- **LED Video Displays**
- **Message Boards**
- **Illumination**

DESCRIPTION

The TLC59281 is a 16-channel, constant-current sink LED driver. Each channel can be turned on/off by writing serial data to an internal register. The constant-current value of all 16 channels is set by a single external resistor.


VLED
VLED
VLED
VLED
Controller
DATA
SCLK
LAT
BLANK
ERROR
READ
OUT0
OUT15
SIN
SOUT
SCLK
LAT
BLANK
IREF
TLC59281
IC1
VCC
VCC
GND
R_{IREF}
3
OUT0
OUT15
SIN
SOUT
SCLK
LAT
BLANK
IREF
ICn
VCC
VCC
GND
R_{IREF}

Typical Application Circuit (Multiple Daisy-Chained TLC59281s)

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TLC59281	SSOP-24/QSOP-24	TLC59281DBQR	Tape and Reel, 2500
		TLC59281DBQ	Tube, 50
TLC59281	QFN-24	TLC59281RGER	Tape and Reel, 3000
		TLC59281RGE	Tape and Reel, 250

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Over operating free-air temperature range, unless otherwise noted.

PARAMETER			TLC59281	UNIT
V_{CC}	Supply voltage: V_{CC}		–0.3 to +6.0	V
I_{OUT}	Output current (dc)	OUT0 to OUT15	40	mA
V_{IN}	Input voltage range	SIN, SCLK, LAT, BLANK, IREF	–0.3 to V_{CC} + 0.3	V
V_{OUT}	Output voltage range	SOUT	–0.3 to V_{CC} + 0.3	V
		OUT0 to OUT15	–0.3 to +18	V
$T_{J(MAX)}$	Operating junction temperature		+150	°C
T_{STG}	Storage temperature range		–55 to +150	°C
	ESD rating	Human body model (HBM)	2	kV
		Charged device model (CDM)	500	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

(2) All voltage values are with respect to network ground terminal.

DISSIPATION RATINGS

PACKAGE	OPERATING FACTOR ABOVE T_A = +25°C	T_A < +25°C POWER RATING	T_A = +70°C POWER RATING	T_A = +85°C POWER RATING
SSOP-24/QSOP-24	14.3 mW/°C	1782 mW	1140 mW	927 mW
QFN-24(1)	24.8 mW/°C	3106 mW	1988 mW	1615 mW

(1) The package thermal impedance is calculated in accordance with JESD51-5.

RECOMMENDED OPERATING CONDITIONS

At T_A= –40°C to +85°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC59281			UNIT
			MIN	NOM	MAX	
DC Characteristics: V_{CC} = 3 V to 5.5 V						
V_{CC}	Supply voltage		3.0		5.5	V
V_O	Voltage applied to output	OUT0 to OUT15			17	V
V_{IH}	High-level input voltage		0.7 × V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage		GND		0.3 × V_{CC}	V
I_{OH}	High-level output current	SOUT			–1	mA
I_{OL}	Low-level output current	SOUT			1	mA
I_{OLC}	Constant output sink current	OUT0 to OUT15	2		35	mA
T_A	Operating free-air temperature range		–40		+85	°C
T_J	Operating junction temperature range		–40		+125	°C
AC Characteristics: V_{CC} = 3 V to 5.5 V						
$f_{CLK\ (SCLK)}$	Data shift clock frequency	SCLK			35	MHz
T_{WH0}	Pulse duration	SCLK	10			ns
T_{WL0}		SCLK	10			ns
T_{WH1}		LAT	20			ns
T_{WH2}		BLANK	20			ns
T_{WL2}		BLANK	20			ns
T_{SU0}	Setup time	SIN–SCLK↑	4			ns
T_{SU1}		LAT↑–SCLK↑	100			ns
T_{H0}	Hold time	SIN–SCLK↑	3			ns
T_{H1}		LAT↑–SCLK↑	10			ns

ELECTRICAL CHARACTERISTICS

At V_{CC} = 3.0 V to 5.5 V and T_A = –40°C to +85°C. Typical values at V_{CC} = 3.3 V and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC59281			UNIT
			MIN	TYP	MAX	
V_{OH}	High-level output voltage	I_{OH} = –1 mA at SOUT	V_{CC} – 0.4		V_{CC}	V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA at SOUT	0		0.4	V
I_{IN}	Input current	V_{IN} = V_{CC} or GND at SIN, SCLK, LAT, and BLANK	–1		1	µA
I_{CC1}	Supply current (V_{CC})	SIN/SCLK/LAT = low, BLANK = high, V_{OUTn} = 1 V, R_{IREF} = 27 kΩ		1	2	mA
I_{CC2}		SIN/SCLK/LAT = low, BLANK = high, V_{OUTn} = 1 V, R_{IREF} = 3 kΩ		4.5	8	mA
I_{CC3}		SIN/SCLK/LAT/BLANK = low, V_{OUTn} = 1 V, R_{IREF} = 3 kΩ		7	18	mA
I_{CC4}		SIN/SCLK/LAT/BLANK = low, V_{OUTn} = 1 V, R_{IREF} = 1.5 kΩ		16	40	mA
I_{OLC}	Constant output current	All OUTn = ON, V_{OUTn} = V_{OUTfix} = 1 V, R_{IREF} = 1.5 kΩ (see Figure 6), at OUT0 to OUT15	31	34	37	mA
I_{OLKG}	Output leakage current	All OUTn for constant-current driver, all outputs off BLANK = high, V_{OUTn} = V_{OUTfix} = 17 V, R_{IREF} = 1.5 kΩ (see Figure 6), at OUT0 to OUT15			0.1	µA
ΔI_{OLC}	Constant-current error (channel-to-channel)(1)	All OUTn = ON, V_{OUTn} = V_{OUTfix} = 1 V, R_{IREF} = 1.5 kΩ at OUT0 to OUT15		±1	±3	%
ΔI_{OLC1}	Constant-current error (device-to-device)(2)	All OUTn = ON, V_{OUTn} = V_{OUTfix} = 1 V, R_{IREF} = 1.5 kΩ at OUT0 to OUT15		±1	±6	%
ΔI_{OLC2}	Line regulation(3)	All OUTn = ON, V_{OUTn} = V_{OUTfix} = 1 V, R_{IREF} = 1.5 kΩ at OUT0 to OUT15		±0.5	±1	%/V
ΔI_{OLC3}	Load regulation(4)	All OUTn = ON, V_{OUTn} = 1 V to 3V, V_{OUTfix} = 1 V, R_{IREF} = 1.5 kΩ, at OUT0 to OUT15		±1	±3	%/V
V_{IREF}	Reference voltage output	R_{IREF} = 1.5 kΩ	1.16	1.20	1.24	V

(1) The deviation of each output from the average of OUT0–OUT15 constant-current. Deviation is calculated by the formula:

$$\Delta\,(\%) = \left(\frac{I_{OUTn}}{\dfrac{(I_{OUT0} + I_{OUT1} + \ldots + I_{OUT14} + I_{OUT15})}{16}} - 1\right) \times 100 .$$

(2) The deviation of the OUT0–OUT15 constant-current average from the ideal constant-current value. Deviation is calculated by the following formula:

$$\Delta\,(\%) = \left(\frac{\dfrac{(I_{OUT0} + I_{OUT1} + \ldots I_{OUT14} + I_{OUT15})}{16} - (\text{Ideal Output Current})}{\text{Ideal Output Current}}\right) \times 100$$

Ideal current is calculated by the formula:

$$I_{OUT(IDEAL)} = 42 \times \left(\frac{1.20}{R_{IREF}}\right)$$

(3) Line regulation is calculated by this equation:

$$\Delta\,(\%/V) = \left(\frac{(I_{OUTn} \text{ at } V_{CC} = 5.5\text{ V}) - (I_{OUTn} \text{ at } V_{CC} = 3.0\text{ V})}{(I_{OUTn} \text{ at } V_{CC} = 3.0\text{ V})}\right) \times \frac{100}{5.5\text{ V} - 3\text{ V}}$$

(4) Load regulation is calculated by the equation:

$$\Delta\,(\%/V) = \left(\frac{(I_{OUTn} \text{ at } V_{OUTn} = 3\text{ V}) - (I_{OUTn} \text{ at } V_{OUTn} = 1\text{ V})}{(I_{OUTn} \text{ at } V_{OUTn} = 1\text{ V})}\right) \times \frac{100}{3\text{ V} - 1\text{ V}}$$

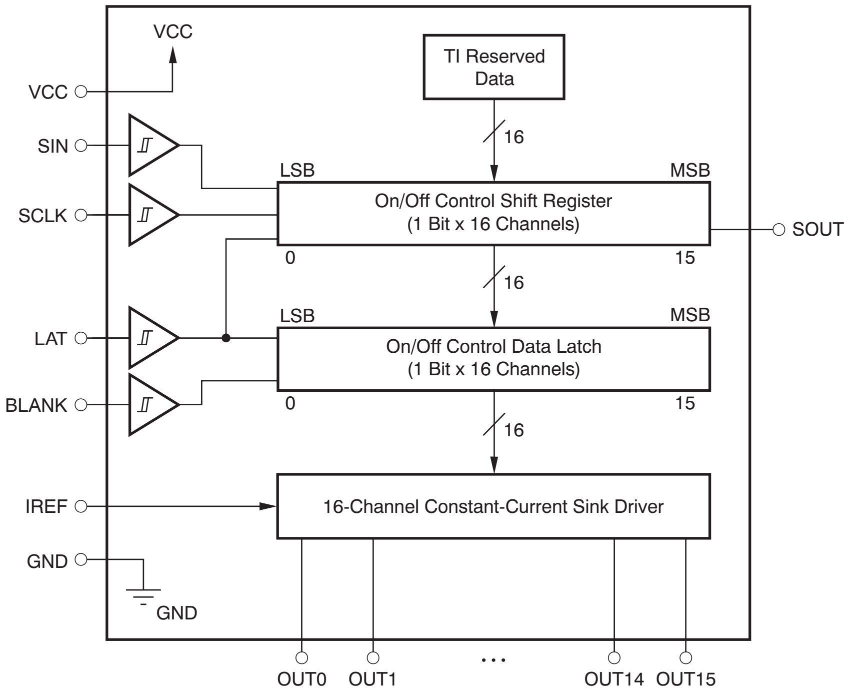
SWITCHING CHARACTERISTICS

At V_{CC} = 3.0 V to 5.5 V, T_A = –40°C to +85°C, C_L = 15 pF, R_L = 130 Ω, R_{IREF} = 1.5 kΩ, and V_{LED} = 5.5 V. Typical values at V_{CC} = 3.3 V and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC59281			UNIT
			MIN	TYP	MAX	
t_{R0}	Rise time	SOUT (see Figure 5)		5	15	ns
t_{R1}		OUTn (see Figure 4)		10	30	ns
t_{F0}	Fall time	SOUT (see Figure 5)		5	15	ns
t_{F1}		OUTn (see Figure 4)		10	30	ns
t_{D0}	Propagation delay time	SCLK↑ to SOUT		8	20	ns
t_{D1}		LAT↑ or BLANK↓ to OUTn sink current on (see Figure 10)		12	30	ns
t_{D2}		LAT↑ or BLANK↑ to OUTn sink current off (see Figure 10)		12	30	ns
t_{ON_ERR}	Output on-time error(1)	On/off latch data = all '1', 20 ns BLANK low level one-shot pulse input (see Figure 4)	–8		+8	ns

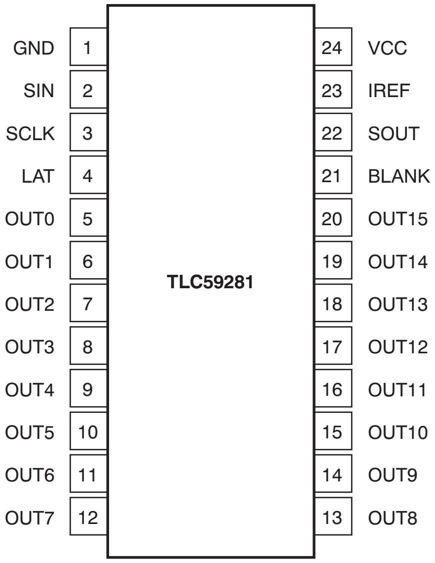
(1) Output on-time error (t_{ON_ERR}) is calculated by the formula: t_{ON_ERR} (ns) = t_{OUT_ON} – BLANK low level one-shot pulse width (T_{WL2}). t_{OUT_ON} indicates the actual on-time of the constant-current driver.

FUNCTIONAL BLOCK DIAGRAM

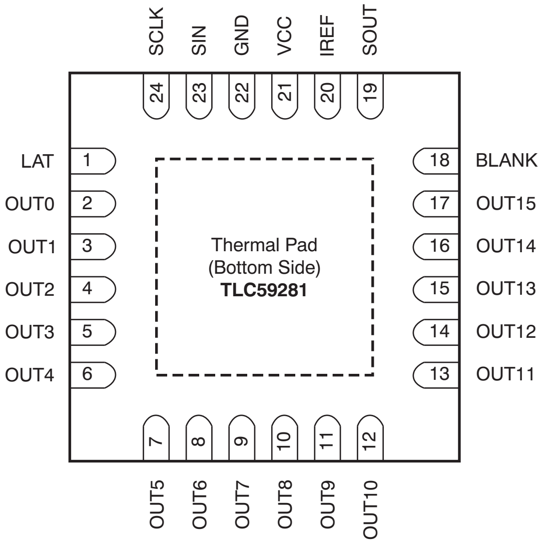

VCC
VCC
SIN
SCLK
LAT
BLANK
IREF
GND
GND
TI Reserved Data
16
LSB
MSB
On/Off Control Shift Register
(1 Bit x 16 Channels)
0
15
SOUT
16
LSB
MSB
On/Off Control Data Latch
(1 Bit x 16 Channels)
0
15
16
16-Channel Constant-Current Sink Driver
OUT0
OUT1
. . .
OUT14
OUT15

DEVICE INFORMATION

SSOP-24/QSOP-24
DBQ PACKAGE
(TOP VIEW)


GND 1
SIN 2
SCLK 3
LAT 4
OUT0 5
OUT1 6
OUT2 7
OUT3 8
OUT4 9
OUT5 10
OUT6 11
OUT7 12
TLC59281
24 VCC
23 IREF
22 SOUT
21 BLANK
20 OUT15
19 OUT14
18 OUT13
17 OUT12
16 OUT11
15 OUT10
14 OUT9
13 OUT8

QFN-24
RGE PACKAGE
(TOP VIEW)


SCLK 24
SIN 23
GND 22
VCC 21
IREF 20
SOUT 19
LAT 1
OUT0 2
OUT1 3
OUT2 4
OUT3 5
OUT4 6
Thermal Pad
(Bottom Side)
TLC59281
18 BLANK
17 OUT15
16 OUT14
15 OUT13
14 OUT12
13 OUT11
7 OUT5
8 OUT6
9 OUT7
10 OUT8
11 OUT9
12 OUT10

NOTE: Thermal pad is not connected to GND internally. The thermal pad must be connected to GND via the PCB pattern.

TERMINAL FUNCTIONS

TERMINAL				
NAME	**DBQ**	**RGE**	**I/O**	**DESCRIPTION**
SIN	2	23	I	Serial data input for driver on/off control. When SIN = high level, data '1' are written into LSB of the on/off control shift register at the rising edge of SCLK.
SCLK	3	24	I	Serial data shift clock. Schmitt buffer input. All data in the on/off control shift register are shifted toward the MSB by 1-bit synchronization of SCLK. A rising edge on SCLK is allowed 100 ns after a rising edge of LAT.
LAT	4	1	I	Edge triggered latch. The data in the on/off control data shift register are transferred to the on/off control data latch at this rising edge. At the same time, the data in the on/off control shift register are replaced with TI reserved data for production test. LAT must be toggled only once after the shift data are updated to avoid the on/off control latch data being replaced with TI reserved data in the shift register. The reserved data is not a fixed number.
BLANK	21	18	I	Blank, all outputs. When BLANK = high level, all constant-current outputs (OUT0–OUT15) are forced off. When BLANK = low level, all constant-current outputs are controlled by the on/off control data in the data latch.
IREF	23	20	I/O	Constant-current value setting, OUT0–OUT15 sink constant-current is set to desired value by connection to an external resistor between IREF and GND.
SOUT	22	19	O	Serial data output. This output is connected to the MSB of the on/off data shift register. SOUT data changes at the rising edge of SCLK.
OUT0	5	2	O	Constant-current output. Each output can be tied together with others to increase the constant-current. Different voltages can be applied to each output.
OUT1	6	3	O	Constant-current output
OUT2	7	4	O	Constant-current output
OUT3	8	5	O	Constant-current output
OUT4	9	6	O	Constant-current output
OUT5	10	7	O	Constant-current output
OUT6	11	8	O	Constant-current output
OUT7	12	9	O	Constant-current output
OUT8	13	10	O	Constant-current output
OUT9	14	11	O	Constant-current output
OUT10	15	12	O	Constant-current output
OUT11	16	13	O	Constant-current output
OUT12	17	14	O	Constant-current output
OUT13	18	15	O	Constant-current output
OUT14	19	16	O	Constant-current output
OUT15	20	17	O	Constant-current output
VCC	24	21	—	Power-supply voltage
GND	1	22	—	Power ground

PARAMETER MEASUREMENT INFORMATION

PIN EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

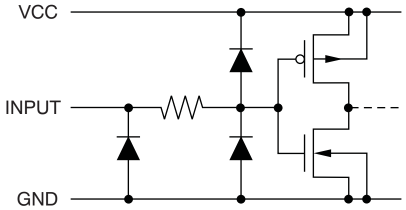

VCC
INPUT
GND

Figure 1. SIN, SCLK, LAT, BLANK

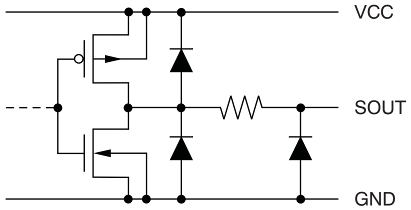

VCC
SOUT
GND

Figure 2. SOUT

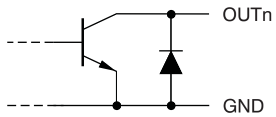
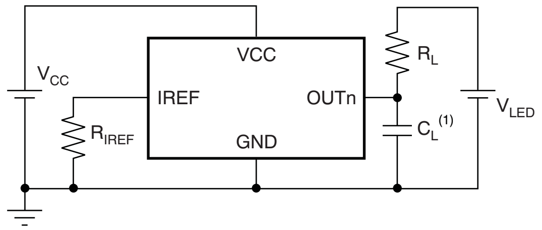


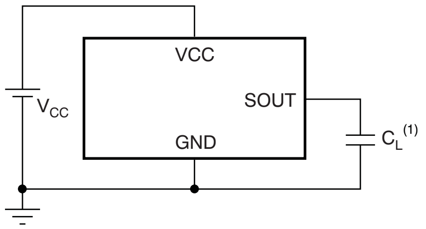
Figure 3. OUT0 Through OUT15

TEST CIRCUITS


VCC
IREF
OUTn
GND
V_{CC}
R_{IREF}
R_L
$C_L^{(1)}$
V_{LED}

(1) C_L includes measurement probe and jig capacitance.

Figure 4. Rise Time and Fall Time Test Circuit for OUTn


VCC
SOUT
GND
V_{CC}
$C_L^{(1)}$

(1) C_L includes measurement probe and jig capacitance.

Figure 5. Rise Time and Fall Time Test Circuit for SOUT

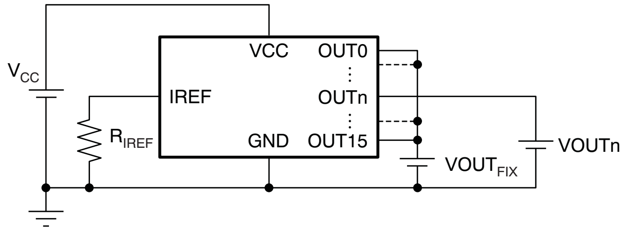
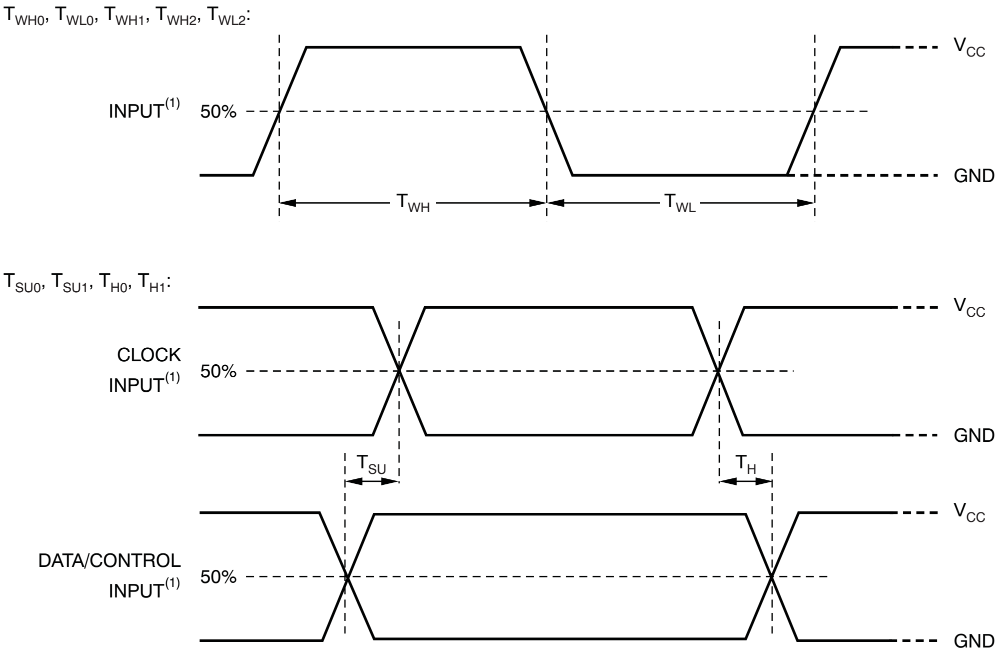

VCC
OUT0
IREF
OUTn
GND
OUT15
V_{CC}
R_{IREF}
$VOUT_{FIX}$
VOUTn

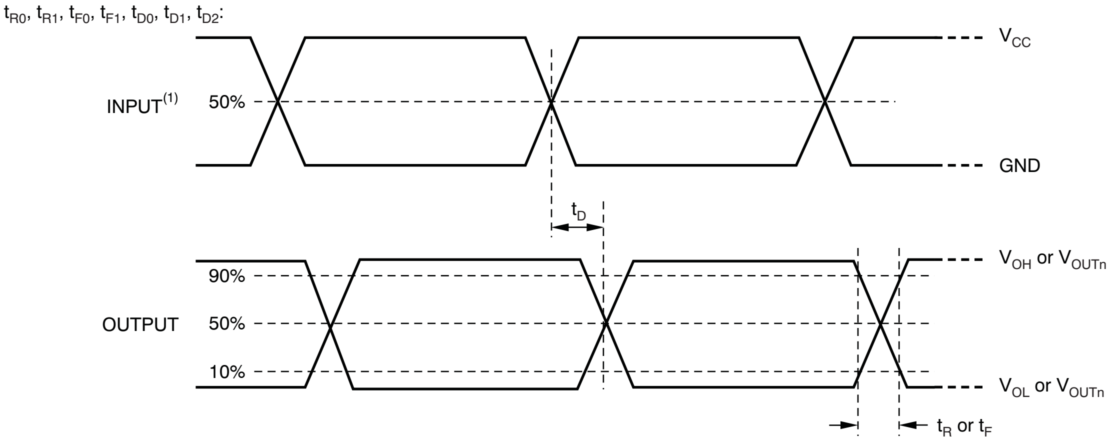
Figure 6. Constant-Current Test Circuit for OUTn

TIMING DIAGRAMS


T_{WH0}, T_{WL0}, T_{WH1}, T_{WH2}, T_{WL2}:
INPUT$^{(1)}$
50%
V_{CC}
GND
T_{WH}
T_{WL}
T_{SU0}, T_{SU1}, T_{H0}, T_{H1}:
CLOCK INPUT$^{(1)}$
50%
V_{CC}
GND
T_{SU}
T_H
DATA/CONTROL INPUT$^{(1)}$
50%
V_{CC}
GND

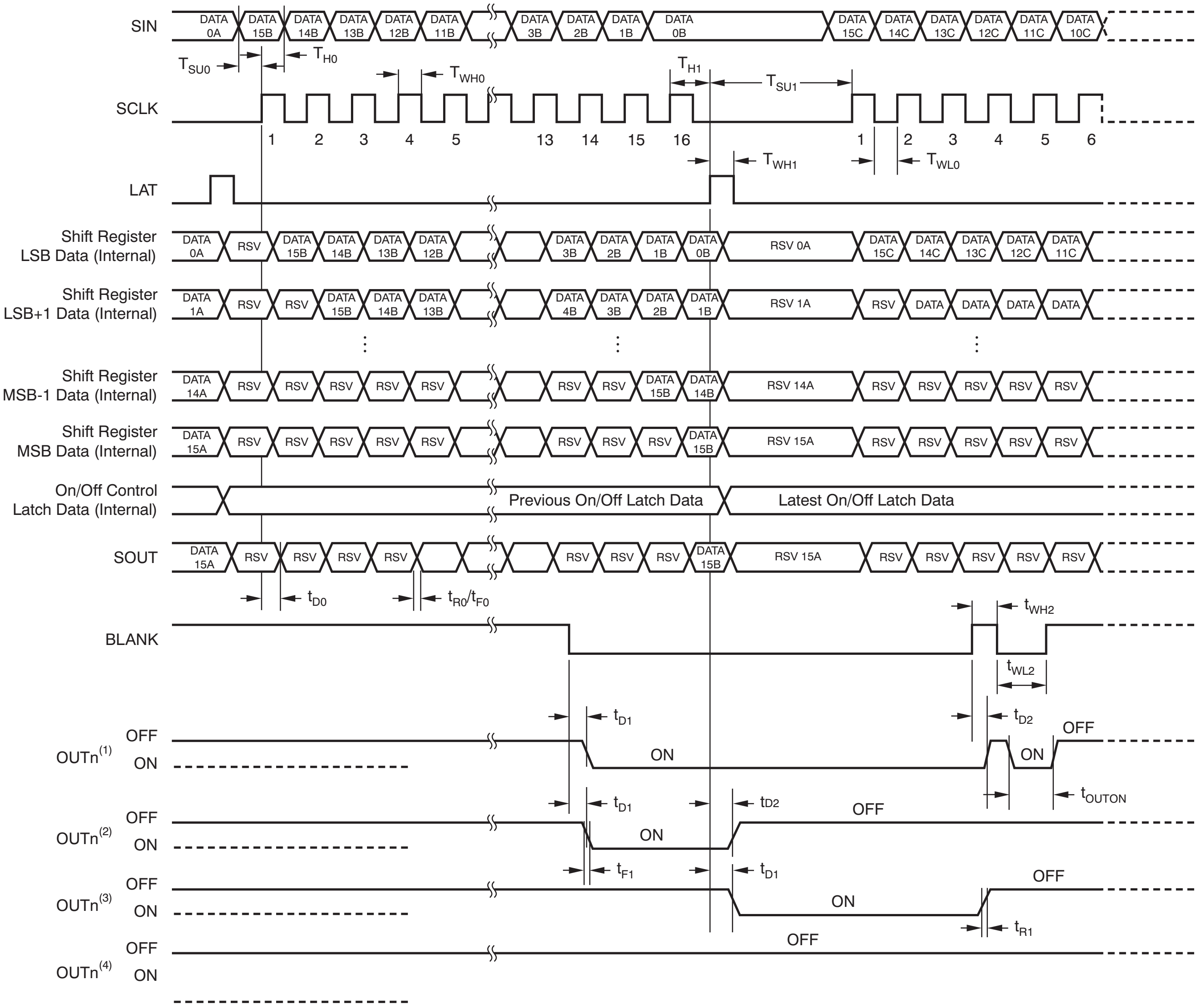
(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 7. Input Timing


t_{R0}, t_{R1}, t_{F0}, t_{F1}, t_{D0}, t_{D1}, t_{D2}:
INPUT$^{(1)}$
50%
V_{CC}
GND
t_D
OUTPUT
90%
50%
10%
V_{OH} or V_{OUTn}
V_{OL} or V_{OUTn}
t_R or t_F

(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 8. Output Timing


SIN
DATA 0A
DATA 15B
DATA 14B
DATA 13B
DATA 12B
DATA 11B
DATA 3B
DATA 2B
DATA 1B
DATA 0B
DATA 15C
DATA 14C
DATA 13C
DATA 12C
DATA 11C
DATA 10C
TSU0
TH0
TWH0
TH1
TSU1
SCLK
1 2 3 4 5 13 14 15 16 1 2 3 4 5 6
TWH1
TWL0
LAT
Shift Register LSB Data (Internal)
RSV
RSV 0A
Shift Register LSB+1 Data (Internal)
DATA 1A
DATA 4B
RSV 1A
Shift Register MSB-1 Data (Internal)
DATA 14A
RSV 14A
Shift Register MSB Data (Internal)
DATA 15A
RSV 15A
On/Off Control Latch Data (Internal)
Previous On/Off Latch Data
Latest On/Off Latch Data
SOUT
tD0
tR0/tF0
BLANK
tWH2
tWL2
tD1
tD2
tOUTON
tF1
tR1
OUTn(1)
OUTn(2)
OUTn(3)
OUTn(4)
OFF
ON

(1) On/off latched data are '1'.

(2) On/off latched data are changed from '1' to '0' at the second LAT signal.

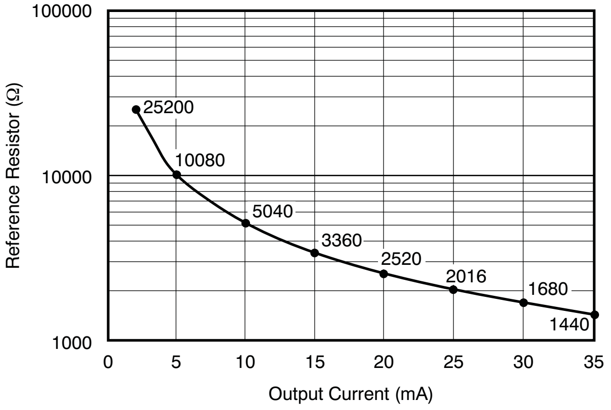
(3) On/off latched data are changed from '0' to '1' at the second LAT signal.

(4) On/off latched data are '0'.

Figure 9. Timing Diagram

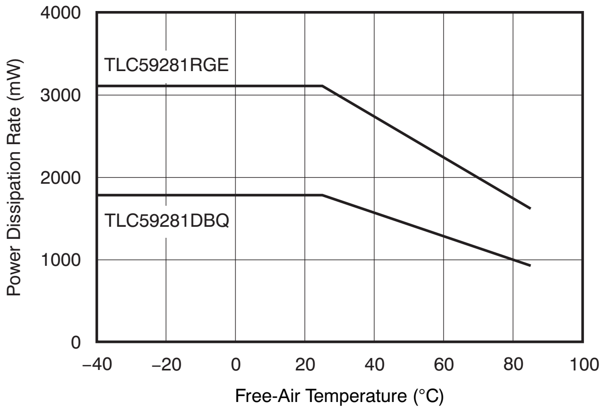
TYPICAL CHARACTERISTICS

At V_{CC} = 3.3 V and T_A = +25°C, unless otherwise noted.



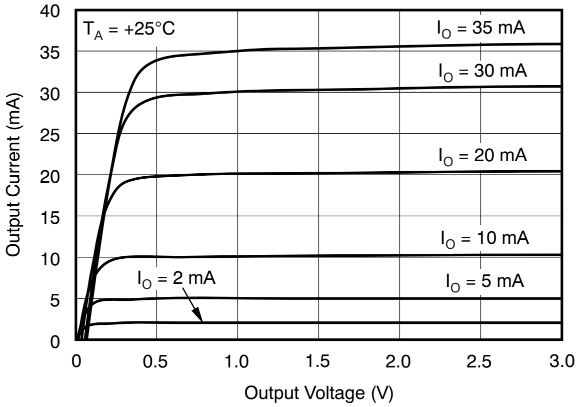
REFERENCE RESISTOR vs OUTPUT CURRENT

Figure 10.



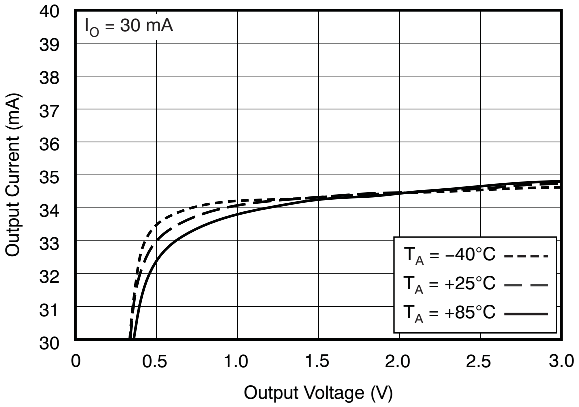
POWER DISSIPATION RATE vs FREE-AIR TEMPERATURE

Figure 11.



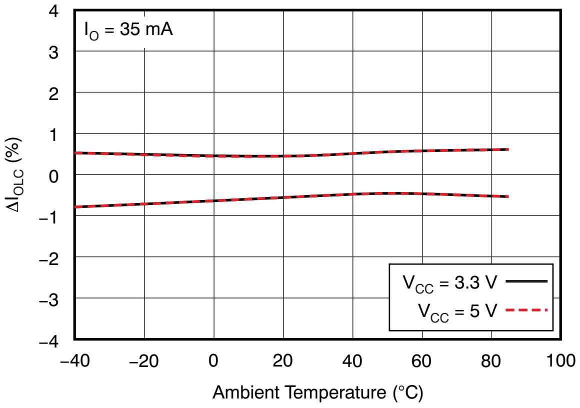
OUTPUT CURRENT vs OUTPUT VOLTAGE

Figure 12.



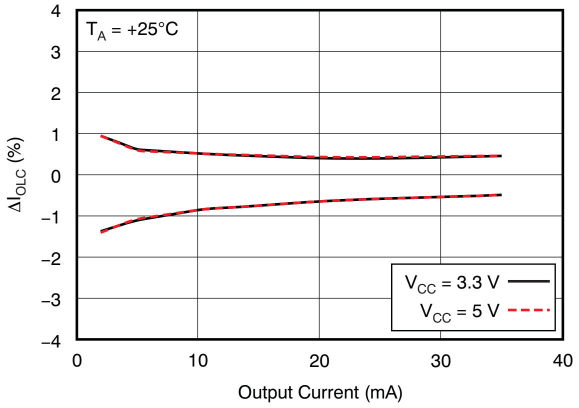
OUTPUT CURRENT vs OUTPUT VOLTAGE

Figure 13.



ΔI_{OLC} vs AMBIENT TEMPERATURE

Figure 14.



ΔI_{OLC} vs OUTPUT CURRENT

Figure 15.

TYPICAL CHARACTERISTICS (continued)

At V_{CC} = 3.3 V and T_A = +25°C, unless otherwise noted.

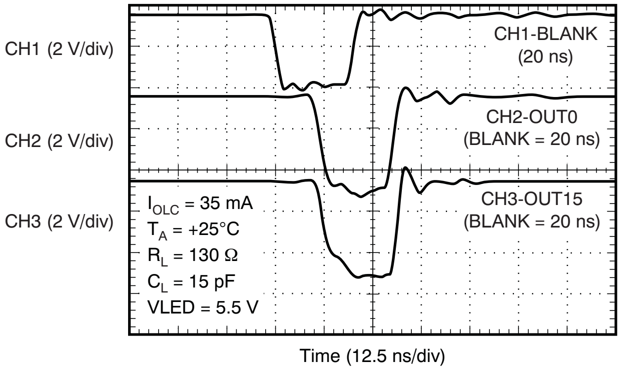

CONSTANT-CURRENT OUTPUT VOLTAGE WAVEFORM

Figure 16.

DETAILED DESCRIPTION

SETTING FOR THE CONSTANT SINK CURRENT VALUE

The constant-current values are determined by an external resistor (R_{IREF}) placed between IREF and GND. The resistor (R_{IREF}) value is calculated by Equation 1.

$$R_{IREF}\ (k\Omega) = \frac{V_{IREF}\ (V)}{I_{OLC}\ (mA)} \times 42$$

Where:

V_{IREF} = the internal reference voltage on the IREF pin (typically 1.20 V) (1)

I_{OLC} must be set in the range of 2 mA to 35 mA. The constant sink current characteristic for the external resistor value is shown in Figure 10. Table 1 describes the constant-current output versus external resistor value.

Table 1. Constant-Current Output versus External Resistor Value

I_{OLCMax} (mA, Typical)	R_{IREF} (kΩ)
35	1.44
30	1.68
25	2.02
20	2.52
15	3.36
10	5.04
5	10.1
2	25.2

CONSTANT-CURRENT DRIVER ON/OFF CONTROL

When BLANK is low, the corresponding output is turned on if the data in the on/off control data latch are '1' and remains off if the data are '0'. When BLANK is high, all outputs are forced off. This control is shown in Table 2.

Table 2. On/Off Control Data Truth Table

ON/OFF CONTROL LATCH DATA	CONSTANT-CURRENT OUTPUT STATUS
0	Off
1	On

When the IC is initially powered on, the data in the on/off control shift register and data latch are not set to the respective default value. Therefore, the on/off control data must be written to the data latch before turning the constant-current output on. BLANK should be at a high level when powered on because the constant-current may be turned on as a result of random data in the on/off control latch.

The on/off data corresponding to any unconnected OUTn outputs should be set to ‘0’ before turning on the remaining outputs. Otherwise, the supply current (I_{CC}) increases while the LEDs are on.

REGISTER CONFIGURATION

The TLC59281 has an on/off control data shift register and data latch. Both the on/off control shift register and latch are 16 bits long and are used to turn the constant-current drivers on and off. Figure 17 shows the shift register and latch configuration. The data at the SIN pin are shifted in to the LSB of the shift register at the rising edge of the SCLK pin; SOUT data change at the rising edge of SCLK. The timing diagram for data writing is shown in Figure 18. The driver on/off is controlled by the data in the on/off control data latch.

The on/off data are latched into the data latch by a rising edge of LAT after the data are written into the on/off control shift register by SIN and SCLK. At the same time, the data in the on/off control shift register are replaced with TI reserved data for production test. Therefore, LAT must be input only once after the on/off data update to avoid the on/off control data latch being replaced with TI reserved data in the shift register. When the IC initially powers on, the data in the on/off control shift register and latch are not set to the default values; on/off control data must be written to the on/off control data latch before turning the constant-current output on. BLANK should be high when the IC is powered on because the constant-current may be turned on at that time as a result of random values in the on/off data latch. All constant-current outputs are forced off when BLANK is high.

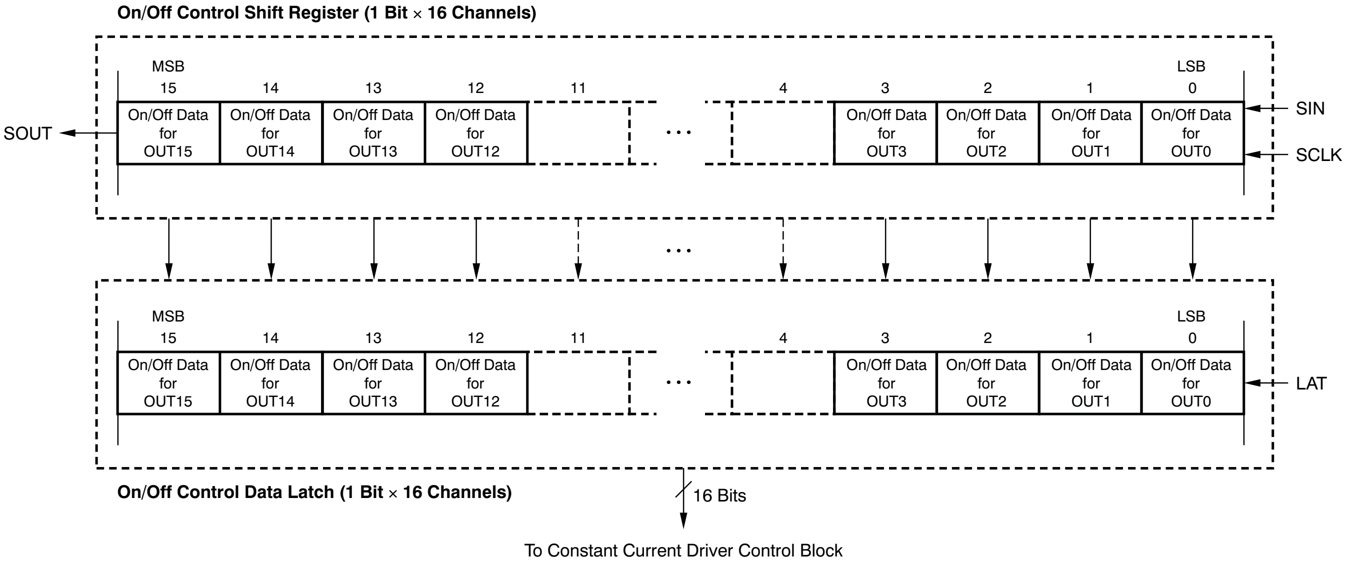
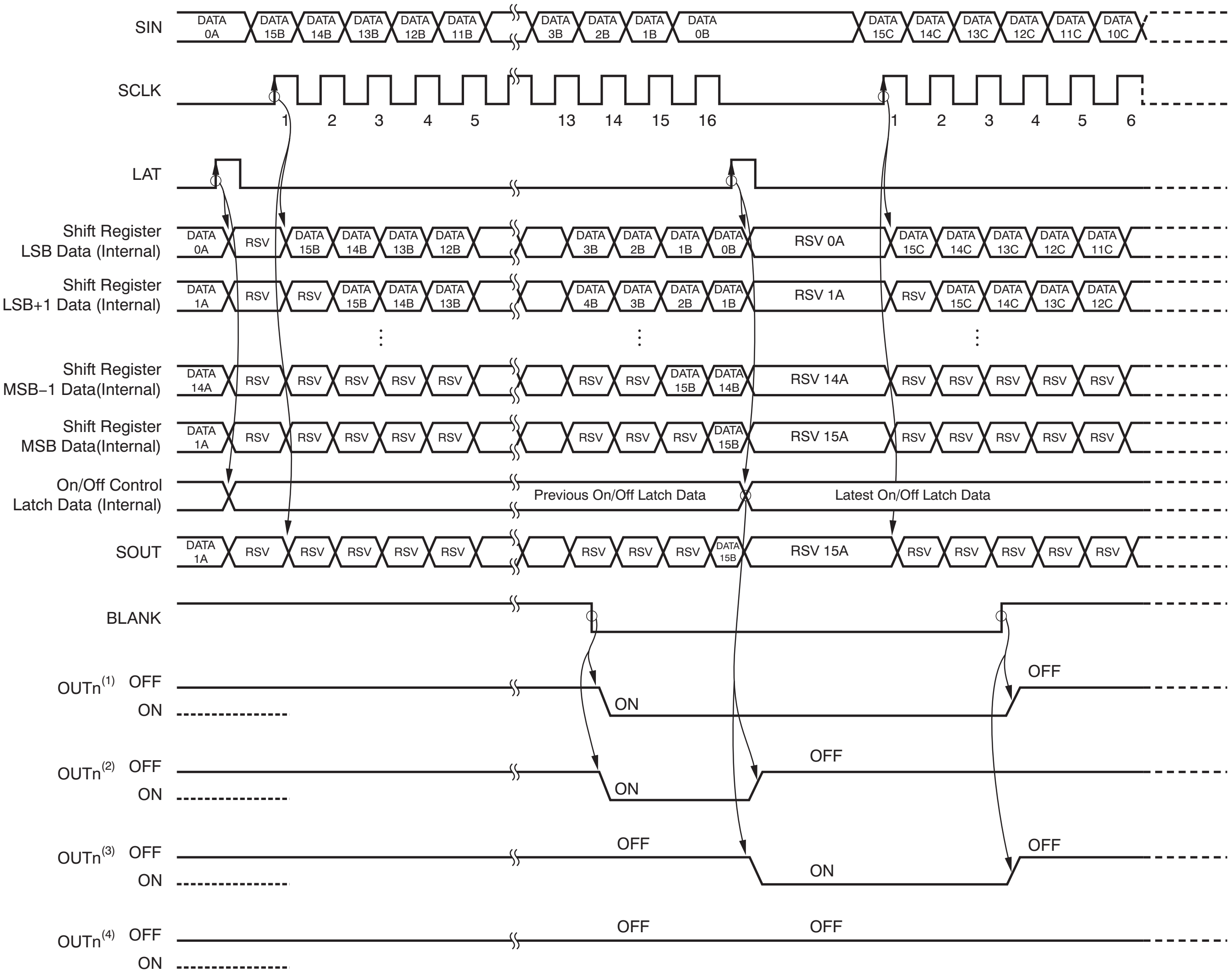

On/Off Control Shift Register (1 Bit × 16 Channels)
MSB
LSB
15
14
13
12
11
4
3
2
1
0
On/Off Data for OUT15
On/Off Data for OUT14
On/Off Data for OUT13
On/Off Data for OUT12
On/Off Data for OUT3
On/Off Data for OUT2
On/Off Data for OUT1
On/Off Data for OUT0
SOUT
SIN
SCLK
LAT
On/Off Control Data Latch (1 Bit × 16 Channels)
16 Bits
To Constant Current Driver Control Block

Figure 17. On/Off Control Shift Register and Latch Configuration


SIN
DATA 0A
DATA 15B
DATA 14B
DATA 13B
DATA 12B
DATA 11B
DATA 3B
DATA 2B
DATA 1B
DATA 0B
DATA 15C
DATA 14C
DATA 13C
DATA 12C
DATA 11C
DATA 10C
SCLK
1
2
3
4
5
13
14
15
16
1
2
3
4
5
6
LAT
Shift Register LSB Data (Internal)
RSV
RSV 0A
Shift Register LSB+1 Data (Internal)
DATA 1A
DATA 4B
RSV 1A
Shift Register MSB−1 Data(Internal)
DATA 14A
RSV 14A
Shift Register MSB Data(Internal)
RSV 15A
On/Off Control Latch Data (Internal)
Previous On/Off Latch Data
Latest On/Off Latch Data
SOUT
BLANK
OUTn(1)
OUTn(2)
OUTn(3)
OUTn(4)
OFF
ON

(1) On/off latched data are '1'.

(2) On/off latched data are changed from '1' to '0' at the second LAT signal.

(3) On/off latched data are changed from '0' to '1' at the second LAT signal.

(4) On/off latched data are '0'.

Figure 18. On/Off Control Operation

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (January 2010) to Revision A **Page**

- Changed SO-24 to SSOP-24/QSOP-24 in Package/Ordering Information table 2
- Changed SO-24 to SSOP-24/QSOP-24 in Dissipation Ratings table 2
- Changed SO-24 to SSOP-24/QSOP-24 in DBQ pinout 6

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Pea
TLC59281DBQ	ACTIVE	SSOP/QSOP	DBQ	24	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
TLC59281DBQR	ACTIVE	SSOP/QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
TLC59281RGE	PREVIEW			24		TBD	Call TI	Call TI
TLC59281RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
TLC59281RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.
information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all
lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable fo
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package,
the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retard
in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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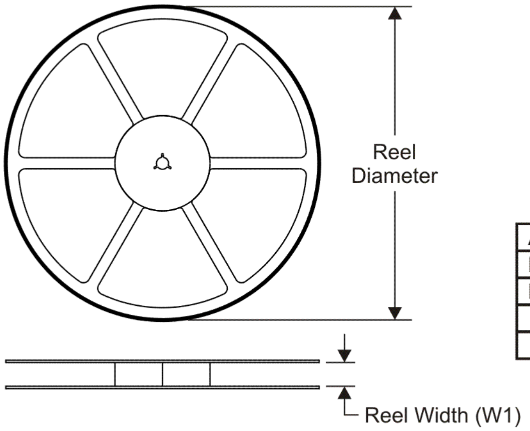
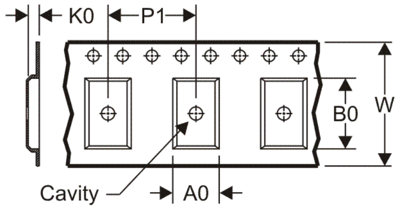
TAPE AND REEL INFORMATION

REEL DIMENSIONS

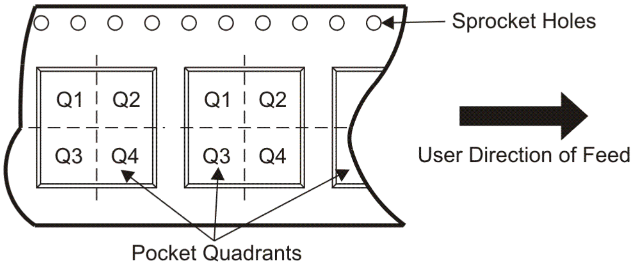

Reel
Diameter
Reel Width (W1)

TAPE DIMENSIONS


K0
P1
B0
W
Cavity
A0

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

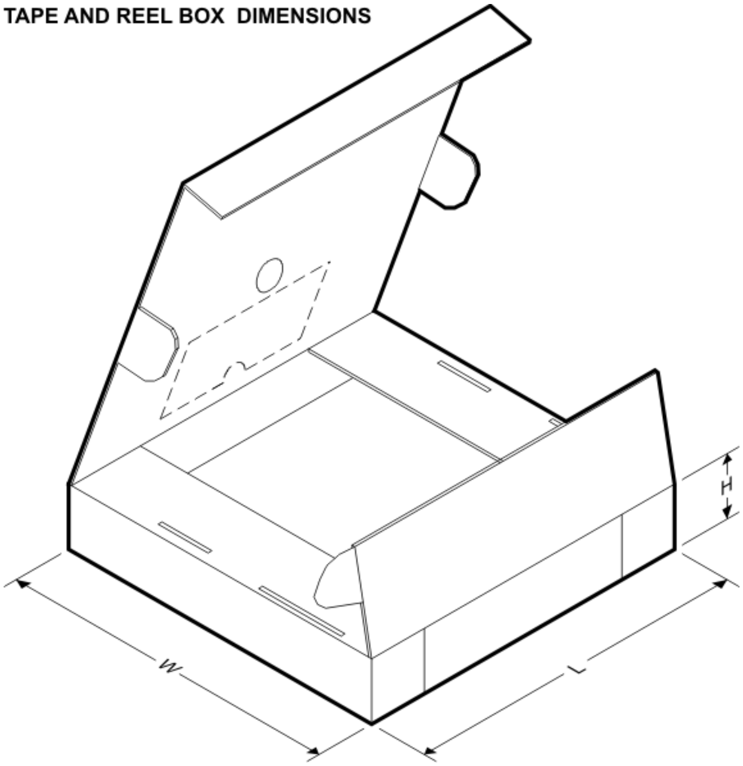
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


Sprocket Holes
Q1
Q2
Q3
Q4
Q1
Q2
Q3
Q4
User Direction of Feed
Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC59281DBQR	SSOP/ QSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC59281RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLC59281RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

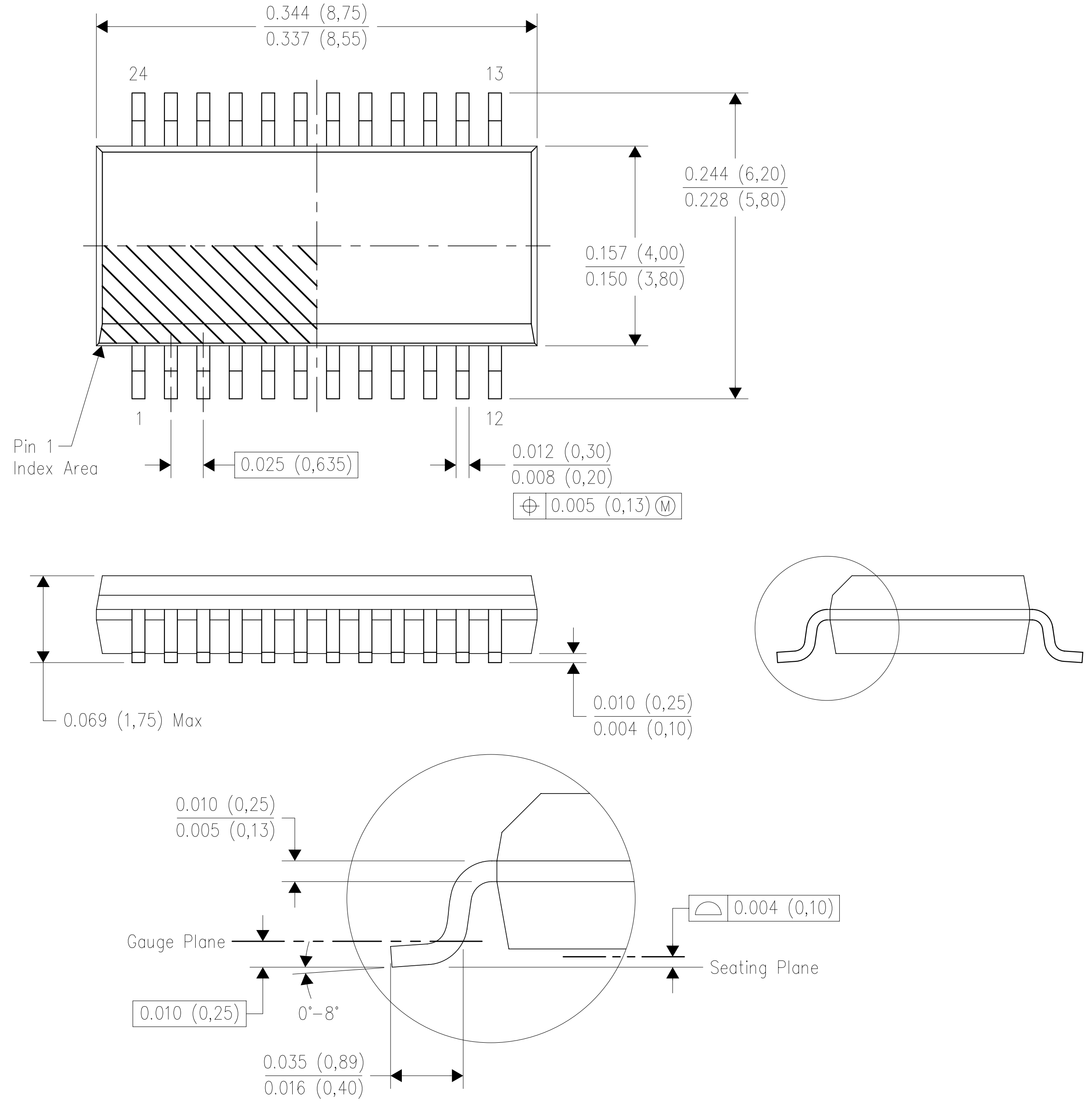
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC59281DBQR	SSOP/QSOP	DBQ	24	2500	346.0	346.0	33.0
TLC59281RGER	VQFN	RGE	24	3000	346.0	346.0	29.0
TLC59281RGET	VQFN	RGE	24	250	190.5	212.7	31.8

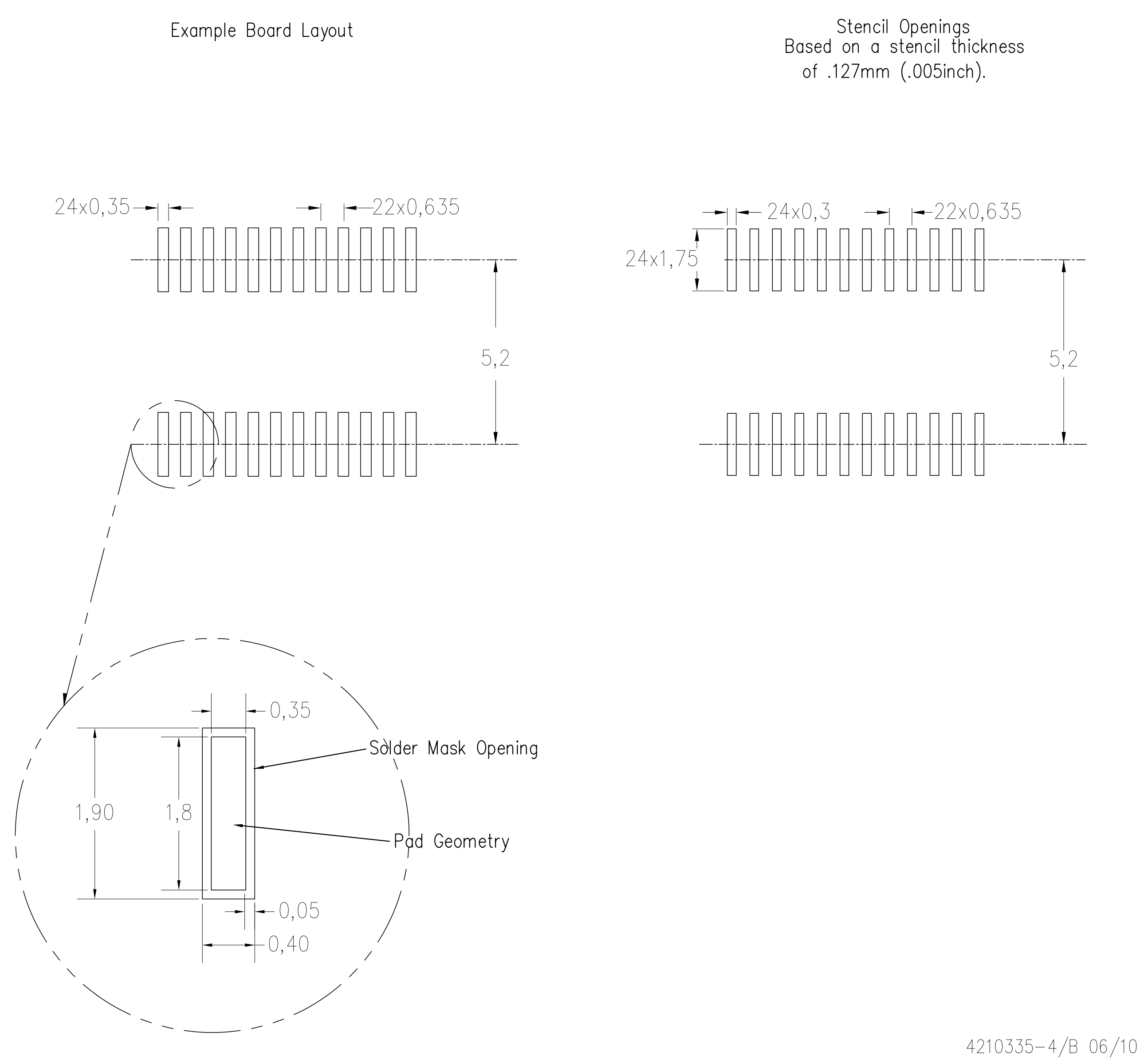
DBQ (R-PDSO-G24) PLASTIC SMALL-OUTLINE PACKAGE


0.344 (8,75)
0.337 (8,55)
24
13
0.244 (6,20)
0.228 (5,80)
0.157 (4,00)
0.150 (3,80)
1
12
Pin 1
Index Area
0.025 (0,635)
0.012 (0,30)
0.008 (0,20)
⌖ 0.005 (0,13) Ⓜ
0.069 (1,75) Max
0.010 (0,25)
0.004 (0,10)
0.010 (0,25)
0.005 (0,13)
Gauge Plane
0.004 (0,10)
Seating Plane
0.010 (0,25)
0°–8°
0.035 (0,89)
0.016 (0,40)

4073301-4/H 10/2008

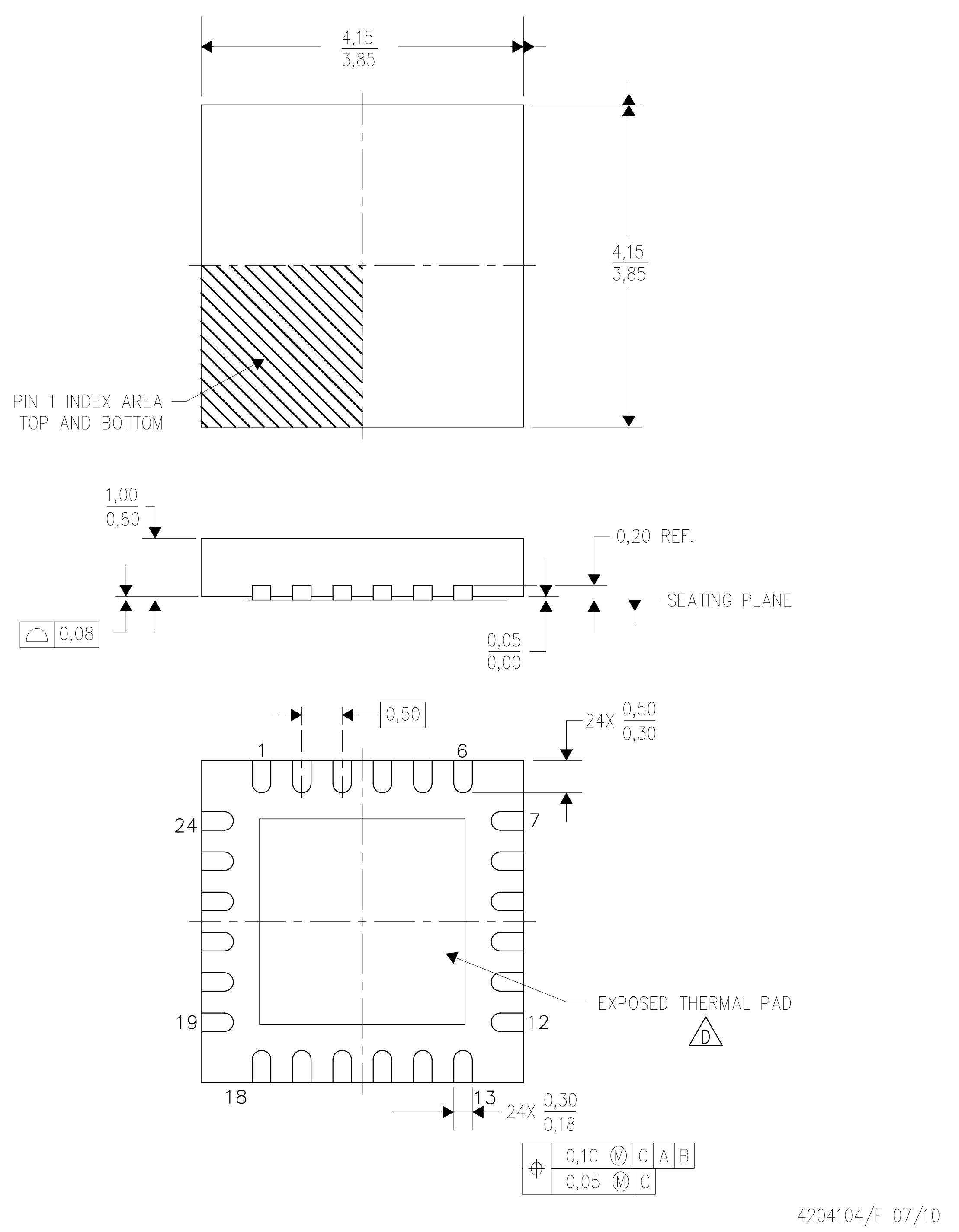
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
- D. Falls within JEDEC MO-137 variation AE.

DBQ (R–PDSO–G24) PLASTIC SMALL OUTLINE PACKAGE


Example Board Layout
Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).
24x0,35
22x0,635
5,2
24x0,3
22x0,635
24x1,75
5,2
0,35
Solder Mask Opening
1,90
1,8
Pad Geometry
0,05
0,40
4210335–4/B 06/10

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

RGE (S-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD



4,15
3,85
4,15
3,85
PIN 1 INDEX AREA
TOP AND BOTTOM
1,00
0,80
0,20 REF.
SEATING PLANE
0,08
0,05
0,00
0,50
24X 0,50
0,30
1
6
24
7
19
12
18
13
EXPOSED THERMAL PAD
D
24X 0,30
0,18
0,10 M C A B
0,05 M C
4204104/F 07/10

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No-Leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- E. Falls within JEDEC MO-220.

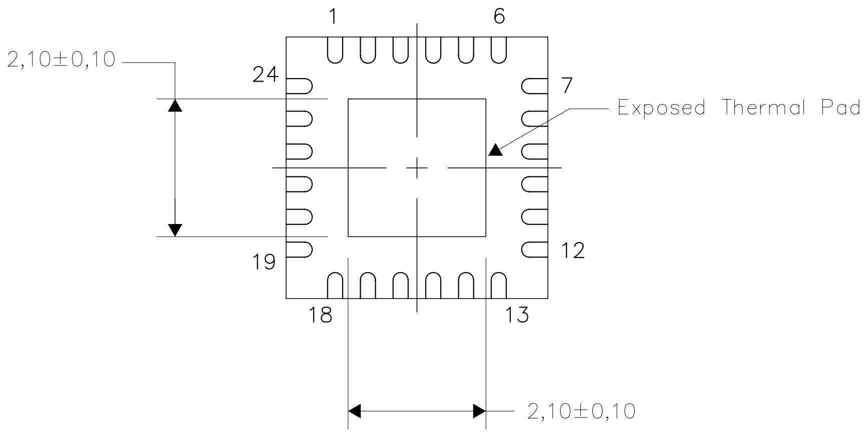
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206344–6/V 11/10

NOTES: A. All linear dimensions are in millimeters

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Logic	logic.ti.com	Industrial	www.ti.com/industrial
Power Mgmt	power.ti.com	Medical	www.ti.com/medical
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Space, Avionics & Defense	www.ti.com/space-avionics-defense
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video and Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless-apps

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