



LB11852FV

Monolithic Digital IC
For Fan Motor
Single-phase Full-wave Pre-driver
with Speed Control Function

Overview

The LB11852FV is a single-phase bipolar driving motor pre-driver with a speed control function based on speed feedback. With a small number of external parts, a highly efficient and very quiet variable-speed drive fan motor with low power consumption and high rotational accuracy can be implemented. The LB11852FV, integrated in a miniature package, is best suited for driving small fan motors requiring speed control.

Features

- Single-phase full-wave driving pre-driver
 - ⇒ With a PMOS-NMOS device used as the external power transistor, low saturation output and a single-phase full-wave drive enable a high-efficiency drive with low power consumption.
- Speed control circuit incorporated
 - ⇒ Compared with open-loop control, a closed-loop control function that uses speed feedback to control the speed makes it possible to improve the rotational speed accuracy and reduce the variations in the rotational speed caused by fluctuations in the supply voltage or load. The separately excited upper direct PWM method is featured as the variable speed system.
- Variable speed control is possible with external PWM input or analog voltage input
 - ⇒ The speed control input signal is compatible with PWM duty ratio and analog voltages.
- Soft start circuit incorporated
- Minimum speed setting pin
 - ⇒ The minimum speed can be set using an external resistor.
- Current limiting circuit incorporated
 - ⇒ Chopper type current limit at startup or lock.
- Reactive current cut circuit incorporated
 - ⇒ Reactive current before phase changeover is cut, ensuring highly silent and low power-consumption drive.
- Automatic resetting type constraint circuit incorporated
- FG (rotational speed detection) output

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Specifications

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Absolute Maximum Ratings at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|--|------------------------|---------------------------------|------------|------|
| V _{CC} pin maximum supply voltage | V _{CC} max | | 18 | V |
| OUTN pin maximum output current | I _{OUTN} max | | 20 | mA |
| OUTP pin maximum Sink current | I _{OUTP} max | | 20 | mA |
| OUT pin output withstand voltage | V _{OUT} max | | 18 | V |
| HB maximum output current | HB | | 10 | mA |
| CTL, C pin withstand voltage | CTL, C max | | 7 | V |
| CVI, LIM pin withstand voltage | CVI, LIM max | | 7 | V |
| RD/FG output pin output withstand voltage | FG max | | 19 | V |
| RD/FG output current | FG max | | 10 | mA |
| 5VREG pin maximum output current | I _{5VREG} max | | 10 | mA |
| Allowable power dissipation | P _d max | Mounted on a specified board *1 | 0.8 | W |
| Operating temperature | T _{opr} | | -30 to 95 | °C |
| Storage temperature | T _{stg} | | -55 to 150 | °C |

*1 Mounted on a specified board : 114.3mm×76.1mm×1.6mm, glass epoxy

*2 T_j max = 150°C. Use the device in a condition that the chip temperature does not exceed T_j = 150°C during operation.

Recommended Operating Conditions at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|------------------|------------------------|------------|------|
| V _{CC} supply voltage 1 | V _{CC1} | V _{CC} pin | 5.5 to 16 | V |
| V _{CC} supply voltage 2 | V _{CC2} | V _{CC} -5VREG | 4.5 to 5.5 | V |
| CTL input voltage range | V _{CTL} | | 0 to 5VREG | V |
| LIM input voltage range | V _{LIM} | | 0 to 5VREG | V |
| CVI input voltage range | V _{CVI} | | 0 to 5VREG | V |
| Hall input common phase input voltage range | V _{ICM} | | 0.2 to 3 | V |

Electrical Characteristics at Ta = 25°C, V_{CC} = 12V, unless otherwise specified

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---------------------------------------|--------------------|--|---------|-----------------------|----------------------|-------|
| | | | min | typ | max | |
| Circuit current | I _{CC1} | During drive | | 12 | 15 | mA |
| | I _{CC2} | During lock protection | | 12 | 15 | mA |
| 5VREG voltage | 5VREG | I _{5VREG} = 5mA | 4.8 | 5.0 | 5.2 | V |
| Current limiting voltage | V _{LIM} | | 190 | 210 | 230 | mV |
| CPWM pin H level voltage | V _{CRH} | | 2.8 | 3.0 | 3.2 | V |
| CPWM pin L level voltage | V _{CRL} | | 0.9 | 1.1 | 1.3 | V |
| CPWM pin charge current | I _{CPWM1} | V _{CPWM} = 0.5V | 24 | 30 | 36 | μA |
| CPWM pin discharge current | I _{CPWM2} | V _{CPWM} = 3.5V | 21 | 27 | 33 | μA |
| CPWM oscillation frequency | F _{PWM} | C = 220pF | | 30 | | kHz |
| CT pin H level voltage | V _{CTH} | | 2.8 | 3.0 | 3.2 | V |
| CT pin L level voltage | V _{CTL} | | 0.9 | 1.1 | 1.3 | V |
| CT pin charge current | I _{CT1} | V _{CT} = 2V | 1.6 | 2.0 | 2.5 | μA |
| CT pin discharge current | I _{CT2} | V _{CT} = 2V | 0.16 | 0.20 | 0.25 | μA |
| CT pin charge/discharge current ratio | R _{CT} | I _{CT1} /I _{CT2} | 8 | 10 | 12 | times |
| OUTN pin output H voltage | V _{ONH} | I _O = 10mA | | V _{CC} -0.85 | V _{CC} -1.0 | V |
| OUTN pin output L voltage | V _{ONL} | I _O = 10mA | | 0.9 | 1.0 | V |
| OUTP pin output L voltage | V _{OPL} | I _O = 10mA | | 0.5 | 0.65 | V |
| Hall input sensitivity | V _{HN} | I _N ⁺ , I _N ⁻ differential voltage (including offset and hysteresis) | | ±15 | ±25 | mV |

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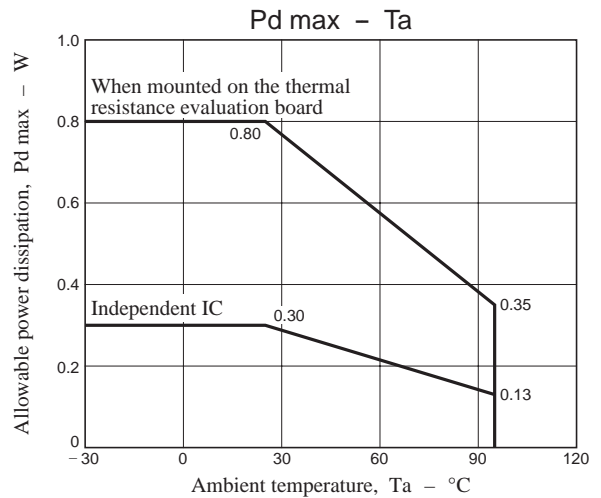
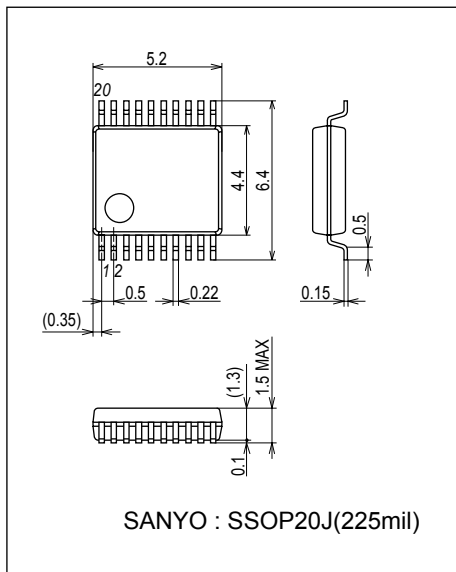
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| Parameter | Symbol | Conditions | Ratings | | | Unit |
|--|-------------|---------------------------|----------|----------|------|---------------|
| | | | min | typ | max | |
| FG output L voltage | V_{FGL} | $I_{FG} = 5\text{mA}$ | | 0.15 | 0.30 | V |
| FG pin leak current | I_{FGL} | $V_{FG} = 19\text{V}$ | | | 30 | μA |
| EO pin output H voltage | V_{EOH} | $I_{EO1} = -0.2\text{mA}$ | VREG-1.2 | VREG-0.8 | | V |
| EO pin output L voltage | V_{EOL} | $I_{EO1} = 0.2\text{mA}$ | | 0.8 | 1.1 | V |
| RC pin output H voltage | V_{RCH} | | 3.2 | 3.45 | 3.7 | V |
| RC pin output L voltage | V_{RCL} | | 0.7 | 0.8 | 1.05 | V |
| RC pin clamp voltage | V_{RCCLP} | | 1.3 | 1.5 | 1.7 | V |
| CTL pin input H voltage | V_{CTLH} | | 2.0 | | VREG | V |
| CTL pin input L voltage | V_{CTLL} | | 0 | | 1.0 | V |
| CTL pin input open voltage | V_{CTLO} | | VREG-0.5 | | VREG | V |
| CTL pin H input H current | I_{CTLH} | $V_{FGIN} = 5\text{VREG}$ | -10 | 0 | 10 | μA |
| CTL pin L input L current | I_{CTLL} | $V_{FGIN} = 0\text{V}$ | -120 | -90 | | μA |
| C pin output H voltage | V_{CH} | | VREG-0.3 | VREG-0.1 | | V |
| C pin output L voltage | V_{CL} | | 1.8 | 2.0 | 2.2 | V |
| LIM pin input bias current | I_{BLIM} | | -1 | | 1 | μA |
| LIM pin common phase input voltage range | V_{LIM} | | 2.0 | | VREG | V |
| SOFT pin charge current | I_{CSOFT} | | 1.0 | 1.3 | 1.6 | μA |
| SOFT pin operating voltage range | V_{ISOFT} | | 2.0 | | VREG | V |

Package Dimensions

unit : mm (typ)

3360



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Truth table

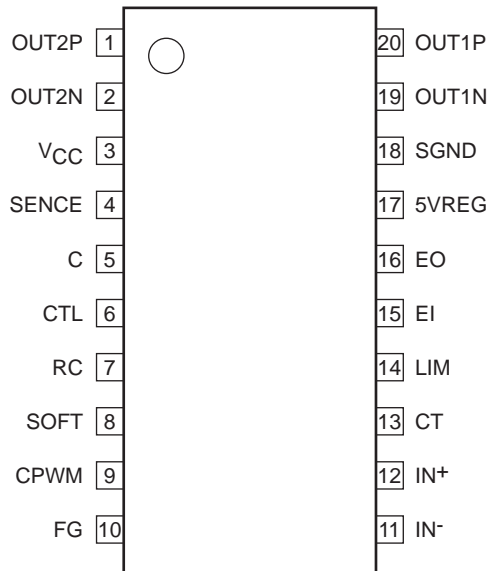
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 Lock protection CPWM = H

| IN ⁻ | IN ⁺ | CT | OUT1P | OUT1N | OUT2P | OUT2N | FG | Mode |
|-----------------|-----------------|----|-------|-------|-------|-------|-----|-----------------|
| H | L | L | L | L | OFF | H | L | OUT1 → 2 drive |
| L | H | | OFF | H | L | L | OFF | OUT2 → 1 drive |
| H | L | H | OFF | L | OFF | H | L | Lock protection |
| L | H | | OFF | H | OFF | L | OFF | |

Speed control CT = L

| EO | CPWM | IN ⁻ | IN ⁺ | OUT1P | OUT1N | OUT2P | OUT2N | Mode |
|----|------|-----------------|-----------------|-------|-------|-------|-------|-------------------|
| L | H | H | L | L | L | OFF | H | OUT1 → 2 drive |
| | | L | H | OFF | H | L | L | OUT2 → 1 drive |
| H | L | H | L | OFF | L | OFF | H | Regeneration mode |
| | | L | H | OFF | H | OFF | L | |

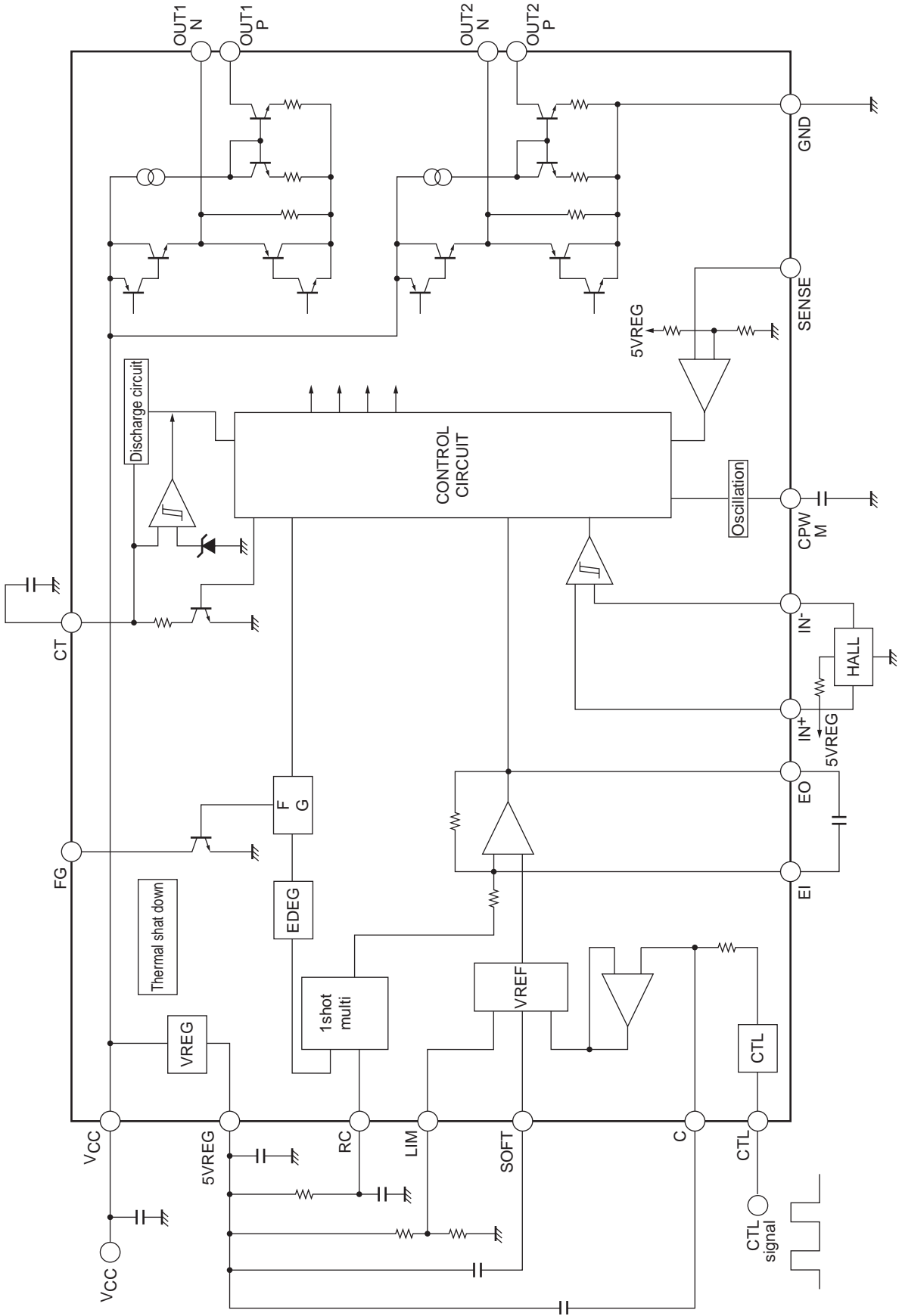
Pin Assignment



Top view

Block Diagram

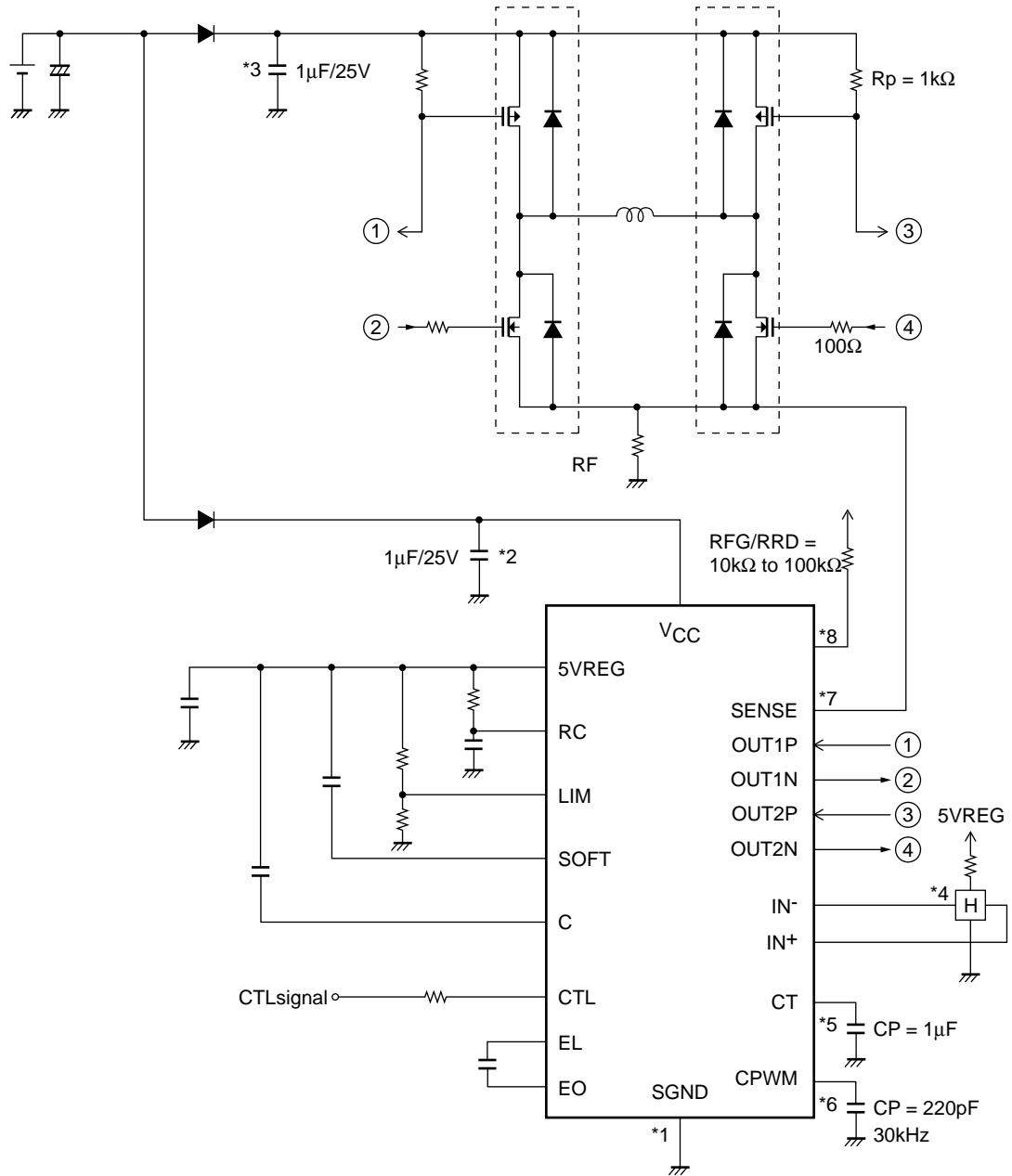
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Sample Application Circuit

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Description of Pre-driver Block

*1: [查询"LB11852FV"供应商](#) Power-GND wiring

The SGND is connected to the control circuit power supply system.

*2 : Power stabilization capacitor

For the power stabilization capacitor on the signal side, use a capacitor of 0.1 μ F or more. Connect the capacitor between VCC and GND with a thick and along the shortest possible route.

*3 : Power-side power stabilization capacitor

For the power-side power stabilization capacitor, use a capacitor of 1 μ F or more. Connect the capacitor between the power-side power supply and GND with a thick and along the shortest possible route.

*4 : IN⁺, IN⁻ pins

Hall signal input pins

Wiring should be short to prevent noise from being carried.

If noise is carried, insert a capacitor between the IN⁺ and IN⁻ pins.

The Hall input circuit functions as a comparator with hysteresis (15mV).

It also has a soft switch zone with ± 30 mV (input signal difference voltage).

It is also recommended that the Hall input level should be a minimum of 100mV (p-p).

*5 : CPWM pin

Pin to connect the capacitor used to generate the PWM basic frequency

Use of CP = 200pF causes oscillation at $f = 30$ kHz, which is the basic frequency of PWM.

As this is also used for the current limiter reset signal, a capacitor must be connected even if the speed is not going to be controlled.

*6 : CT pin

Pin to connect the capacitor used for lock detection

The constant-current charging and constant-current discharging circuits incorporated cause locking when the pin voltage reaches 3.0V, and releasing the lock protection when it drops to 1.0V.

Connect this pin to the GND when it is not to be used (locking not necessary).

*7 : SENSE pin

Current limiter detection pin

When the pin voltage exceeds 0.21V, the current limiter is activated, and operation enters lower regeneration mode.

Connect this pin to the GND when it is not to be used.

*8 : FG pin

Rotational speed detection pin

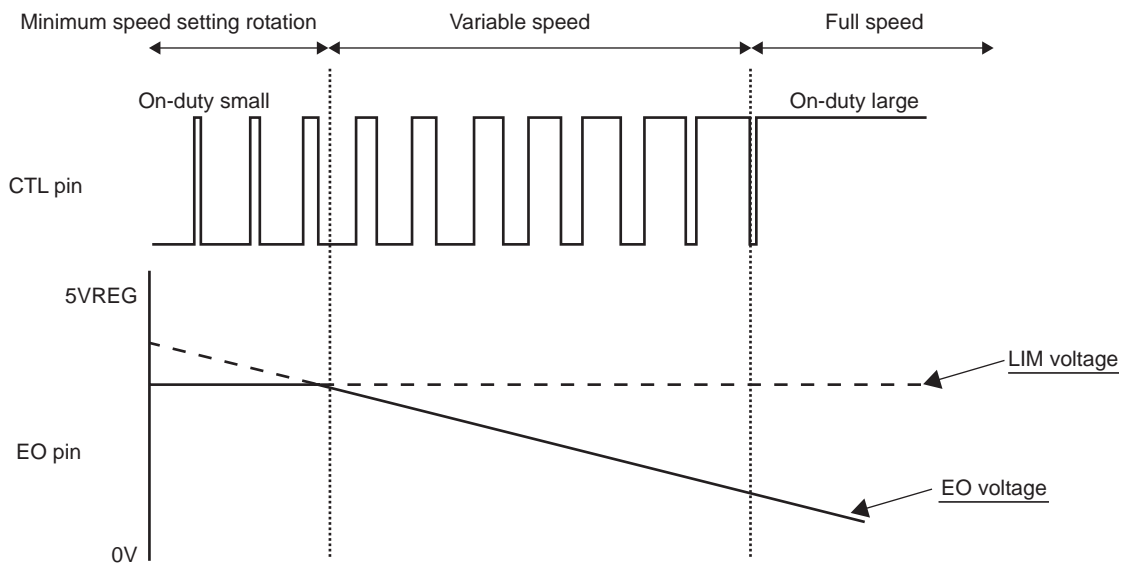
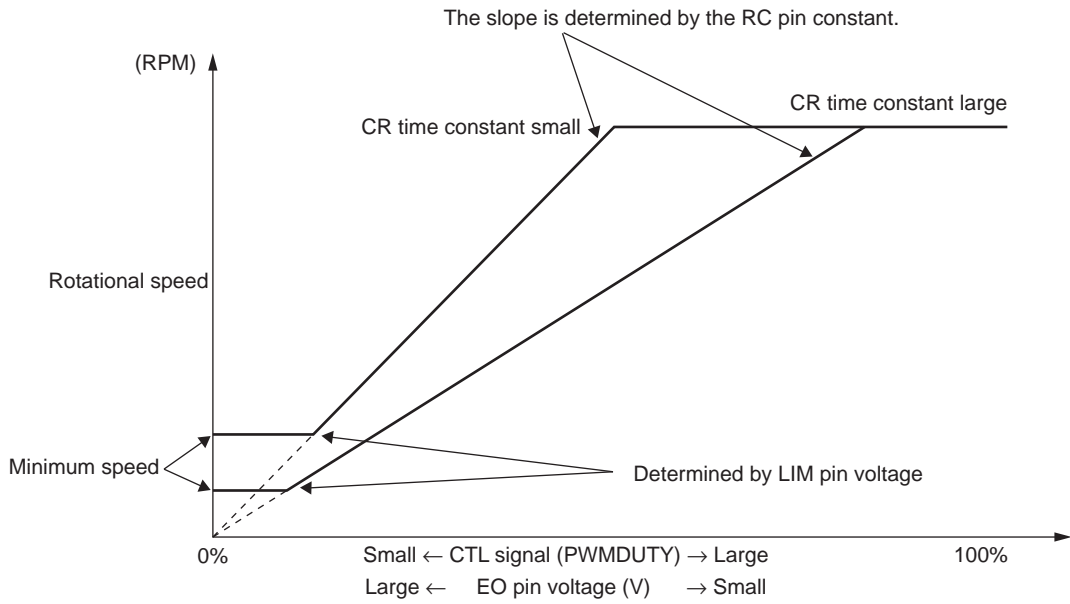
This is an open collector output that can detect the rotational speed using the FG output corresponding to the phase changeover.

Keep this pin open when it is not to be used.

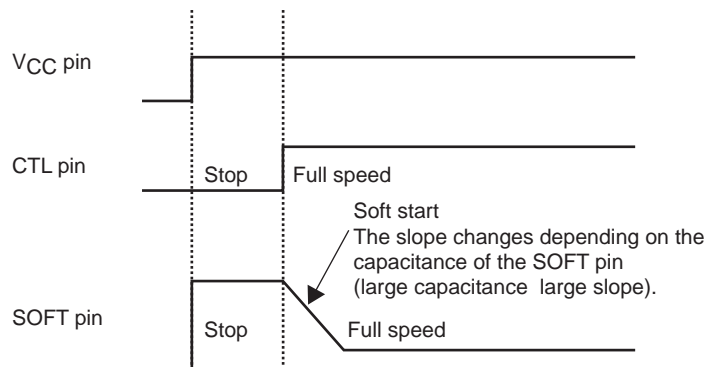
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Description of Speed Control Block

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Speed control diagram



2. Timing at startup (soft start)

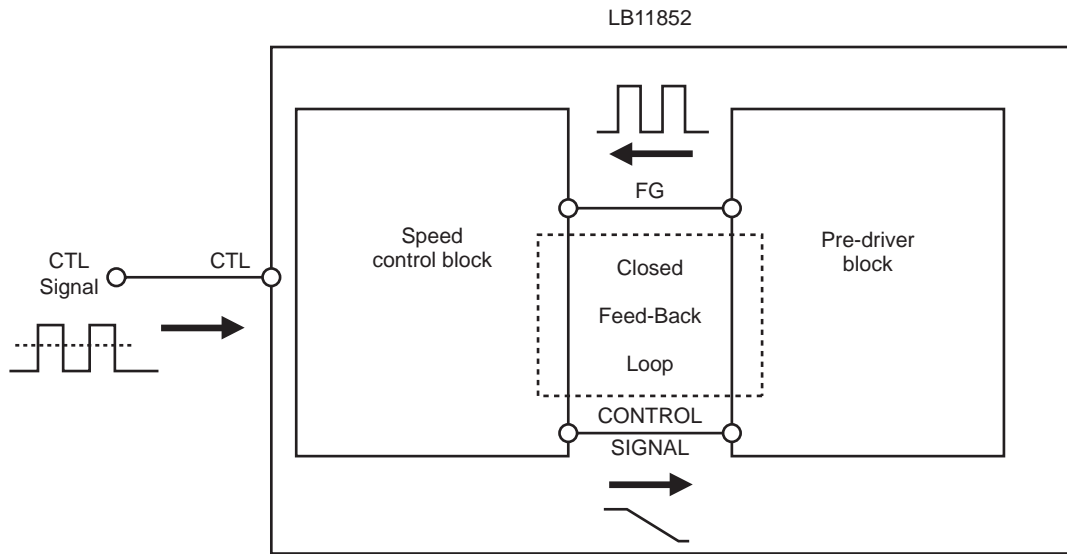


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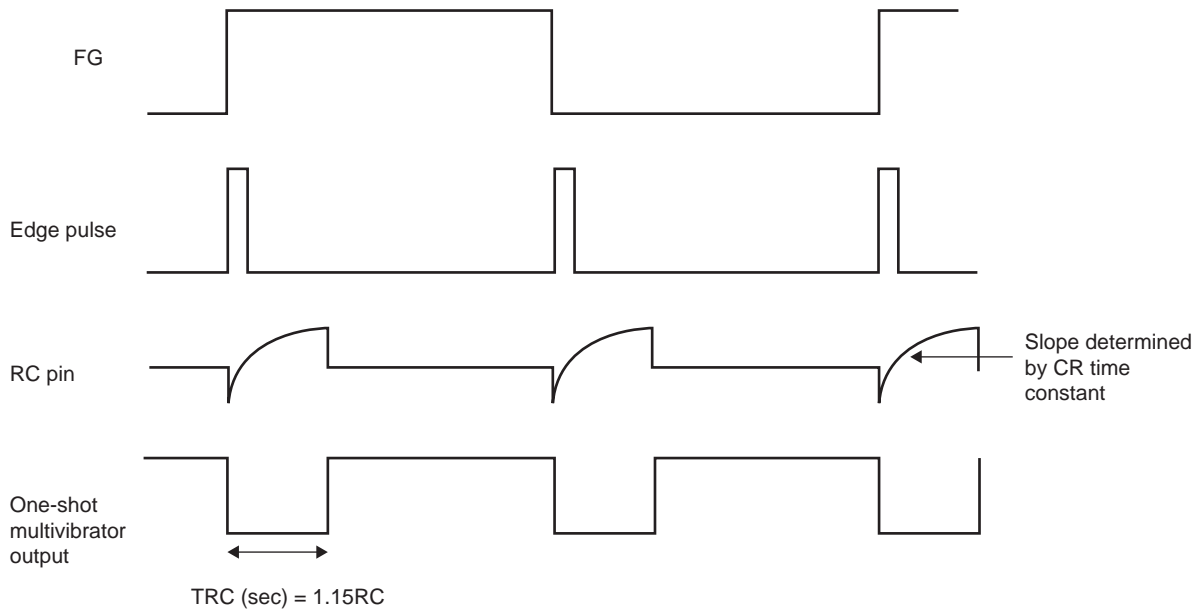
2. Supplementary description of operations

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By inputting the duty pulses, a feedback loop is formed inside the LB11852 IC to establish the FG period (rotational speed of the motor) that corresponds to the control voltage of the pulses.



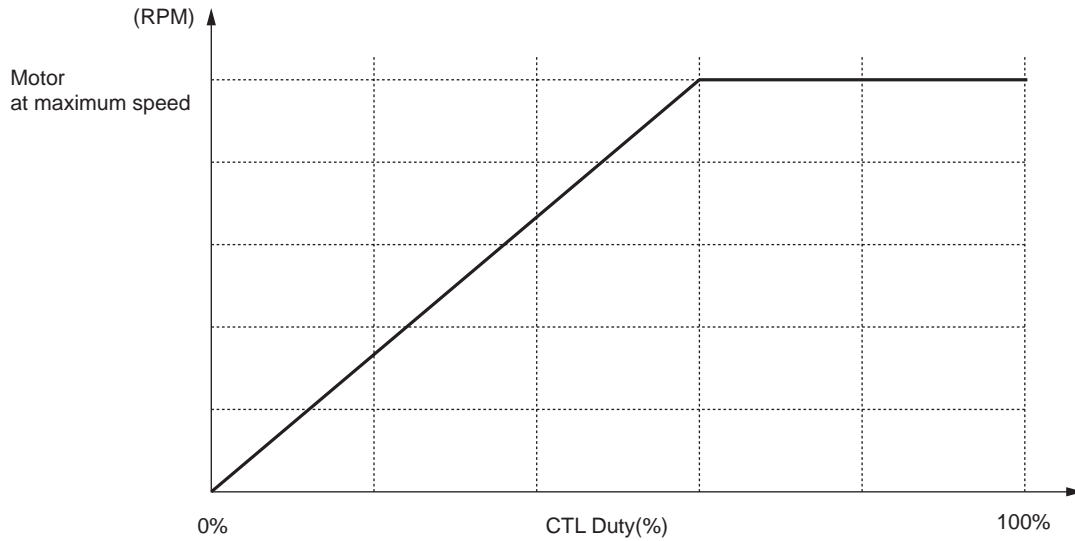
The operation inside the IC is as follows. Pulse signals are created from the edges of the FG signals as shown in the figure below, and using these signals as a reference, waveforms with a pulse width determined by the CR time constant are generated using a one-shot multivibrator. These pulse waveforms are then integrated to control the duty ratio of the pre-driver output as the control voltage.



By changing the pulse width as determined by the CR time constant, the VCTL versus rotational speed slope can be adjusted as shown in the speed control diagram in the previous section. However, since pulses that are determined by the CR time constant are used, the CR variations are output as-is as the speed control error.

4. Procedure for calculating the constant
(RC pin)
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The slope shown in the speed control diagram is determined by the constant of the RC pin.



- 1) Obtain the FG signal frequency f_{FG} (Hz) at the maximum rotational speed of the motor (with two FG pulses per rotation).

$$f_{FG} \text{ (Hz)} = 2 \text{ rpm}/60 \cdots (1)$$

- 2) Obtain the time constant of the components connected to the RC pin (use the duty ratio (example : 100% = 1.0 or 60% = 0.6) as the CTL duty ratio for achieving the maximum rotational speed).

$$R \times C = \text{Duty ratio}/(3.3 \times 1.1 \times f_{FG}) \cdots (2)$$

- 3) Obtain the resistance and the capacitance of the capacitor.

Based on the discharge capability of the RC pin, the capacitance of the capacitor which can be used is in the range of $0.01\mu\text{F}$ to $0.015\mu\text{F}$.

Therefore, obtain the appropriate resistance from the result of (2) above using the formula in (3) or (4) below.

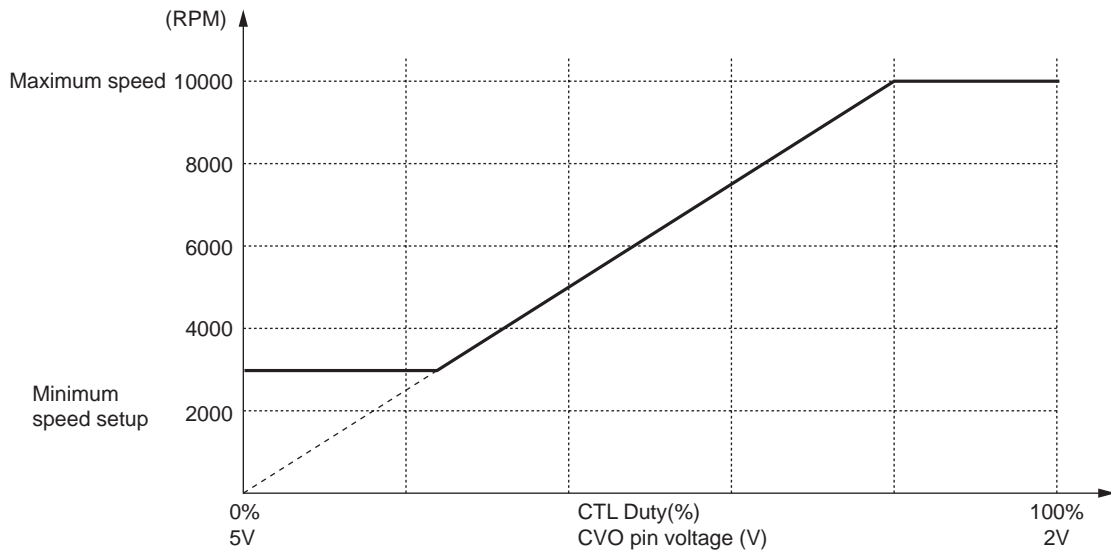
$$R = (R \times C)/0.01\mu\text{F} \cdots (3)$$

$$R = (R \times C)/0.015\mu\text{F} \cdots (4)$$

The temperature characteristics of the curve are determined by the temperature characteristics of the capacitor of the RC pin. To minimize the variations in the rotational speed caused by temperature, a capacitor with excellent temperature characteristics must be used.

(LIM pin)
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The minimum speed is determined by the voltage of the LIM pin.



1) Obtain the ratio of the minimum speed required to the maximum speed.

$$Ra = \text{Minimum/maximum speed} \cdots (1)$$

In the example shown in the figure above : $Ra = \text{minimum/maximum speed} = 3000/10000 = 0.3$

2) Obtain the product of the duty ratio at which the maximum speed is achieved and the value in formula (1).

$$Ca = \text{Maximum speed duty ratio} \times Ra \cdots (2)$$

In the example given : $Ca = \text{maximum speed duty ratio} \times Ra = 0.8 \times 0.3 = 0.24$

3) Obtain the required LIM pin voltage.

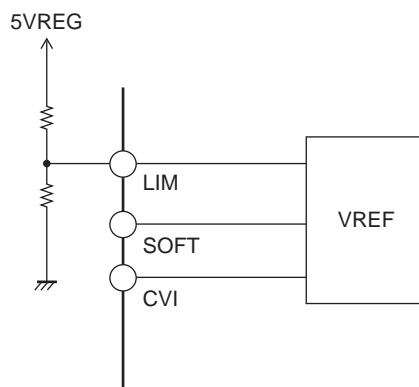
$$\text{LIM} = 5 - (3 \times Ca) \cdots (3)$$

In the example given : $\text{LIM} = 5 - (3 \times Ca) = 5 - (3 \times 0.24) \approx 4.3\text{V}$

4) Divide the resistance of 5VREG to generate the LIM voltage.

In the example given, the voltage is 4.3V so the resistance ratio is 1 : 6.

The resistance is 10kΩ between 5VREG and LIM and 62kΩ between LIM and GND.

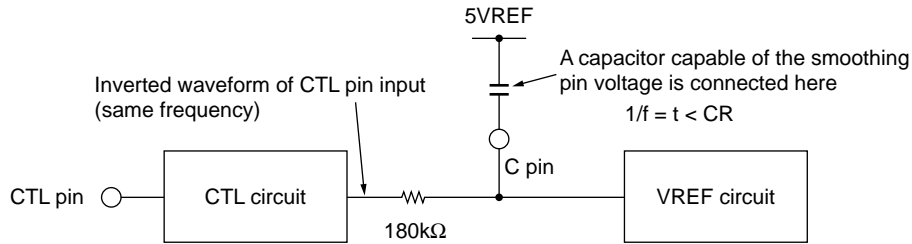


(C pin)
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In order to connect a capacitor capable of smoothing the pin voltage to the C pin, the correlation given in the following equation must be satisfied when f (Hz) serves as the input frequency of the CTL pin. (R is incorporated inside the IC, and it is $180\text{k}\Omega$ (typ.).)

$$1/f = t < CR$$

The higher the capacitance of the capacitor, the slower the response to changes in the input signals.



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