

Octal D-Type Flip-Flop With 3-State Outputs

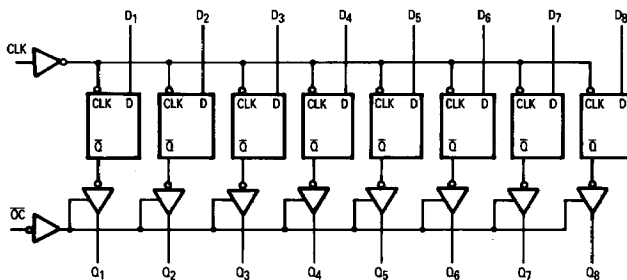
**ELECTRICALLY TESTED PER:
MPG54ALS574**

The 54ALS574 is a high-speed, low-power Octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable (OE) are common to all flip-flops. The 54ALS574 is manufactured using advanced Low Power Schottky technology and is compatible with all Motorola TTL families.

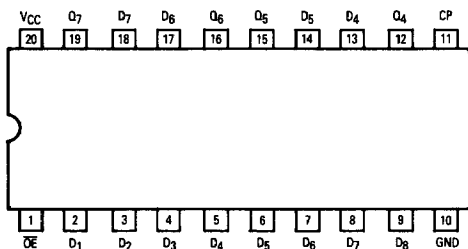
- Edge-Triggered D-Type Inputs
- Buffered Positive Edge Triggered Clock
- 3-State Output for Bus Interface
- Eight Latches in a Single Pack
- Hysteresis on Latch Enable
- Hysteresis on Clock Input to Improve Noise Margin
- Input Clamp Diodes Limit High Speed Termination Effects

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LOGIC DIAGRAM



CONNECTION DIAGRAM



H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = HIGH Impedance



AVAILABLE AS:

- 1) JAN: N/A
- 2) SMD: 8400101
- 3) 883C: 54ALS574/BXAJC

**X = CASE OUTLINE AS FOLLOWS:
 PACKAGE: CERDIP: R
 CERFLAT: S
 LCC: 2**



***Call Factory for latest update**

PIN ASSIGNMENTS

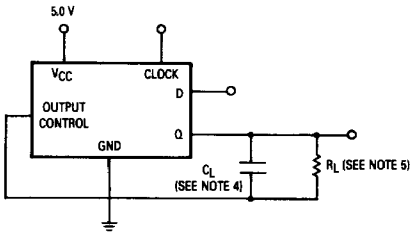
FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
OE	1	1	1	VCC
Q ₀	2	2	2	VCC
D ₀	3	3	3	VCC
D ₁	4	4	4	VCC
Q ₁	5	5	5	VCC
Q ₂	6	6	6	VCC
D ₂	7	7	7	VCC
D ₃	8	8	8	VCC
Q ₃	9	9	9	VCC
GND	10	10	10	GND
CP	11	11	11	VCC
Q ₄	12	12	12	OPEN
D ₄	13	13	13	OPEN
D ₅	14	14	14	OPEN
Q ₅	15	15	15	OPEN
Q ₆	16	16	16	OPEN
D ₆	17	17	17	OPEN
D ₇	18	18	18	OPEN
Q ₇	19	19	19	OPEN
VCC	20	20	20	VCC

**BURN-IN CONDITIONS:
 VCC = 5.0 V MIN/6.0 V MAX**

TRUTH TABLE

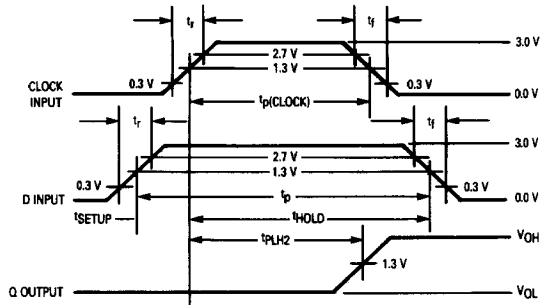
Inputs		Outputs	
D _n	CP	OE	Q _n
H		L	H
L		L	L
X	X	H	Z

SYNCHRONOUS SWITCHING TEST CIRCUIT (HIGH LEVEL DATA) AND WAVEFORMS

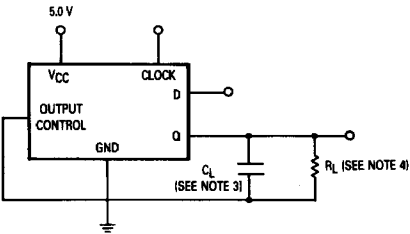


NOTES:

1. Clock input pulse characteristics:
 $t_r = t_f = 6.0 \pm 1.5$ ns, $t_p(\text{clock}) = 16.5$ ns, and PRR ≤ 1.0 MHz.
2. D input pulse characteristics:
 $t_r = t_f = 6.0 \pm 1.5$ ns, $t_{\text{setup}} = 15$ ns, $t_{\text{hold}} = 4.0$ ns, $t_p = 19$ ns, and PRR is 50% of the clock PRR.
3. For t_{MAX} , the clock input pulse characteristics are as follows:
 $t_r = t_f = 3.0$ ns, $t_p(\text{clock}) = 16.5$ ns, PRR = 30 MHz.
4. $C_L = 50$ pF $\pm 10\%$ (including jig and probe capacitance, without package in test fixture).
5. $R_L = 499 \Omega \pm 1.0\%$.
6. Voltage measurements are to be made with respect to network ground terminal.

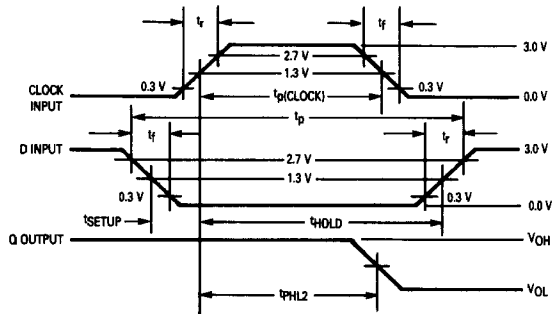


SYNCHRONOUS SWITCHING TEST CIRCUIT (LOW LEVEL DATA) AND WAVEFORMS

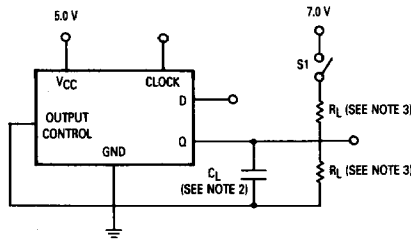


NOTES:

1. Clock input pulse characteristics:
 $t_r = t_f = 6.0 \pm 1.5$ ns, $t_p(\text{clock}) = 16.5$ ns, and PRR ≤ 1.0 MHz.
2. D input pulse characteristics:
 $t_r = t_f = 6.0 \pm 1.5$ ns, $t_{\text{setup}} = 15$ ns, $t_{\text{hold}} = 4.0$ ns, $t_p = 19$ ns, and PRR is 50% of the clock PRR.
3. $C_L = 50$ pF $\pm 10\%$ (including jig and probe capacitance, without package in test fixture).
4. $R_L = 499 \Omega \pm 1.0\%$.
5. Voltage measurements are to be made with respect to network ground terminal.



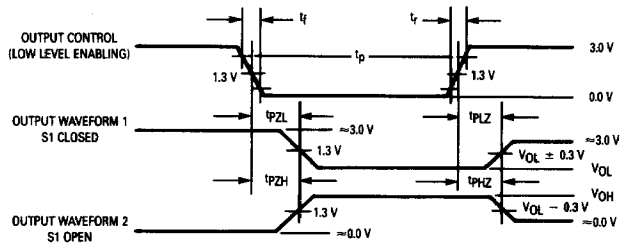
TRI-STATE SWITCHING TEST CIRCUIT AND WAVEFORMS



- NOTES:**
- Output control input characteristics:
 $t_r = t_f = 6.0 \pm 1.5$ ns, $t_p = 200$ ns, and PRR ≤ 1.0 MHz.
 - $C_L = 50$ pF $\pm 10\%$ (including jig and probe capacitance, without package in test fixture).
 - $R_L = 489 \Omega \pm 1.0\%$.
 - Voltage measurements are to be made with respect to network ground terminal.

SWITCH POSITIONS

Symbol	S1
tpZH	Open
tpZL	Closed
tPLZ	Closed
tpHZ	Closed



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Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		-55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
VOH	Logical "1" Output Voltage	2.4		2.4		2.4		V	V _{CC} = 4.5 V, I _{OH} = -1.0 mA, OE = 0.8 V, V _{IN} = 2.0 V, CP = (See Note 1), other inputs are open.
VOL	Logical "0" Output Voltage		0.4		0.4		0.4	V	V _{CC} = 4.5 V, I _{OL} = 12 mA, V _{IL} = 0.8 V, CP = (See Note 1), other inputs are open.
VIC	Input Clamping Voltage		-1.5					V	V _{CC} = 4.5 V, I _{IN} = -18 mA, other inputs are open.
I _{IH}	Logical "1" Input Current		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other inputs are open.
I _{IHH}	Logical "1" Input Current		100		100		100	μA	V _{CC} = 5.5 V, V _{IHH} = 7.0 V, other inputs are open.
I _{IL}	Logical "0" Input Current	0	-200	0	-200	0	-200	μA	V _{CC} = 5.5 V, V _{IN} = 0.4 V, other inputs are open.
I _O	Output Current	-15	-110	-15	-110	-15	-110	mA	V _{CC} = 5.5 V, V _{IN} = 5.5 V, other inputs are open, V _{OUT} = 2.25 V, CP = (See Note 1), OE = GND.
I _{IOZH}	Output Off Current High		20		20		20	μA	V _{CC} = 5.5 V, V _{IN} = 2.0 V, other inputs are open, V _{OUT} = 2.7 V, OE = 5.0 V, CP = (See Note 1).
I _{IOZL}	Output Off Current Low		-20		-20		-20	mA	V _{CC} = 5.5 V, V _{IN} = 0.8 V, other inputs are open, V _{OUT} = 0.4 V, OE = 5.0 V, CP = (See Note 1).
I _{CCH}	Power Supply Current Off		17		17		17	mA	V _{CC} = 5.5 V, V _{IN} = 5.0 V (all inputs), OE = GND, CP = (See Note 1).
I _{CCL}	Power Supply Current Off		23		23		23	mA	V _{CC} = 5.5 V, V _{IN} = GND (all inputs), CP = (See Note 1).
I _{CCZ}	Power Supply Current Off		27		27		27	mA	V _{CC} = 5.5 V, V _{IN} = GND (all inputs), OE = 5.0 V, CP = (See Note 1).
V _{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V _{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V _{CC} = 5.0 V, V _{INL} = 0.4 V, and V _{INH} = 2.5 V.

NOTES:

1. Apply  3.0 V, 5.5 V pulse prior to test.

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		-55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL2}	Propagation Delay /Data-Output CLK to Qn	4.0	12	4.0	15	4.0	15	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 499 Ω.
t _{PLH2}	Propagation Delay /Data-Output CLK to Qn	4.0	12	4.0	15	4.0	15	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 499 Ω.
t _{PLZ}	Propagation Delay /Data-Output OE to Qn	3.0	13	3.0	15	3.0	15	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 499 Ω.
t _{PHZ}	Propagation Delay /Data-Output OE to Qn	2.0	8.0	2.0	10	2.0	10	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 499 Ω.
t _{PZL}	Propagation Delay /Data-Output OE to Qn	4.0	18	4.0	21	4.0	21	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 499 Ω.
t _{PZH}	Propagation Delay /Data-Output OE to Qn	4.0	18	4.0	21	4.0	21	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 499 Ω.
f _{MAX}	Maximum Clock Frequency	30		30		30		MHz	V _{CC} = 5.0 V, C _L = 50 pF, (See Note 1).

NOTE:

1. f_{MAX} limit is the frequency of the input pulse. The output frequency shall be one half the input frequency.