4 A Synchronous Buck Power MOSFET Driver

The NCP5351 is a dual MOSFET gate driver optimized to drive the gates of both high−side and low−side Power MOSFETs in a Synchronous Buck converter. The NCP5351 is an excellent companion to multiphase controllers that do not have integrated gate drivers, such as ON Semiconductor's CS5323, CS5305 or CS5307. This architecture provides a power supply designer the flexibility to locate the gate drivers close to the MOSFETs.

The 4.0 A drive capability makes the NCP5351 ideal for minimizing switching losses in MOSFETs with large input capacitance. Optimized internal, adaptive nonoverlap circuitry further reduces switching losses by preventing simultaneous conduction of both MOSFETs.

The floating top driver design can accommodate MOSFET drain voltages as high as 25 V. Both gate outputs can be driven low, and supply current reduced to less than 25 μA, by applying a low logic level to the Enable (EN) pin. An undervoltage lockout function ensures that both driver outputs are low when the supply voltage is low, and a thermal shutdown function provides the IC with overtemperature protection.

The NCP5351 is pin−to−pin compatible with the SC1205 and is available in a standard SO−8 package and thermally enhanced QFN−10.

Features

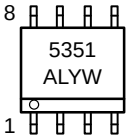
- 4.0 A Peak Drive Current
- Rise and Fall Times < 15 ns Typical into 6000 pF
- Propagation Delay from Inputs to Outputs < 20 ns
- Adaptive Nonoverlap Time Optimized for Large Power MOSFETs
- Floating Top Driver Accommodates Applications Up to 25 V
- Undervoltage Lockout to Prevent Switching when the Input Voltage is Low
- Thermal Shutdown Protection Against Overtemperature
- < 1.0 mA Quiescent Current − Enabled
- 25 μA Quiescent Current − Disabled
- Internal TG to DRN Pulldown Resistor Prevents HV Supply−Induced Turn On of High−Side MOSFET

ON Semiconductor®

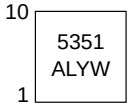
http://onsemi.com

MARKING DIAGRAMS

SO−8
D SUFFIX
CASE 751



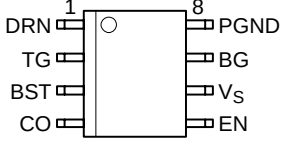
QFN−10
MN SUFFIX
CASE 485C



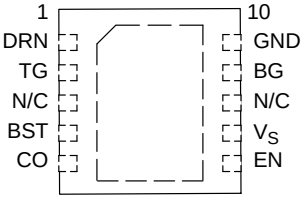
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

PIN CONNECTIONS

SO−8



QFN−10



ORDERING INFORMATION

Device	Package	Shipping†
NCP5351D	SO−8	98 Units/Rail
NCP5351DR2	SO−8	2500 Tape & Reel
NCP5351MNR2	QFN−10	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

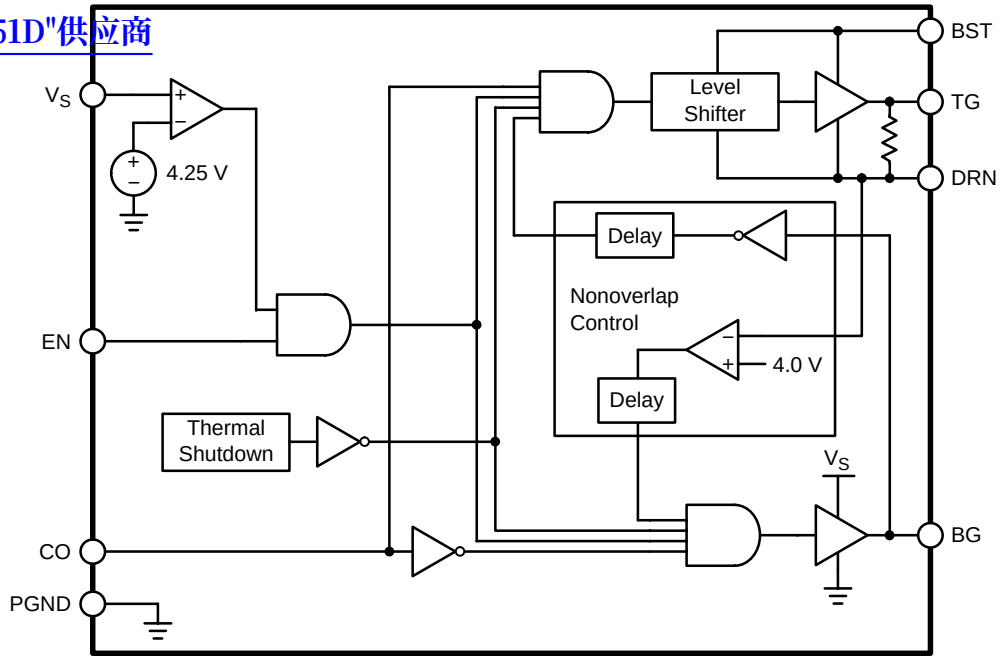


Figure 1. Block Diagram

Table 1. Input−Output Truth Table

EN	CO	DRN	TG	BG
L	X	X	L	L
H	L	< 3.0 V	L	H
H	H	< 3.0 V	H	L
H	L	> 5.0 V	L	L
H	H	> 5.0 V	H	L

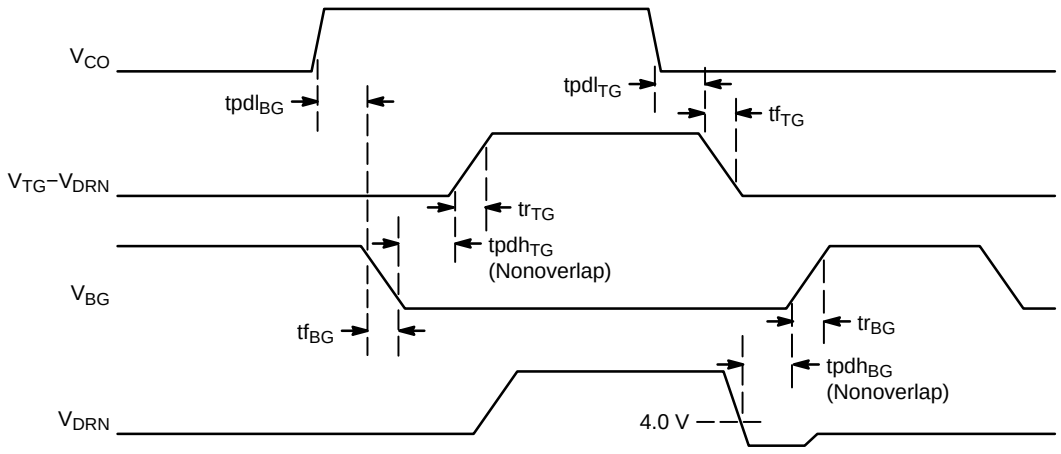


Figure 2. Timing Diagram

PACKAGE PIN DESCRIPTION

Pin Number		Pin Symbol	Description
SO−8	QFN−10		
1	1	DRN	The switching node common to the high and low−side FETs. The high−side (TG) driver and supply (BST) are referenced to this pin.
2	2	TG	Driver output to the high−side MOSFET gate.
3	4	BST	Bootstrap supply voltage input. In conjunction with a Schottky diode to V_S, a 0.1 μF to 1.0 μF ceramic capacitor connected between BST and DRN develops supply voltage for the high−side driver (TG).
4	5	CO	Logic level control input produces complementary output states − no inversion at TG; inversion at BG.
−	3, 8	N/C	Not Connected.
5	6	EN	Logic level enable input forces TG and BG low, and supply current to 10 μA when EN is low.
6	7	V_S	Power supply input. A 0.1 μF to 1.0 μF ceramic capacitor should be connected from this pin to PGND.
7	9	BG	Driver output to the low−side (synchronous rectifier) MOSFET gate.
8	−	PGND	Ground.
−	10	GND	Ground.

MAXIMUM RATINGS

Rating	Value	Unit
Operating Junction Temperature, T_J	Internally Limited	°C
Package Thermal Resistance: SO−8 Junction−to−Case, $R_{\theta JC}$ Junction−to−Ambient, $R_{\theta JA}$	 45 165	 °C/W °C/W
Storage Temperature Range, T_S	−65 to 150	°C
Lead Temperature Soldering: Reflow: (SMD styles only) (Note 1)	230 peak	°C
MSL Rating	1	−

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

1. 60 seconds maximum above 183°C.

MAXIMUM RATINGS

Pin Symbol	Pin Name	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
V_S	Main Supply Voltage Input	6.3 V	−0.3 V	NA	4.0 A Peak (< 100 μs) 250 mA DC
BST	Bootstrap Supply Voltage Input	25 V wrt/PGND 6.3 V wrt/DRN	−0.3 V wrt/DRN	NA	4.0 A Peak (< 100 μs) 250 mA DC
DRN	Switching Node (Bootstrap Supply Return)	25 V	−1.0 V DC −5.0 V for 100 ns −6.0 V for 20 ns	4.0 A Peak (< 100 μs) 250 mA DC	NA
TG	High−Side Driver Output (Top Gate)	25 V wrt/PGND 6.3 V wrt/DRN	−0.3 V wrt/DRN	4.0 A Peak (< 100 μs) 250 mA DC	4.0 A Peak (< 100 μs) 250 mA DC
BG	Low−Side Driver Output (Bottom Gate)	6.3 V	−0.3 V	4.0 A Peak (< 100 μs) 250 mA DC	4.0 A Peak (< 100 μs) 250 mA DC
CO	TG & BG Control Input	6.3 V	−0.3 V	1.0 mA	1.0 mA
EN	Enable Input	6.3 V	−0.3 V	1.0 mA	1.0 mA
PGND	Ground	0 V	0 V	4.0 A Peak (< 100 μs) 250 mA DC	NA

NOTE: All voltages are with respect to PGND except where noted.

ELECTRICAL CHARACTERISTICS ($0°C < T_J < 125°C$; $V_S = 5.0$ V; 4.0 V $< V_{BST} < 25$ V; $V_{EN} = V_S$; unless otherwise noted)

Parameter	Test Conditions	Min	Typ	Max	Unit
DC OPERATING SPECIFICATIONS					
POWER SUPPLY					
V_S Quiescent Current, Operating	V_{CO} = 0 V, 4.5 V; No output switching	−	1.0	−	mA
V_{BST} Quiescent Current, Operating	V_{CO} = 0 V, 4.5 V; No output switching	−	50	−	μA
Quiescent Current, Non−Operating	V_{EN} = 0 V; V_{CO} = 0 V, 4.5 V	−	−	25	μA
Undervoltage Lockout					
Start Threshold	CO = 0 V	4.05	4.25	4.48	V
Hysteresis	CO = 0 V	−	275	−	mV
CO INPUT CHARACTERISTICS					
High Threshold	−	2.0	−	−	V
Low Threshold	−	−	−	0.8	V
Input Bias Current	$0 < V_{CO} < V_S$	−	0	1.0	μA
EN INPUT CHARACTERISTICS					
High Threshold	Both outputs respond to CO	2.0	−	−	V
Low Threshold	Both outputs are low, independent of CO	−	−	0.8	V
Input Bias Current	$0 < V_{EN} < V_S$	−	0	10	μA
THERMAL SHUTDOWN					
Overtemperature Trip Point	−	−	170	−	°C
Hysteresis	−	−	30	−	°C
HIGH−SIDE DRIVER					
Peak Output Current	−	−	4.0	−	A
Output Resistance (Sourcing)	Duty Cycle < 2.0%, Pulse Width < 100 μs, T_J = 125°C, $V_{BST} - V_{DRN}$ = 4.5 V, V_{TG} = 4.0 V + V_{DRN}	−	0.5	−	Ω
Output Resistance (Sinking)	Duty Cycle < 2.0%, Pulse Width < 100 μs, T_J = 125°C, $V_{BST} - V_{DRN}$ = 4.5 V, V_{TG} = 0.5 V + V_{DRN}	−	0.42	−	Ω
LOW−SIDE DRIVER					
Peak Output Current	−	−	4.0	−	A
Output Resistance (Sourcing)	Duty Cycle < 2.0%, Pulse Width < 100 μs, T_J = 125°C, V_S = 4.5 V, V_{BG} = 4.0 V	−	0.6	−	Ω
Output Resistance (Sinking)	Duty Cycle < 2.0%, Pulse Width < 100 μs, T_J = 125°C, V_S = 4.5 V, V_{BG} = 0.5 V	−	0.42	−	Ω

ELECTRICAL CHARACTERISTICS (continued) (0°C < T_J < 125°C; V_S = 5.0 V; 4.0 V < V_{BST} < 25 V; V_{EN} = V_S, C_{LOAD} = 5.7 nF; unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
AC OPERATING SPECIFICATIONS						
HIGH−SIDE DRIVER						
Rise Time	tr_{TG}	$V_{BST} - V_{DRN}$ = 5.0 V, T_J = 125°C	−	8.0	16	ns
Fall Time	tf_{TG}	$V_{BST} - V_{DRN}$ = 5.0 V, T_J = 125°C	−	14	21	ns
Propagation Delay Time, TG Going High (Nonoverlap Time)	$tpdh_{TG}$	$V_{BST} - V_{DRN}$ = 5.0 V, T_J = 125°C	30	45	60	ns
Propagation Delay Time, TG Going Low	$tpdl_{TG}$	$V_{BST} - V_{DRN}$ = 5.0 V, T_J = 125°C	−	18	37	ns
LOW−SIDE DRIVER						
Rise Time	tr_{BG}	T_J = 125°C	−	10	15	ns
Fall Time	tf_{BG}	T_J = 125°C	−	12	20	ns
Propagation Delay Time, BG Going High (Non−Overlap Time)	$tpdh_{BG}$	T_J = 125°C	25	55	80	ns
Propagation Delay Time, BG Going Low	$tpdl_{BG}$	T_J = 125°C	−	10	18	ns
UNDERVOLTAGE LOCKOUT						
V_S Rising	$tpdh_{UVLO}$	EN = V_S, CO = 0 V, dV_S/dt > 1.0 V/μs, from 4.0 V to 4.5 V, time to BG > 1.0 V, T_J = 125°C	−	30	−	μs
V_S Falling	$tpdl_{UVLO}$	EN = V_S, CO = 0 V, dV_S/dt < −1.0 V/μs, from 4.5 V to 4.0 V, time to BG < 1.0 V, T_J = 125°C	−	500	−	μs

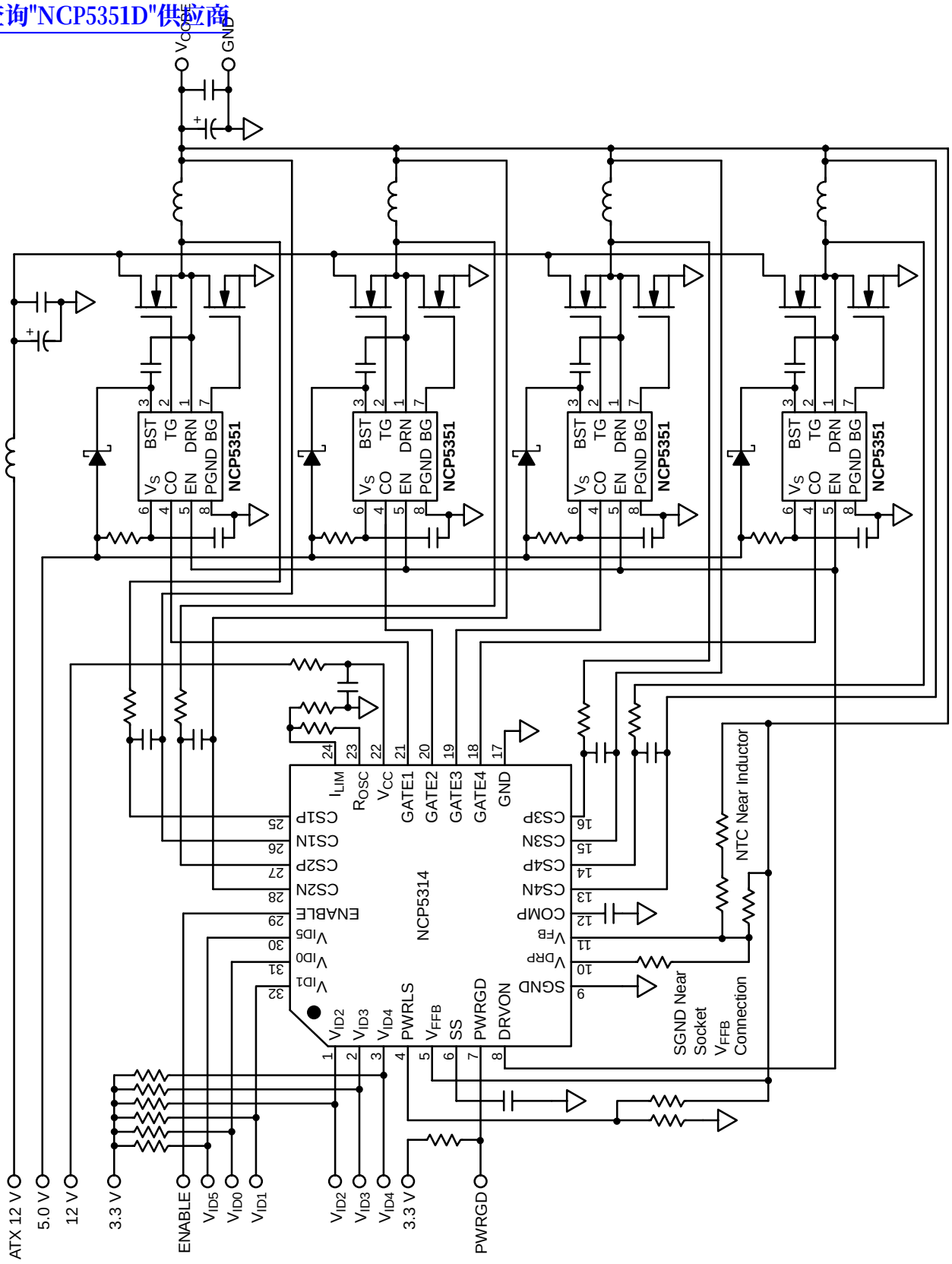


Figure 3. Application Diagram

APPLICATIONS INFORMATION

Theory Of Operation

Enable Pin

The Enable Pin (EN) is controlled by a logic level input. With a logic level high on the EN pin, the output states of the drivers are controlled by applying a logic level voltage to the CO pin. With a logic level low both gates are forced low. By bringing both gates low when disabling, the output voltage is prevented from ringing below ground, which could potentially cause damage to the microprocessor or the device being powered.

Undervoltage Lockout

The TG and BG are held low until V_S reaches 4.25 V during startup. The CO pin takes control of the gates' states when the V_S threshold is exceeded. If V_S decreases 300 mV below threshold, the output gate will be forced low and remain low until V_S rises above startup threshold.

Adaptive Nonoverlap

The Adaptive Nonoverlap prevents a condition where the top and bottom MOSFETs conduct at the same time and short the input supply. When the top MOSFET is turning off, the drain (switch node) is sampled and the BG is disabled for a fixed delay time ($tpdh_{BG}$) after the drain drops below 4 V, thus eliminating the possibility of shoot−through. When the bottom MOSFET is turning off, TG is disabled for a fixed delay ($tpdh_{TG}$) after BG drops below 2.0 V. (See Figure 2 for complete timing information).

Layout Guidelines

When designing any switching regulator, the layout is very important for proper operation. The designer should follow some simple layout guidelines when incorporating gate drivers in their designs. Gate drives experience high di/dt during switching and the inductance of gate drive traces should be minimized. Gate drive traces should be kept as short and wide as practical and should have a return path directly below the gate trace. The use of a ground plane is a desirable way to return ground signals. Also, component location will make a difference. The boost and the V_S capacitor are the most critical and should be placed as close as possible to the driver IC pins, as shown in Figure 4(a), C21 and C17.

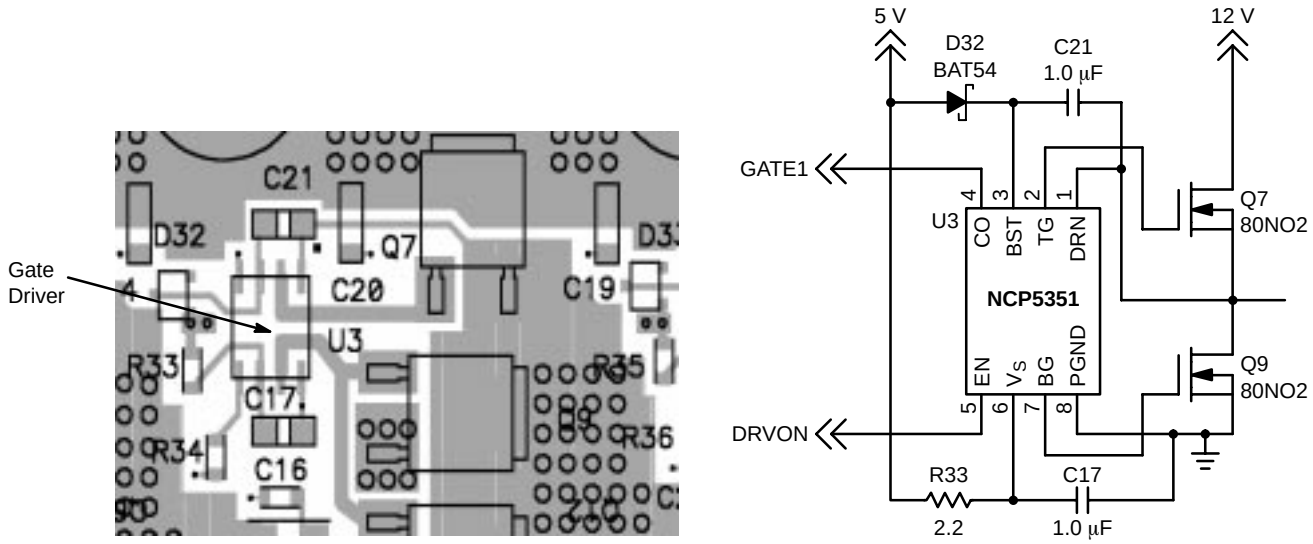
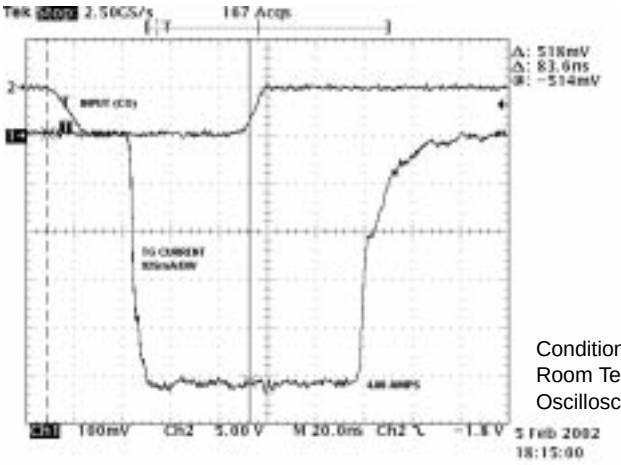
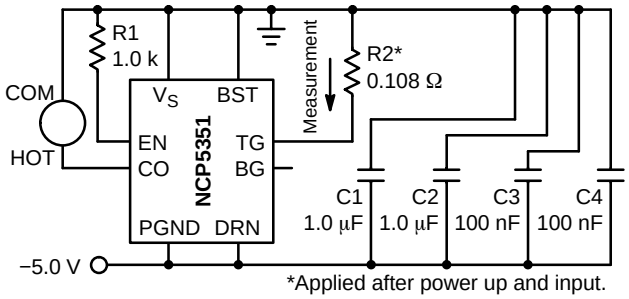


Figure 4. Proper Layout (a), Component Selection (b)

TYPICAL PERFORMANCE CHARACTERISTICS





Conditions: BST − DRN = 5.0 V;
Room Temperature;
Oscilloscope referenced to V_S (5.0 V).

Figure 5. Top Gate Sinking Current from 0.108 Ω

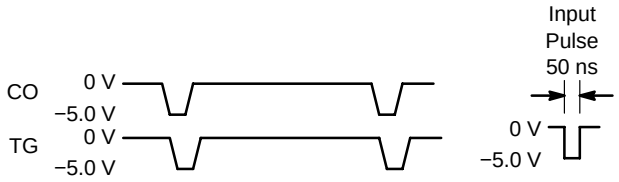
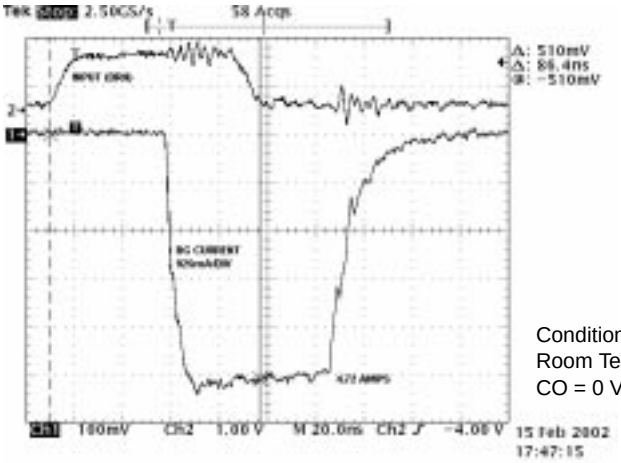
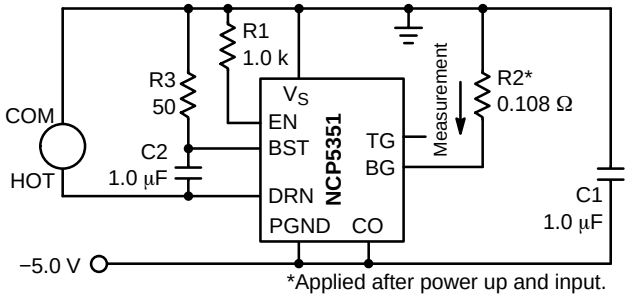


Figure 6. Top Gate Sinking





Conditions: V_S = 5.0 V;
Room Temperature;
CO = 0 V.

Figure 7. Bottom Gate Sinking Current from 0.108 Ω

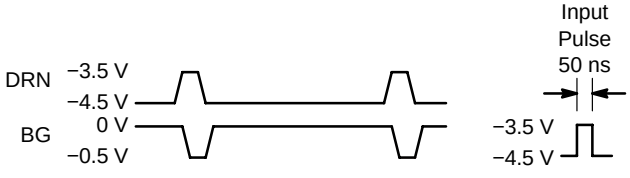
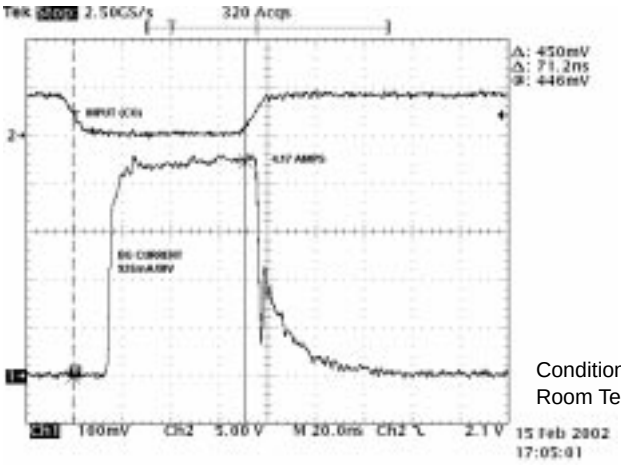
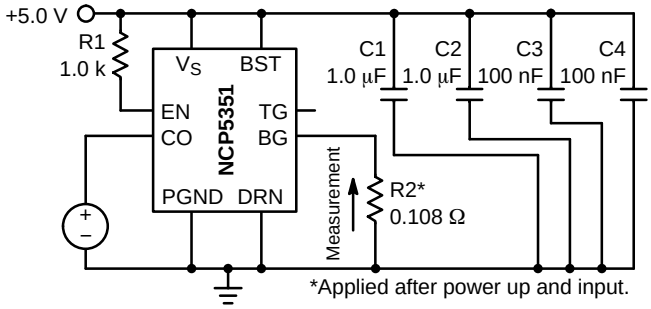


Figure 8. Bottom Gate Sinking

TYPICAL PERFORMANCE CHARACTERISTICS





Conditions: V_S = 5.0 V;
Room Temperature; DRN = 0 V.

Figure 9. Bottom Gate Sourcing Current into 0.108 Ω

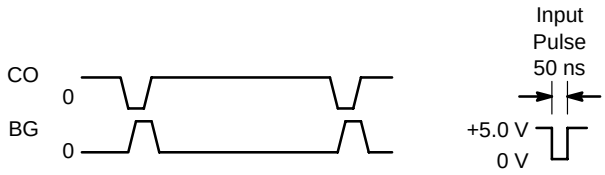
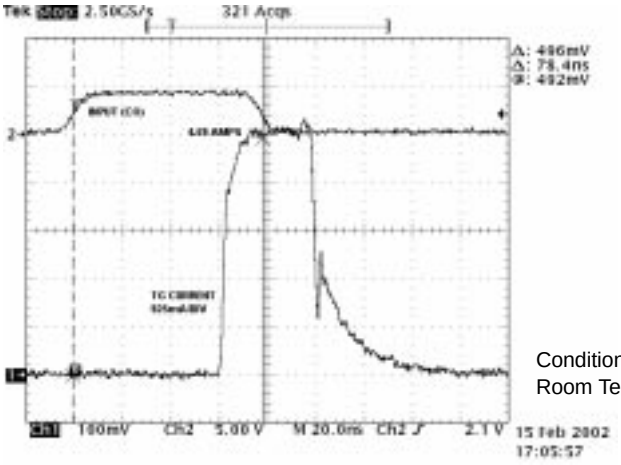
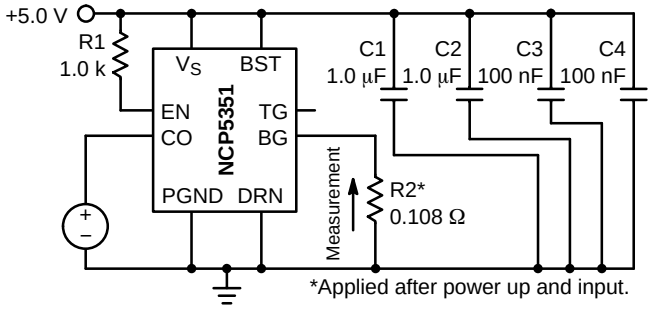


Figure 10. Bottom Gate Sourcing





Conditions: BST − DRN = 5.0 V;
Room Temperature; DRN = 0 V.

Figure 11. Top Gate Sourcing Current into 0.108 Ω

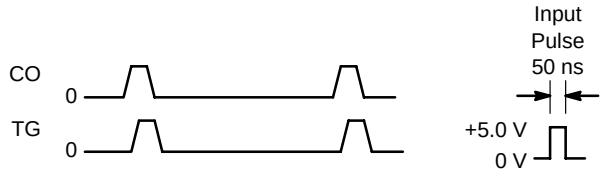


Figure 12. Top Gate Sourcing

TYPICAL PERFORMANCE CHARACTERISTICS

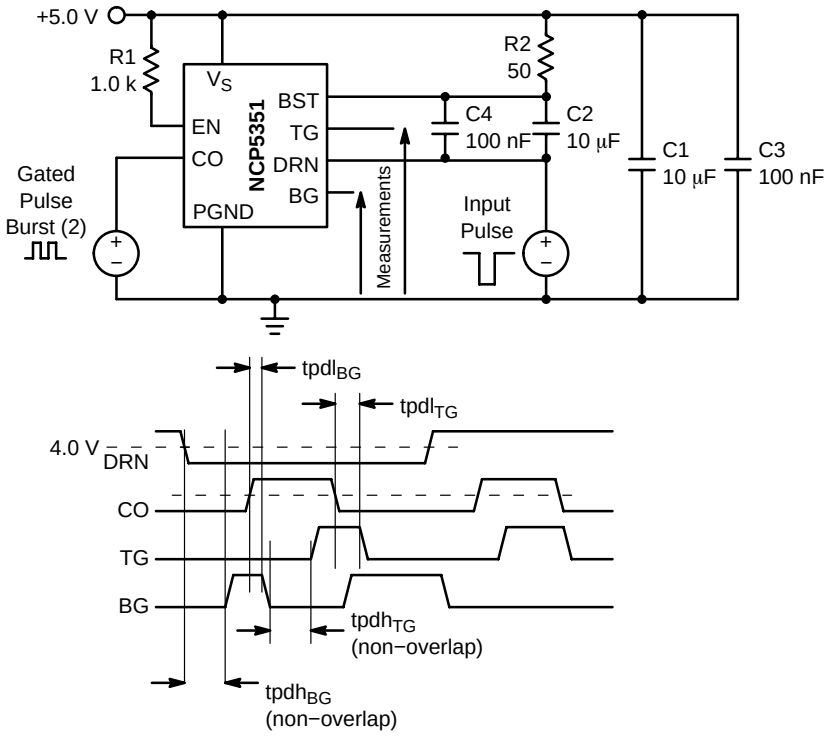
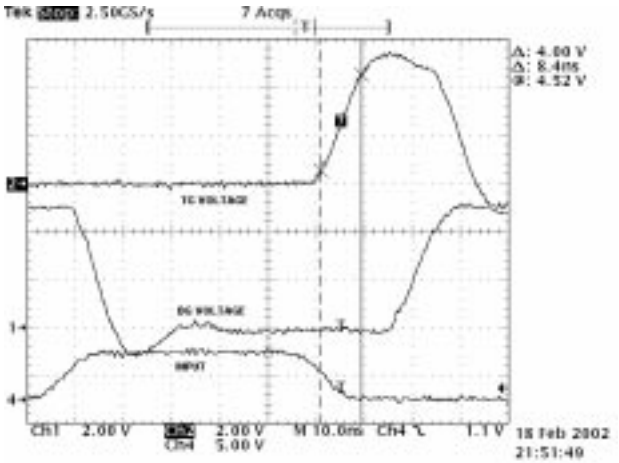
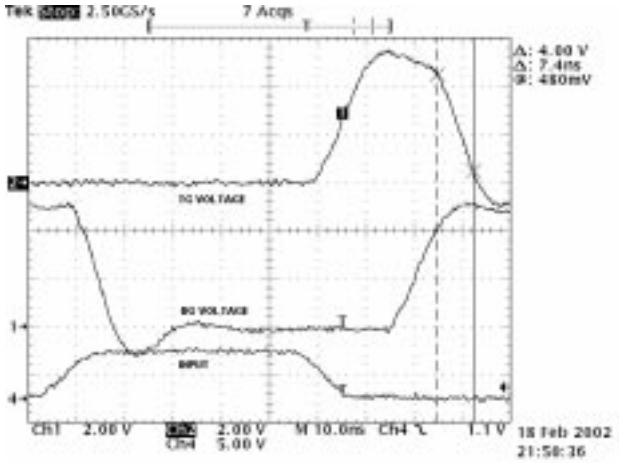


Figure 13. Nonoverlap Test Configuration



Conditions: V_S = 5.0 V; BST − DRN = 5.0 V; C_{LOAD} = 5.7 nF; Room Temperature.

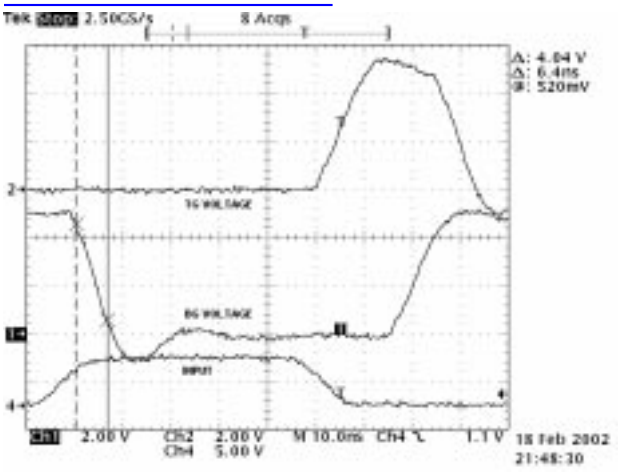
Figure 14. Top Gate Rise Time



Conditions: V_S = 5.0 V; BST − DRN = 5.0 V; C_{LOAD} = 5.7 nF; Room Temperature.

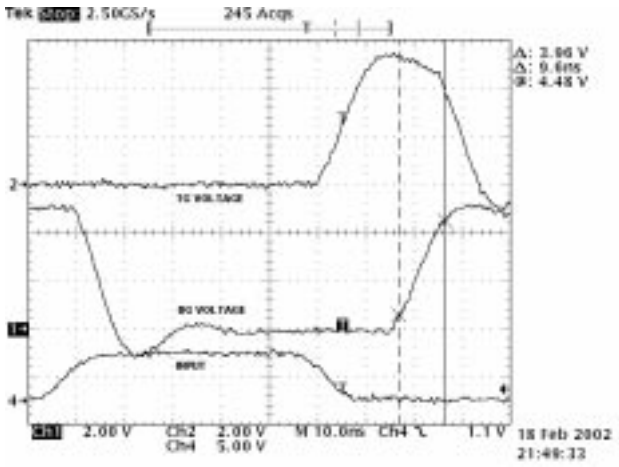
Figure 15. Top Gate Fall Time

TYPICAL PERFORMANCE CHARACTERISTICS



Conditions: V_S = 5.0 V; BST − DRN = 5.0 V; C_{LOAD} = 5.7 nF; Room Temperature.

Figure 16. Bottom Gate Fall Time



Conditions: V_S = 5.0 V; BST − DRN = 5.0 V; C_{LOAD} = 5.7 nF; Room Temperature.

Figure 17. Bottom Gate Rise Time

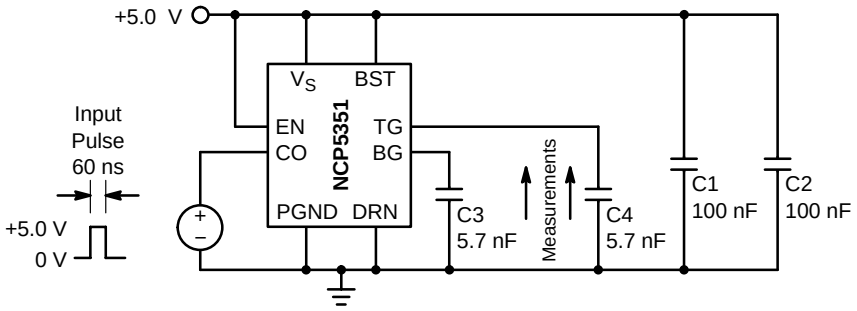
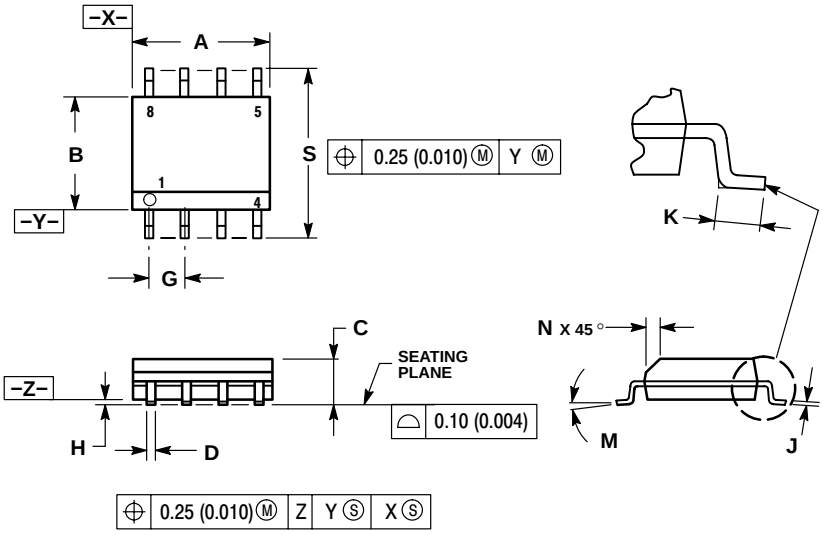


Figure 18. Bottom Gate and Top Gate Rise/Fall Time Test

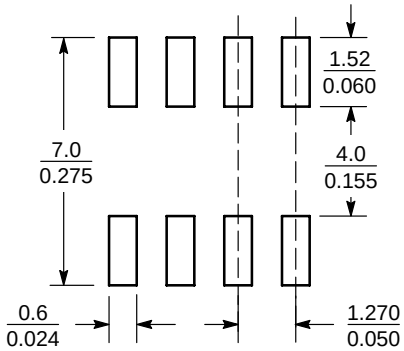
PACKAGE DIMENSIONS

SOIC−8 NB
CASE 751−07
ISSUE AB



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

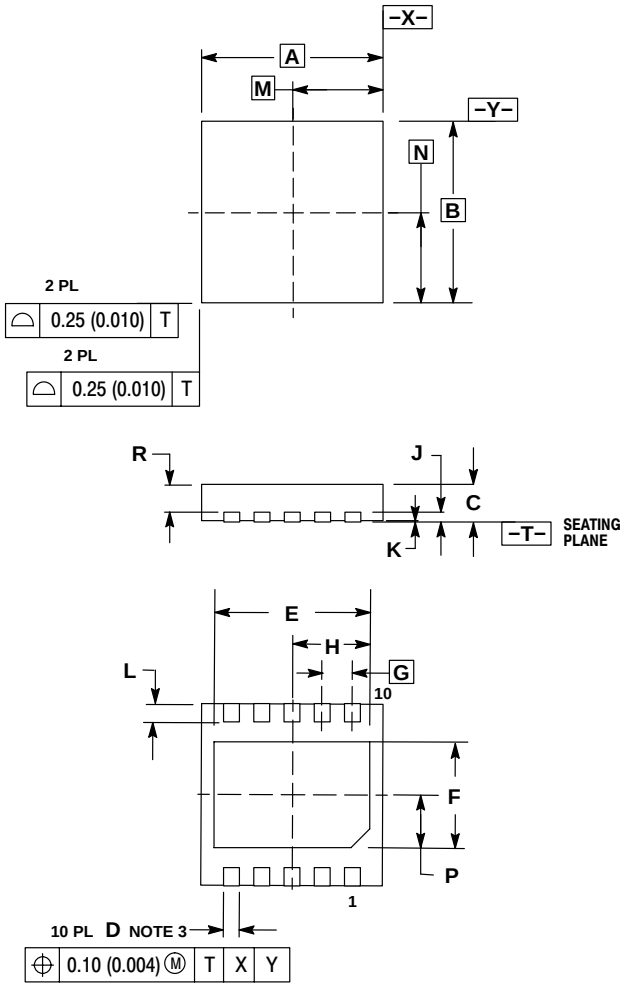
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244



SCALE 6:1 (mm / inches)

PACKAGE DIMENSIONS

QFN−10
CASE 485C−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	3.00 BSC		0.118 BSC	
B	3.00 BSC		0.118 BSC	
C	0.80	1.00	0.031	0.039
D	0.20	0.30	0.008	0.012
E	2.45	2.55	0.096	0.100
F	1.75	1.85	0.069	0.073
G	0.50 BSC		0.020 BSC	
H	1.23	1.28	0.048	0.050
J	0.20 REF		0.008 REF	
K	0.00	0.05	0.000	0.002
L	0.35	0.45	0.014	0.018
M	1.50 BSC		0.059 BSC	
N	1.50 BSC		0.059 BSC	
P	0.88	0.93	0.035	0.037
R	0.60	0.80	0.024	0.031

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