

DUAL JK FLIP-FLOP WITH SET AND RESET; POSITIVE-EDGE TRIGGER

FEATURES

- J, $\bar{K}$ inputs for easy D-type flip-flop
- Toggle flip-flop or "do nothing" mode
- Output capability: standard
- I²C category: flip-flops

GENERAL DESCRIPTION

The 74HC/HCT109 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT109 are dual positive-edge triggered, $\overline{J}\overline{K}$ flip-flops with individual J, $\overline{K}$ inputs, clock (CP) inputs, set ($\overline{S}_D$) and reset ($\overline{R}_D$) inputs; also complementary Q and $\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input.

The J and $\bar{K}$ inputs control the state changes of the flip-flops as described in the mode select function table.

The J and K inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

The JK design allows operation as a D-type flip-flop by tying the J and $\bar{K}$ inputs together.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PHL} / t _{PLH}	propagation delay nCP to nQ, nQ̄ nSD to nQ, nQ̄ nRD to nQ, nQ̄	C _L = 15 pF V _{CC} = 5 V	15 12 12	17 14 15	ns ns ns
f _{max}	maximum clock frequency		75	61	MHz
C _I	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per flip-flop	notes 1 and 2	20	22	pF

$GND = 0\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}; t_r = t_f = 6\text{ ns}$

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz	C_L = output load capacitance in pF
f_o = output frequency in MHz	V_{CC} = supply voltage in V
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs	

2. For HC the condition is $V_I = \text{GND to } V_{CC}$
For HCT the condition is $V_I = \text{GND to } V_{CC} - 1.5 \text{ V}$

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z).

16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\bar{R}_D, 2\bar{R}_D$	asynchronous reset-direct input (active LOW)
2, 14, 3, 13	$1J, 2J, 1\bar{K}, 2\bar{K}$	synchronous inputs; flip-flops 1 and 2
4, 12	$1CP, 2CP$	clock input (LOW-to-HIGH, edge-triggered)
5, 11	$1\bar{S}_D, 2\bar{S}_D$	asynchronous set-direct input (active LOW)
6, 10	$1Q, 2Q$	true flip-flop outputs
7, 9	$1\bar{Q}, 2\bar{Q}$	complement flip-flop outputs
8	GND	ground (0 V)
16	V_{CC}	positive supply voltage

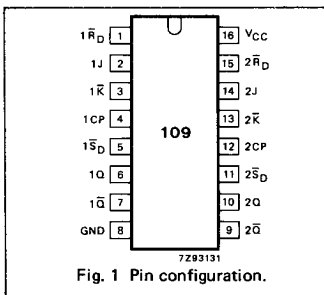


Fig. 1 Pin configuration.

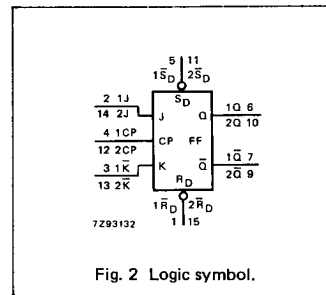


Fig. 2 Logic symbol.

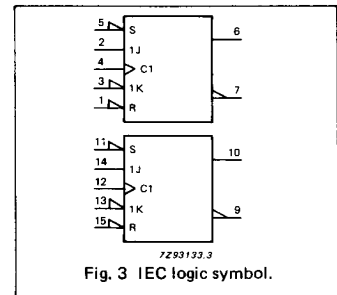


Fig. 3 IEC logic symbol.

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FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\bar{S}_D$	$\bar{R}_D$	CP	J	$\bar{K}$	Q	$\bar{Q}$
asynchronous set	L	H	X	X	X	H	L
asynchronous reset	H	L	X	X	X	L	H
undetermined	L	L	X	X	X	H	H
toggle	H	H	↑	h	l	$\bar{q}$	q
load "0" (reset)	H	H	↑	l	l	L	L
load "1" (set)	H	H	↑	h	h	H	H
hold "no change"	H	H	↑	l	h	q	$\bar{q}$

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
↑ = LOW-to-HIGH CP transition

Fig. 4 Functional diagram.

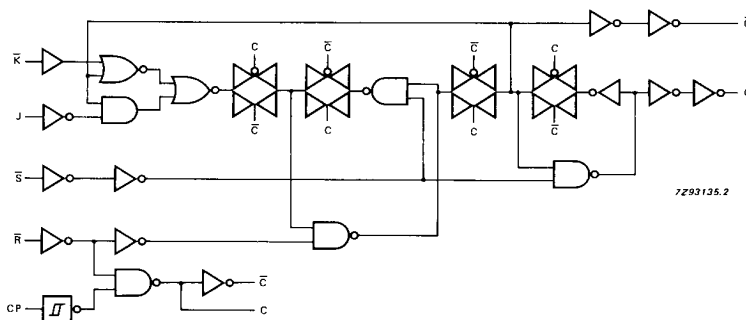


Fig. 5 Logic diagram (one flip-flop).

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For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I_{CC} category: flip-flops**AC CHARACTERISTICS FOR 74HC**GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V _{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay nCP to nQ, nQ̄		50 18 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t _{PLH}	propagation delay nS _D to nQ		30 11 9	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 7
t _{PHL}	propagation delay nS _D to nQ̄		41 15 12	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 7
t _{PHL}	propagation delay nR _D to nQ		41 15 12	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig. 7
t _{PLH}	propagation delay nR _D to nQ̄		39 14 11	170 34 29		215 43 37		255* 51 43	ns	2.0 4.5 6.0	Fig. 7
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t _W	clock pulse width HIGH or LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t _W	set or reset pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t _{rem}	removal time nS _D , nR _D to nCP	70 14 12	19 7 6		90 18 15		105 21 18		ns	2.0 4.5 6.0	Fig. 7
t _{su}	set-up time nJ, nK to nCP	70 14 12	17 6 5		90 18 15		105 21 18		ns	2.0 4.5 6.0	Fig. 6
t _h	hold time nJ, nK to nCP	5 5 5	0 0 0		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 6
f _{max}	maximum clock pulse frequency	6.0 30 35	22 68 81		5.0 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I_{CC} category: flip-flops

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nJ, nK	0.35
nR _D	0.35
nS _D	0.35
nCP	0.35

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS	
		74HCT									V _{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} / t _{PLH}	propagation delay nCP to nQ, nQ		20	35		44		53	ns	4.5	Fig. 6	
t _{PLH}	propagation delay nS _D to nQ		13	26		33		39	ns	4.5	Fig. 7	
t _{PHL}	propagation delay nS _D to nQ		19	35		44		53	ns	4.5	Fig. 7	
t _{PHL}	propagation delay nR _D to nQ		19	35		44		53	ns	4.5	Fig. 7	
t _{PLH}	propagation delay nR _D to nQ		16	32		40		48	ns	4.5	Fig. 7	
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6	
t _W	clock pulse width HIGH or LOW	18	9		23		27		ns	4.5	Fig. 6	
t _W	set or reset pulse width HIGH or LOW	16	8		20		24		ns	4.5	Fig. 7	
t _{rem}	removal time nS _D , nR _D to nCP	16	8		20		24		ns	4.5	Fig. 7	
t _{su}	set-up time nJ, nK to nCP	18	8		23		27		ns	4.5	Fig. 6	
t _h	hold time nJ, nK to nCP	3	−3		3		3		ns	4.5	Fig. 6	
f _{max}	maximum clock pulse frequency	27	55		22		18		MHz	4.5	Fig. 6	

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AC WAVEFORMS

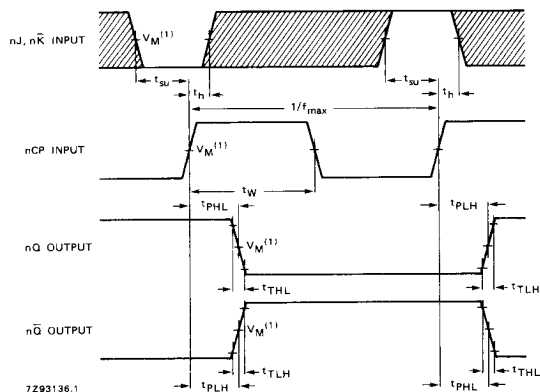


Fig. 6 Waveforms showing the clock (nCP) to output (nQ, nQ̄) propagation delays, the clock pulse width, the nJ, nK̄ to nCP set-up, the nCP to nJ, nK̄ hold times, the output transition times and the maximum clock pulse frequency.

Note to Fig. 6

The shaded areas indicate when the input is permitted to change for predictable output performance.

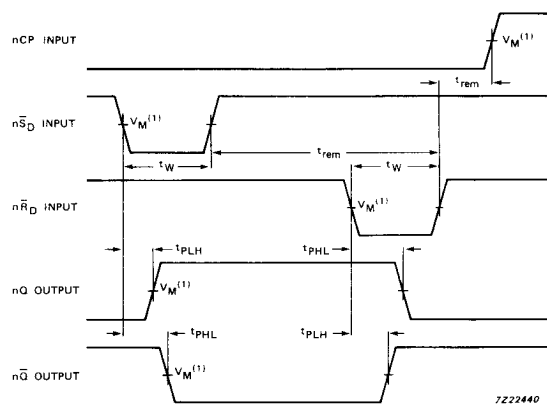


Fig. 7 Waveforms showing the set (nSD) and reset (nRD) input to output (nQ, nQ̄) propagation delays, the set and reset pulse widths and the nRD, nSD to nCP removal time.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.