

## 2-Mbit (256K x 8) Static RAM

### Features

- High speed: 45 ns
- Wide voltage range: 4.5 V – 5.5 V
- Pin compatible with CY62138V
- Ultra low standby power
  - Typical standby current: 1  $\mu$ A
  - Maximum standby current: 5  $\mu$ A
- Ultra low active power
  - Typical active current: 1.6 mA @ f = 1 MHz
- Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{OE}$  features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Available in Pb-free 32-pin SOIC and 32-pin TSOP II packages

### Functional Description <sup>[1]</sup>

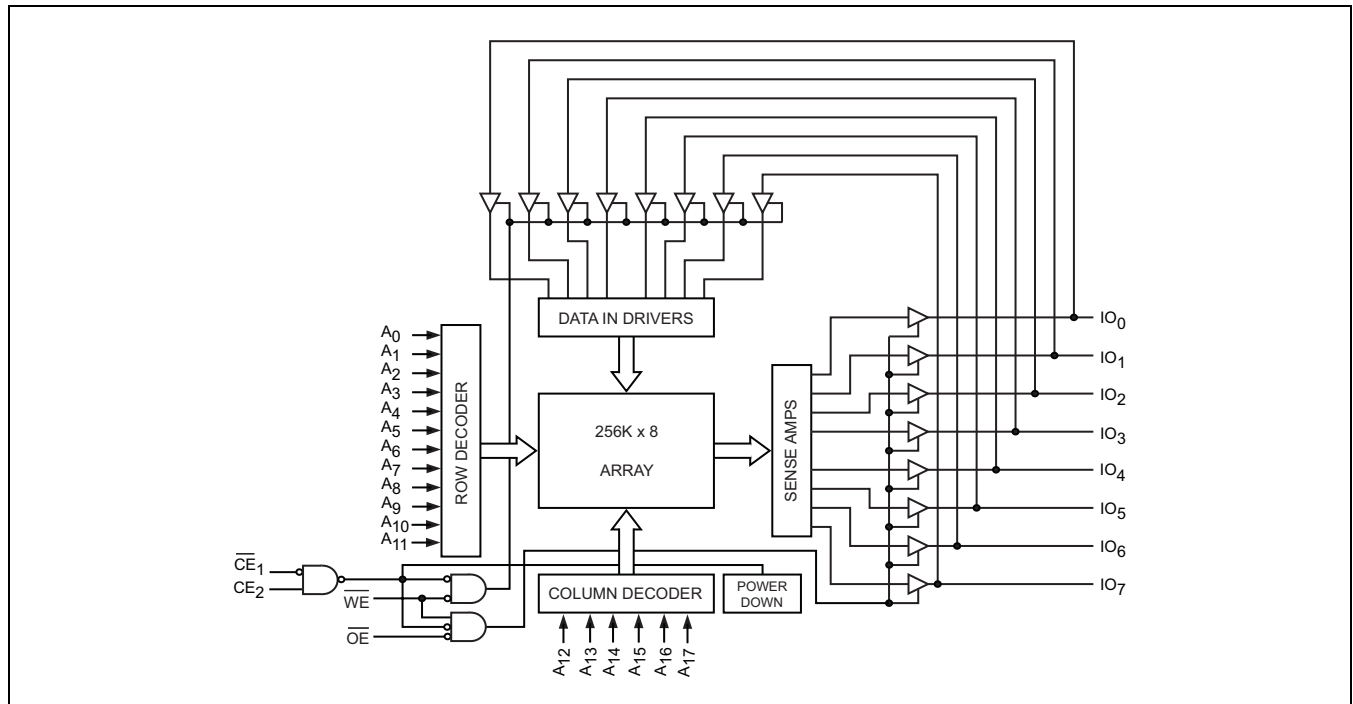
The CY62138F is a high performance CMOS static RAM organized as 256K words by 8 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW).

To write to the device, take Chip Enable ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Write Enable (WE) inputs LOW. Data on the eight IO pins ( $IO_0$  through  $IO_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{17}$ ).

To read from the device, take Chip Enable ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and output enable ( $\overline{OE}$ ) LOW while forcing Write Enable (WE) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the IO pins.

The eight input and output pins ( $IO_0$  through  $IO_7$ ) are placed in a high impedance state when the device is deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH and WE LOW).

### Logic Block Diagram

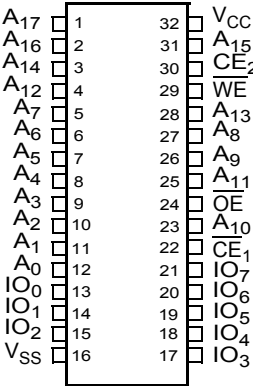


#### Note

1. For best practice recommendations, refer to the Cypress application note "System Design Guidelines" at <http://www.cypress.com>.

Pin Configuration <sup>[2]</sup>

32-Pin SOIC/TSOP II Pinout  
Top View



Product Portfolio

Product	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
					Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (μA)	
					f = 1MHz		f = f <sub>max</sub>			
	Min	Typ <sup>[3]</sup>	Max		Typ <sup>[3]</sup>	Max	Typ <sup>[3]</sup>	Max	Typ <sup>[3]</sup>	Max
CY62138FLL	4.5V	5.0V	5.5V	45	1.6	2.5	13	18	1	5

**Notes**  
 2. NC pins are not connected on the die.  
 3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25°C.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... -65°C to + 150°C

Ambient Temperature with  
Power Applied ..... -55°C to + 125°C

Supply Voltage to Ground  
Potential ..... -0.5V to 6.0V ( $V_{CCmax} + 0.5V$ )

DC Voltage Applied to Outputs  
in High-Z state <sup>[4, 5]</sup> ..... -0.5V to 6.0V ( $V_{CCmax} + 0.5V$ )

DC Input Voltage <sup>[4, 5]</sup> ..... -0.5V to 6.0V ( $V_{CCmax} + 0.5V$ )

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V  
(MIL-STD-883, Method 3015)

Latch-up Current ..... > 200 mA

## Operating Range

Device	Range	Ambient Temperature	$V_{CC}$ <sup>[6]</sup>
CY62138FLL	Industrial	-40°C to +85°C	4.5V to 5.5V

## Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions	45 ns			Unit
			Min	Typ <sup>[3]</sup>	Max	
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -1.0$ mA	2.4			V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 2.1$ mA			0.4	V
$V_{IH}$	Input HIGH Voltage	$V_{CC} = 4.5V$ to $5.5V$	2.2		$V_{CC} + 0.5$	V
$V_{IL}$	Input LOW Voltage	$V_{CC} = 4.5V$ to $5.5V$	-0.5		0.8	V
$I_{IX}$	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1		+1	μA
$I_{OZ}$	Output Leakage Current	$GND \leq V_O \leq V_{CC}$ , Output Disabled	-1		+1	μA
$I_{CC}$	$V_{CC}$ Operating Supply Current	$f = f_{max} = 1/t_{RC}$		13	18	mA
		$f = 1$ MHz		1.6	2.5	
$I_{SB2}$ <sup>[7]</sup>	Automatic CE Power Down Current CMOS inputs	$\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = 0$ , $V_{CC} = V_{CC(max)}$		1	5	μA

## Capacitance (For all packages) <sup>[8]</sup>

Parameter	Description	Test Conditions	Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25^\circ C$ , $f = 1$ MHz,	10	pF
$C_{OUT}$	Output capacitance	$V_{CC} = V_{CC(typ)}$	10	pF

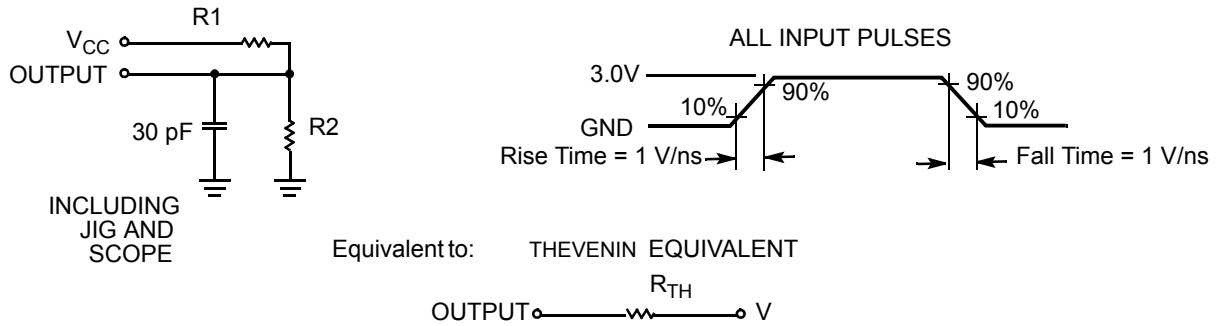
## Thermal Resistance <sup>[8]</sup>

Parameter	Description	Test Conditions	SOIC	TSOP II	Unit
$\Theta_{JA}$	Thermal Resistance (Junction to Ambient)	Still air, soldered on a 3 × 4.5 inch two-layer printed circuit board	44.53	44.16	°C/W
$\Theta_{JC}$	Thermal Resistance (Junction to Case)		24.05	11.97	°C/W

### Notes

- $V_{IL(min)}$  = -2.0V for pulse durations less than 20 ns.
- $V_{IH(max)}$  =  $V_{CC} + 0.75V$  for pulse durations less than 20ns.
- Full device AC operation assumes a 100 μs ramp time from 0 to  $V_{CC(min)}$  and 200 μs wait time after  $V_{CC}$  stabilization.
- Only chip enables ( $\overline{CE}_1$  and  $CE_2$ ) must be at CMOS level to meet the  $I_{SB2}$  /  $I_{CCDR}$  spec. Other inputs can be left floating.
- Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms

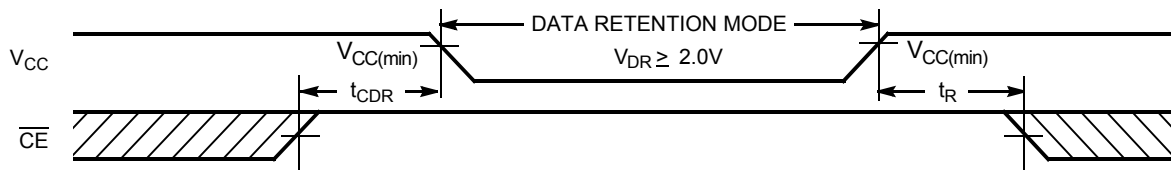


Parameters	5.0V	Unit
R1	1800	Ω
R2	990	Ω
R <sub>TH</sub>	639	Ω
V <sub>TH</sub>	1.77	V

## Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min	Typ <sup>[3]</sup>	Max	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention		2.0			V
I <sub>CCDR</sub> <sup>[7]</sup>	Data Retention Current	V <sub>CC</sub> = V <sub>DR</sub> , $\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V		1	5	μA
t <sub>CDR</sub> <sup>[8]</sup>	Chip Deselect to Data Retention Time		0			ns
t <sub>R</sub> <sup>[9]</sup>	Operation Recovery Time		t <sub>RC</sub>			ns

## Data Retention Waveform<sup>[10]</sup>



### Notes:

- Full device AC operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min)</sub> ≥ 100 μs or stable at V<sub>CC(min)</sub> ≥ 100 μs.
- $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and CE<sub>2</sub>. When  $\overline{CE}_1$  is LOW and CE<sub>2</sub> is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or CE<sub>2</sub> is LOW,  $\overline{CE}$  is HIGH.

## Switching Characteristics (Over the Operating Range) <sup>[11]</sup>

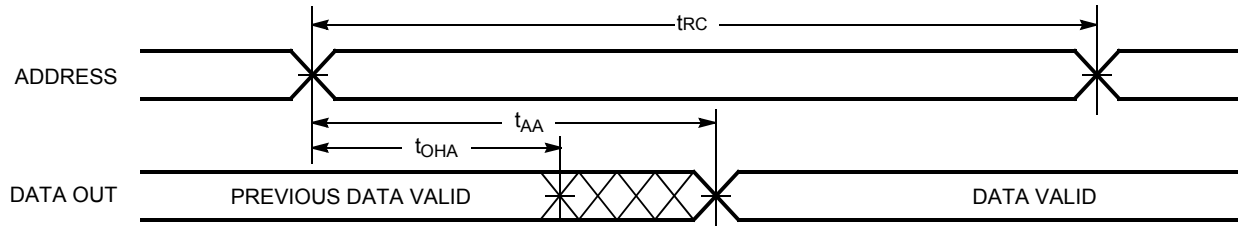
Parameter	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t <sub>RC</sub>	Read Cycle Time	45		ns
t <sub>AA</sub>	Address to Data Valid		45	ns
t <sub>OHA</sub>	Data Hold from Address Change	10		ns
t <sub>ACE</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to Data Valid		45	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		22	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low-Z <sup>[12]</sup>	5		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High-Z <sup>[12, 13]</sup>		18	ns
t <sub>LZCE</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to Low Z <sup>[12]</sup>	10		ns
t <sub>HZCE</sub>	$\overline{CE}_1$ HIGH or CE <sub>2</sub> LOW to High-Z <sup>[12, 13]</sup>		18	ns
t <sub>PU</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to power up	0		ns
t <sub>PD</sub>	$\overline{CE}_1$ HIGH or CE <sub>2</sub> LOW to power down		45	ns
Write Cycle <sup>[14]</sup>				
t <sub>WC</sub>	Write Cycle Time	45		ns
t <sub>SCE</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to Write End	35		ns
t <sub>AW</sub>	Address Setup to Write End	35		ns
t <sub>HA</sub>	Address Hold from Write End	0		ns
t <sub>SA</sub>	Address Setup to Write Start	0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	35		ns
t <sub>SD</sub>	Data Setup to Write end	25		ns
t <sub>HD</sub>	Data Hold from Write End	0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High-Z <sup>[12, 13]</sup>		18	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low-Z <sup>[12]</sup>	10		ns

### Notes

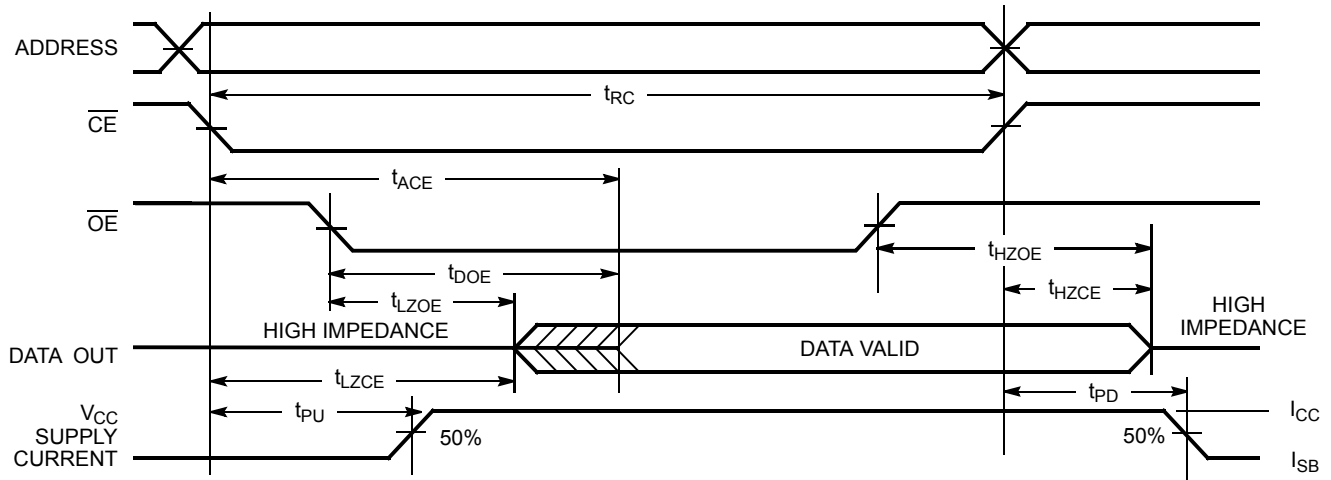
- Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1V/ns) or less, timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the [AC Test Loads and Waveforms on page 4](#).
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high impedance state.
- The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE}_1 = V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

## Switching Waveforms

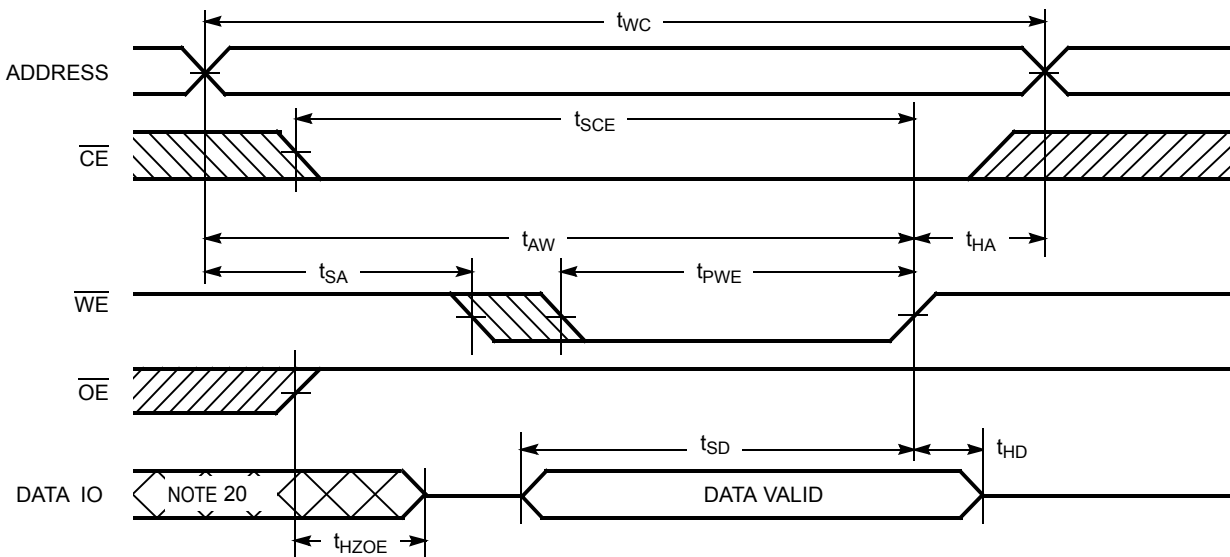
### Read Cycle 1 (Address transition controlled) [15, 16]



### Read Cycle No. 2 ( $\overline{OE}$ controlled) [10, 16, 17]



### Write Cycle No. 1 ( $\overline{WE}$ controlled) [10, 14, 18, 19]

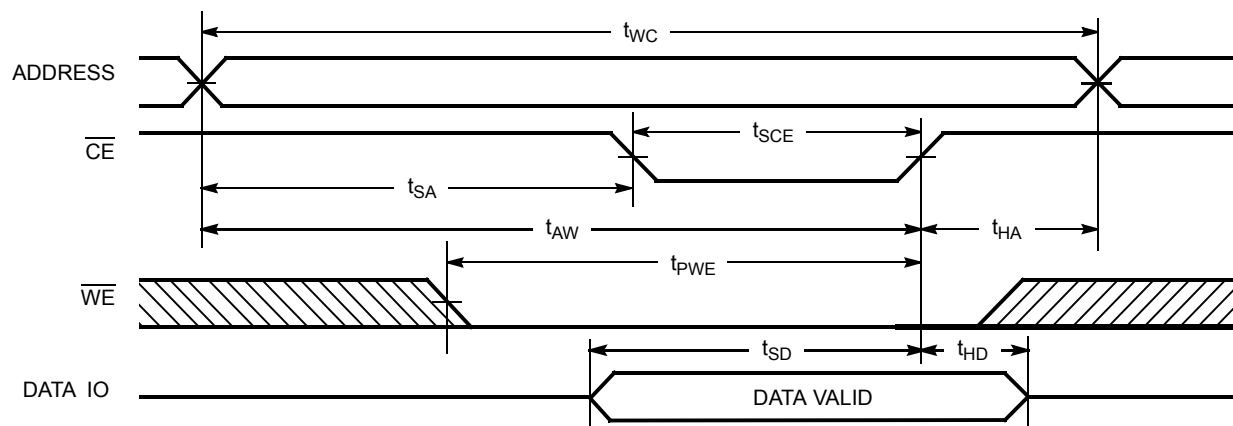


#### Notes:

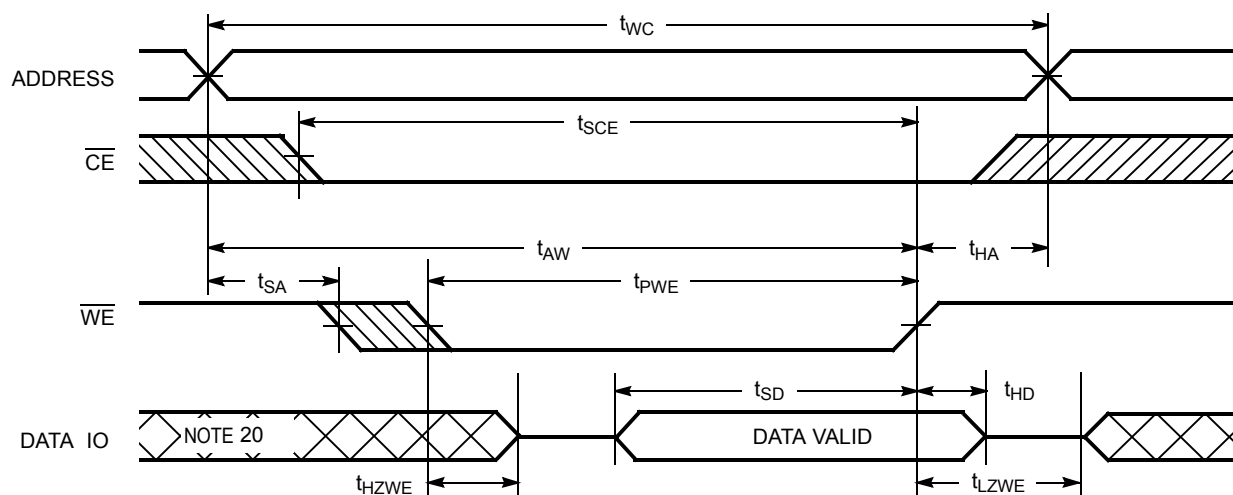
15. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $CE_2 = V_{IH}$ .
16.  $\overline{WE}$  is HIGH for read cycle.
17. Address valid before or similar to  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.
18. Data IO is high impedance if  $\overline{OE} = V_{IH}$ .
19. If  $\overline{CE}_1$  goes HIGH or  $CE_2$  goes LOW simultaneously with  $\overline{WE}$  HIGH, the output remains in high impedance state.
20. During this period, the IOs are in output state. Do not apply input signals.

## Switching Waveforms (continued)

### Write Cycle No. 2 ( $\overline{\text{CE1}}$ or $\text{CE2}$ controlled) [10, 14, 18, 19]



### Write Cycle No. 3 ( $\overline{\text{WE}}$ controlled, $\overline{\text{OE}}$ LOW) [10, 19]



## Truth Table

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power Down	Standby ( $I_{\text{SB}}$ )
L	H	L	Data Out	Read	Active ( $I_{\text{CC}}$ )
L	L	X	Data In	Write	Active ( $I_{\text{CC}}$ )
L	H	H	High Z	Selected, Outputs Disabled	Active ( $I_{\text{CC}}$ )

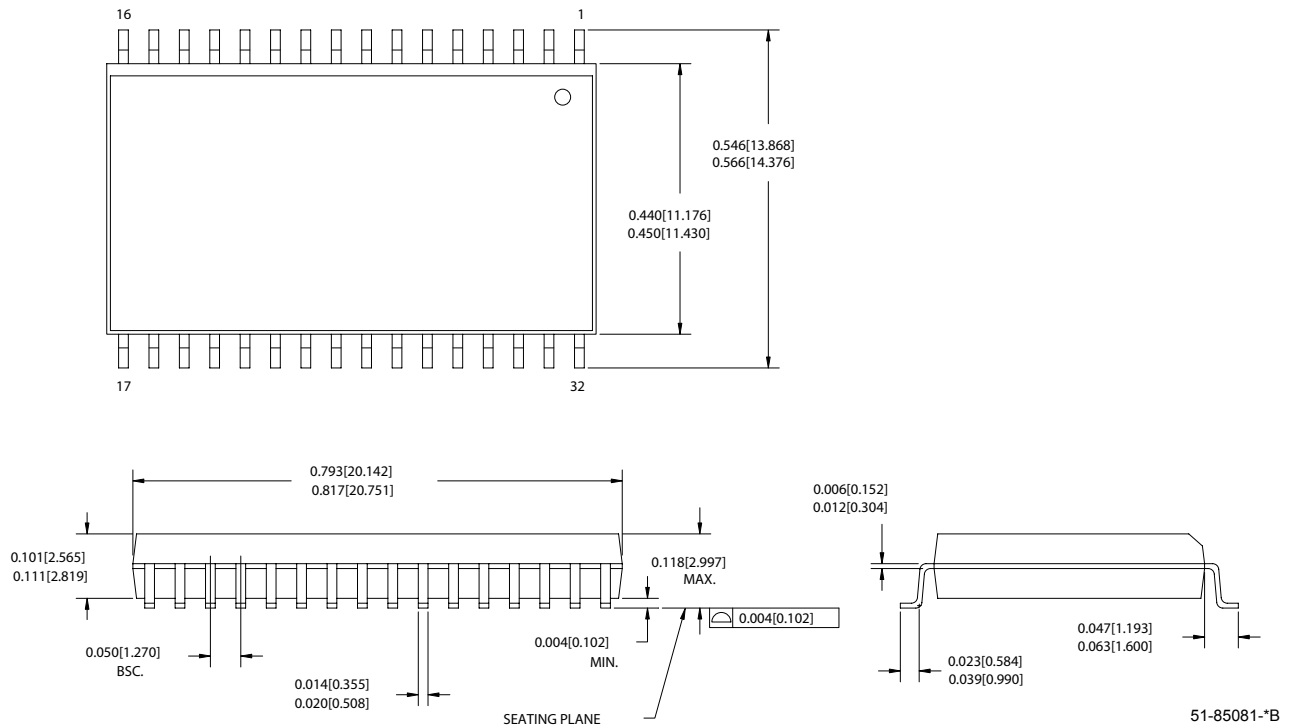
## Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62138FLL-45SXI	51-85081	32-pin Small Outline Integrated Circuit (Pb-free)	Industrial
	CY62138FLL-45ZSXI	51-85095	32-pin Thin Small Outline Package II (Pb-free)	

Contact your local Cypress sales representative for availability of these parts.

## Package Diagrams

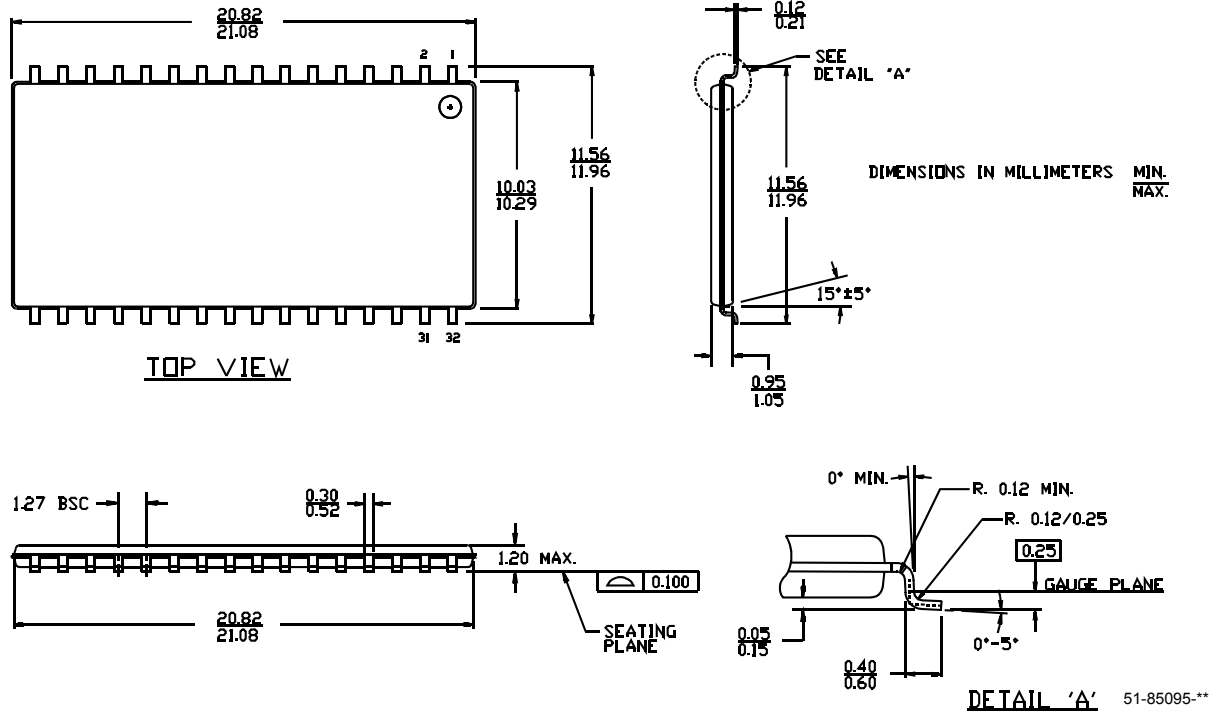
**Figure 1. 32-pin (450 Mil) Molded SOIC, 51-85081**





**Package Diagrams** (continued)

**Figure 2. 32-Pin TSOP II, 51-85095**



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## Document History Page

Document Title: CY62138F MoBL <sup>®</sup> 2-Mbit (256K x 8) Static RAM Document Number: 001-13194				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	797956	See ECN	VKN	New Data Sheet
*A	940341	See ECN	VKN	Added footnote #7 related to I <sub>SB2</sub> and I <sub>CCDR</sub>