REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	NOR 5962-R146-92	92-03-09	Monica L. Poelking
B	Add device types 05 and 06. Add case outlines X and Y. Editorial changes throughout.	96-06-26	Monica L. Poelking

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																			
SHEET																			
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B					
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28					

REV STATUS OF SHEETS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Tim H. Noh

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APPROVED BY
Don Cool

DRAWING APPROVAL DATE
91-09-11

REVISION LEVEL
B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, 8-BIT, CHMOS MICROCONTROLLER WITH 8 K BYTES EPROM MEMORY, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-91576
A	67268	

SHEET 1 OF 28

DESC FORM 193
JUL 94

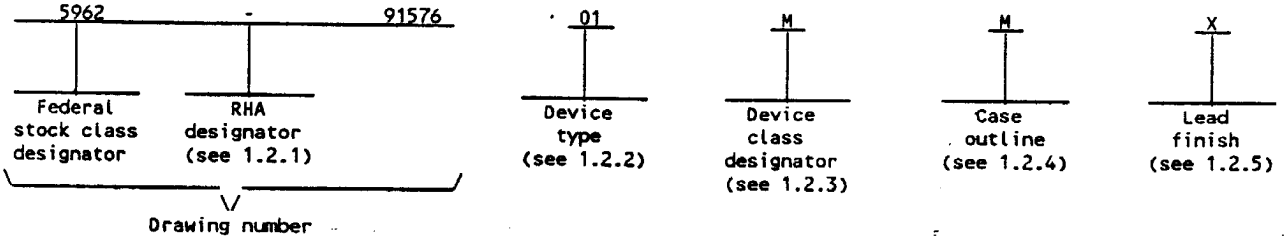
5962-E360-96

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Three product assurance classes consisting of space application (device class V), military high reliability (device classes M and Q), and non-traditional military (device class N) with a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". For device class N, the user is cautioned to assure that the device is appropriate for the application environment. When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes N, Q, and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	87C52	8-bit microcontroller with 8k-bytes EPROM memory (3.5 to 12 MHz)
02	87C52-16	8-bit microcontroller with 8k-bytes EPROM memory (3.5 to 16 MHz)
03	87C52	8-bit microcontroller with 8k-bytes of one time programmable EPROM memory (3.5 - 12 MHz)
04	87C52-16	8-bit microcontroller with 8k-bytes of one time programmable EPROM memory (3.5 - 16 MHz)
05	87C52	8-bit microcontroller with 8k-bytes of one time programmable EPROM memory (3.5 - 12 MHz)
06	87C52-16	8-bit microcontroller with 8k-bytes of one time programmable EPROM memory (3.5 - 16 MHz)

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
N	Certification and qualification to MIL-I-38535 with a non-traditional performance environment 1/
Q or V	Certification and qualification to MIL-I-38535

1/ Any device outside the traditional performance environment; i.e., an operating temperature range of -55°C to +125°C and which requires hermetic packaging.

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
M	CQCC1-J44	44	J lead chip carrier 2/
Q	GDIP1-T40 or CDIP2-T40	40	Dual-in-line package 2/
U	CQCC1-N44	44	Square leadless chip carrier 2/
X	MS-011-AC 3/	40	Plastic dual-line-line package
Y	MS-018-AC 3/	44	Plastic J-leaded chip carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes N, Q, and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 4/

Storage temperature range	-65°C to +150°C
Voltage on EA/V_{PP} pin to V_{SS} range	0 V dc to +13.0 V dc
Voltage on any pin to V_{SS} range	-0.5 V dc to +6.5 V dc
Input, output current on any two pins	±10 mA
Power dissipation (P_D)	1.5 W
Maximum junction temperature (T_J)	+200°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case outline X	15°C/W
Case outline Y	14°C/W
Case outline M, Q, and U	See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	5.0 V dc ±10%
Case operating temperature range (T_C):	
Devices 01 - 04	-55°C to +125°C
Devices 05 and 06	-40°C to +85°C
Maximum input low voltage(except EA)	0.2 V_{CC} - 0.25 V
Maximum input low voltage ($\overline{EA}$)	0.2 V_{CC} - 0.45 V
Minimum input high voltage (except XTAL1, RESET)	0.2 V_{CC} + 1.1 V
Minimum input high voltage (XTAL1, RESET)	0.7 V_{CC} + 0.2 V

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 5/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

2/ For device types 01 and 02, lid shall be transparent to permit ultraviolet light erasure.
3/ see JEDEC Publication 95.
4/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
5/ Values will be added when they become available.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

2.2 Non-Government publication. The following document forms a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the sloicitaion. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Publication 95 - Registered and Standard Outlines for Semiconductor Devices.

(Applications for copies should be addressed to the Electronic Industry Association, 2500 Wilson Boulevard, Arlington, VA 2201-3834).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes N, Q, and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes N, Q, and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Switching waveforms. The switching waveforms shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes N, Q, and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes N, Q, and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes N, Q, and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes N, Q, and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes N, Q, and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-I-38535, appendix A).

3.11 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.11.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.5.

3.11.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.6 and table III.

3.11.3 Verification of erasure of programmability of EPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A sub-groups	Device type	Limits Min	Limits Max	Unit
Input low voltage (except EA)	V_{IL}			1,2,3	All	-0.5 2/	$0.2\ V_{CC}$ -0.25	V
Input low voltage to EA	V_{IL1}			1,2,3	All	0 2/	$0.2\ V_{CC}$ -0.45	V
Input high voltage (except XTAL1, RESET)	V_{IH}			1,2,3	All	$0.2\ V_{CC}$ +1.1	V_{CC} +0.5 2/	V
Input high voltage (XTAL1, RESET)	V_{IH1}			1,2,3	All	$0.7\ V_{CC}$ +0.2	V_{CC} +0.5 2/	V
Output low voltage (Ports 1,2,3)	V_{OL}	I_{OL} = 1.6 mA 3/	$V_{IN} = V_{IH}$ min, V_{IL} max, V_{CC} = 4.5 V	1,2,3	All		0.45	V
Output low voltage port 0, ALE, PSEN	V_{OL1}	I_{OL} = 3.2 mA 3/		1,2,3	All		0.45	V
Output high voltage (Ports 1,2,3)	V_{OH}	I_{OH} = -60 µA 4/		1,2,3	All	2.4		V
		I_{OH} = -25 µA 4/				$0.75\ V_{CC}$		
		I_{OH} = -10 µA				$0.90\ V_{CC}$		
Output high voltage port 0 in external bus mode, ALE, PSEN	V_{OH1}	I_{OH} = -800 µA		1,2,3	All	2.4		
		I_{OH} = -300 µA				$0.75\ V_{CC}$		
		I_{OH} = -80 µA				$0.90\ V_{CC}$		
Logic 0 input current, ports 1,2,3	I_{IL}	V_{IN} = 0.45 V		1,2,3	All		-75	µA
Logic 1 to 0 transition current ports 1,2,3	I_{TL}	V_{CC} = 5.5 V 5/					-750	
Input leakage current port 0	I_{LI}	$V_{IN} = V_{IH}$ min				0	10	
		$V_{IN} = V_{IL}$ max				0	-10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A sub-groups	Device type	Limits Min	Limits Max	Unit
Reset pull down resistor	R_{RST}		1,2,3	All	50	300	kΩ
Pin capacitance	C_{IO}	See 4.4.1c	4	All		10	pF
Supply current running at 12 MHz, idle at 12 MHz, power down	I_{CC1}	2/ 6/	1,2,3	01, 03 05		35 6 75	mA mA µA
Supply current running at 16 MHz, idle at 16 MHz, power down	I_{CC2}	6/	1,2,3	02, 04 06		39 7 75	mA mA µA
Functional test		See 4.4.1b, V_{CC} = 4.5 V, 5.5 V	7,8	All			
EXTERNAL PROGRAM AND DATA MEMORY CHARACTERISTICS							
Oscillator frequency	$1/t_{clcl}$	See figure 4 7/ 8/ 9/	9,10,11	01,03,05	3.5	12	MHz
			9,10,11	02,04,06	3.5	16	
ALE pulse width	t_{LHLL}		9,10,11	01,03,05	112		ns
			9,10,11	02,04,06	68		
			9,10,11	All	$2t_{CLCL}$ -55		
Address valid to ALE low	t_{AVLL}		9,10,11	01,03,05	13		ns
			9,10,11	02,04,06	5		
			9,10,11	All	8/ t_{CLCL} -70		
Address hold after ALE low	t_{LLAX}		9,10,11	01,03,05	33		
			9,10,11	02,04,06	12		
			9,10,11	All	t_{CLCL} -50		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A sub-groups	Device type	Limits Min	Limits Max	Unit
ALE low to valid instr. in	t_{LLIV}	See figure 4 7/ 8/ 9/	9,10,11	01,03,05		218	ns
			9,10,11	02,04,06		132	
			9,10,11	All		$4t_{CLCL}$ -115	
ALE low to $\overline{PSEN}$ low	t_{LLPL}		9,10,11	01,03,05	28		ns
			9,10,11	02,04,06	7		
			9,10,11	All	t_{CLCL} -55		
$\overline{PSEN}$ pulse width	t_{PLPH}		9,10,11	01,03,05	190		ns
			9,10,11	02,04,06	125		
			9,10,11	All	$3t_{CLCL}$ -60		
$\overline{PSEN}$ low to valid instr. in	t_{PLIV}		9,10,11	01,03,05		130	ns
			9,10,11	02,04,06		65	
			9,10,11	All		$3t_{CLCL}$ -120	
Input instr. hold after PSEN	t_{PXIX}		9,10,11	All	0		
Input instr. float after PSEN	t_{PXIZ}		9,10,11	01,03,05		58	ns
			9,10,11	02,04,06		37	
			9,10,11	All		t_{CLCL} -25	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Address to valid instr. in	t_{AVIV}	See figure 4 7/ 8/ 9/	9,10,11	01,03,05		312	ns
			9,10,11	02,04,06		188	
			9,10,11	All		$5t_{CLCL}$ -120	
$\overline{PSEN}$ low to address float	t_{PLAZ}		9,10,11	All		25	ns
$\overline{RD}$ pulse width	t_{RLRH}		9,10,11	01,03,05	400		ns
			9,10,11	02,04,06	270		
			9,10,11	All	$6t_{CLCL}$ -100		
$\overline{WR}$ pulse width	t_{WLWH}		9,10,11	01,03,05	400		ns
			9,10,11	02,04,06	270		
			9,10,11	All	$6t_{CLCL}$ -100		
$\overline{RD}$ low to valid data in	t_{RLDV}		9,10,11	01,03,05		232	ns
			9,10,11	02,04,06		123	
			9,10,11	All		$5t_{CLCL}$ -185	
Data hold after $\overline{RD}$	t_{RHDX}		9,10,11	All	0		ns
Data float after $\overline{RD}$	t_{RHDZ}		9,10,11	01,03,05		82	ns
			9,10,11	02,04,06		30	
			9,10,11	All		$2t_{CLCL}$ -85	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
ALE low to valid data in	t_{LLDV}	See figure 4 7/ 8/ 9/	9,10,11	01,03,05		496	ns
			9,10,11	02,04,06		320	
			9,10,11	All		$8t_{CLCL}$ -170	
Address to valid data in	t_{AVDV}		9,10,11	01,03,05		565	ns
			9,10,11	02,04,06		370	
			9,10,11	All		$9t_{CLCL}$ -185	
ALE low to $\overline{RD}$ or or $\overline{WR}$ low	t_{LLWL}		9,10,11	01,03,05	185	315	ns
			9,10,11	02,04,06	120	250	
			9,10,11	All	$3t_{CLCL}$ -65	$3t_{CLCL}$ +65	
Address to $\overline{RD}$ to $\overline{WR}$ low	t_{AVWL}		9,10,11	01,03,05	188		ns
			9,10,11	02,04,06	102		
			9,10,11	All	$4t_{CLCL}$ -145		
Data valid to $\overline{WR}$ transition	t_{QVWX}		9,10,11	01,03,05	8		ns
			9,10,11	02,04,06	5		
			9,10,11	All	t_{CLCL} - 75		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A sub-groups	Device type	Limits Min	Limits Max	Unit
Data hold after $\overline{WR}$	t_{WHQX}	See figure 4 7/ 8/ 9/	9,10,11	01,03,05	18		ns
			9,10,11	02,04,06	5		
			9,10,11	All	t_{CLCL} -65		
$\overline{RD}$ low to address float	t_{RLAZ}		9,10,11	All		0	ns
$\overline{RD}$ or $\overline{WR}$ high to ALE high	t_{WHLH}		9,10,11	01,03,05	18	148	ns
			9,10,11	02,04,06	5	127	
			9,10,11	All	t_{CLCL} 9/ -65	t_{CLCL} +65	
Serial port clock cycle time	t_{XLXL}	See figure 4 7/ 8/ 9/	9,10,11	01,03,05	1000		ns
			9,10,11	02,04,06	740		
			9,10,11	All	$12t_{CLCL}$		
Output data setup to clock rising edge	t_{QVXH}		9,10,11	01,03,05	700		ns
			9,10,11	02,04,06	484		
			9,10,11	All	$10t_{CLCL}$ -133		
Output data hold after clock rising edge	t_{XHQX}		9,10,11	01,03,05	50		ns
			9,10,11	02,04,06	6		
			9,10,11	All	$2t_{CLCL}$ -117		
Input data hold after clock rising edge	t_{XHDX}		9,10,11	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A sub-groups	Device type	Limits Min	Limits Max	Unit
Clock rising edge to input data valid	t_{XHDV}	See figure 4 7/ 8/ 9/	9,10,11	01,03,05	700		ns
			9,10,11	02,04,06	484		
			9,10,11	All	$10t_{CLCL}$ -133		
High time	t_{CHCX}		9,10,11	All	20		ns
Low time	t_{CLCX}		9,10,11	All	20		ns
Rise time	t_{CLCH}		9,10,11	All		20	ns
Fall time	t_{CHCL}		9,10,11	All		20	ns

1/ Unless otherwise specified, all testing to be performed using worst case test conditions. The operating temperature shall be as specified in 1.4.

2/ Guaranteed, if not tested, to the limits specified.

3/ Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE pin may exceed 0.8 V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5 mA and no more than two outputs exceed the test conditions.

4/ Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{CC} specification when the address bits are stabilizing.

5/ Pins of ports 1, 2, and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2 V.

6/ I_{CC} Max at other frequencies is given by: Active mode: I_{CC} Max = 0.94 x FREQ + 23.72: Idle mode: I_{CC} Max = 0.14 x FREQ + 4.32, where FREQ is the external oscillator frequency in MHz. I_{CC} Max is given in mA. See figure 4.

7/ All devices to be tested at 16 MHz only, but guaranteed across the specified operating frequency range. Devices not meeting the limits of the 16 MHz devices may be retested to be supplied at the slower 12 MHz speed grade.

8/ Parametric values are based on a 12 MHz oscillator for device types 01, 03, and 05, a 16 MHz oscillator for device types 02, 04, 06, and a variable oscillator for all devices.

9/ Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100 pF, load capacitance for all other outputs = 80 pF.

Device types	All	
Case outlines	Q,X	M,U, and Y
Terminal number	Terminal symbol	Terminal symbol
1	P1.0/T2	NC
2	P1.1/T2EX	T2/P1.0
3	P1.2	T2EX/P1.1
4	P1.3	P1.2
5	P1.4	P1.3
6	P1.5	P1.4
7	P1.6	P1.5
8	P1.7	P1.6
9	RST	P1.7
10	RxD/P3.0	RST
11	TxD/P3.1	RxD/P3.0
12	INT0/P3.2	NC
13	INT1/P3.3	TxD/P3.1
14	T0/P3.4	INT0/P3.2
15	T1/P3.5	INT1/P3.3
16	WR/P3.6	T0/P3.4
17	RD/P3.7	T1/P3.5
18	XTAL2	WR/P3.6
19	XTAL1	RD/P3.7
20	V_{SS}	XTAL2
21	P2.0/A8	XTAL1
22	P2.1/A9	V_{SS}
23	P2.2/A10	NC
24	P2.3/A11	P2.0/A8
25	P2.4/A12	P2.1/A9
26	P2.5/A13	P2.2/A10
27	P2.6/A14	P2.3/A11
28	P2.7/A15	P2.4/A12
29	PSEN	P2.5/A13
30	ALE/PROG	P2.6/A14
31	EA/V_{PP}	P2.7/A15
32	P0.7/AD7	PSEN
33	P0.6/AD6	ALE/PROG
34	P0.5/AD5	NC
35	P0.4/AD4	EA/V_{PP}
36	P0.3/AD3	P0.7/AD7
37	P0.2/AD2	P0.6/AD6
38	P0.1/AD1	P0.5/AD5
39	P0.0/AD0	P0.4/AD4
40	V_{DD}	P0.3/AD3
41	----	P0.2/AD2
42	----	P0.1/AD1
43	----	P0.0/AD0
44	----	V_{DD}

NC = No connection

FIGURE 1. Terminal connections.

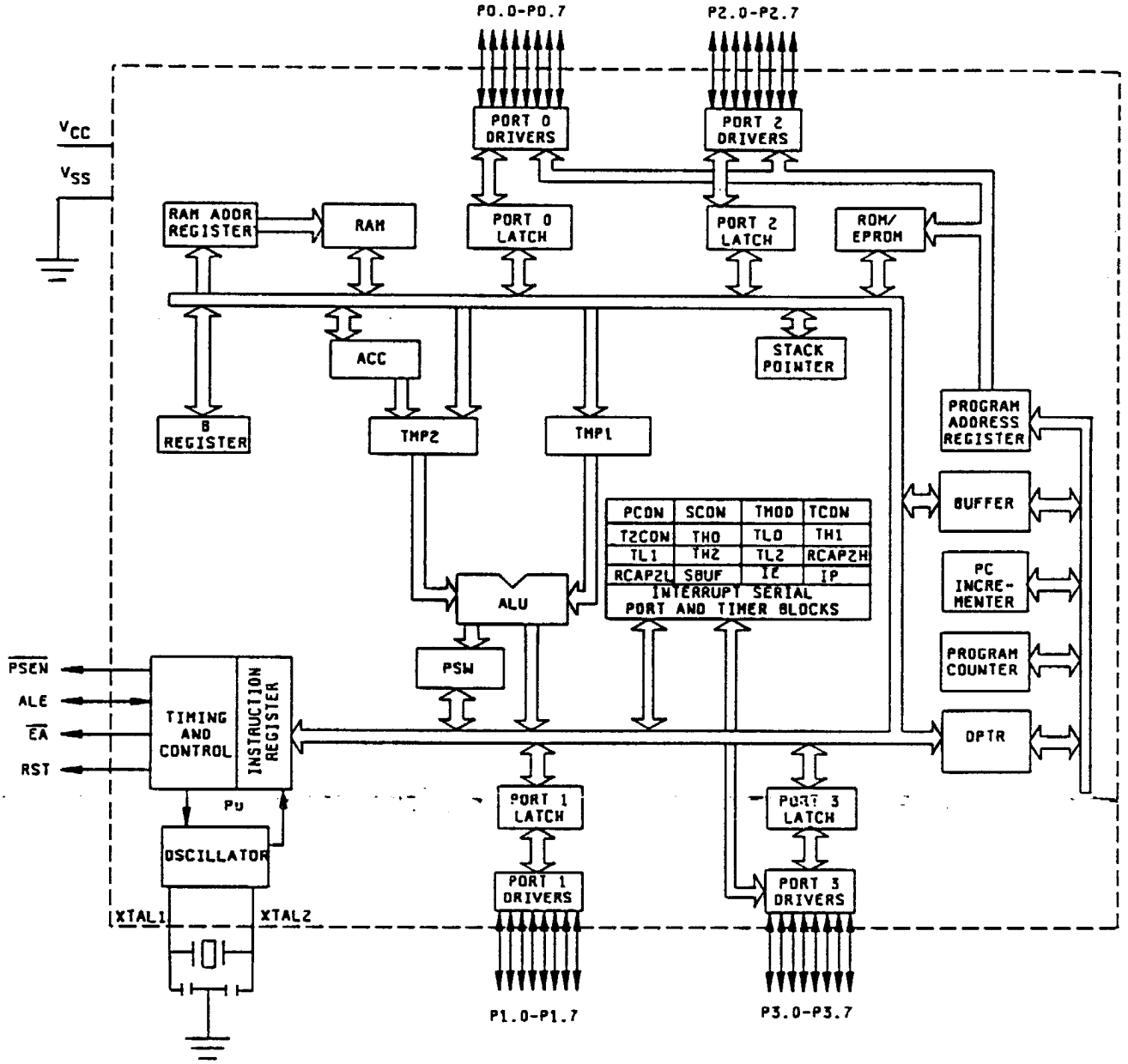
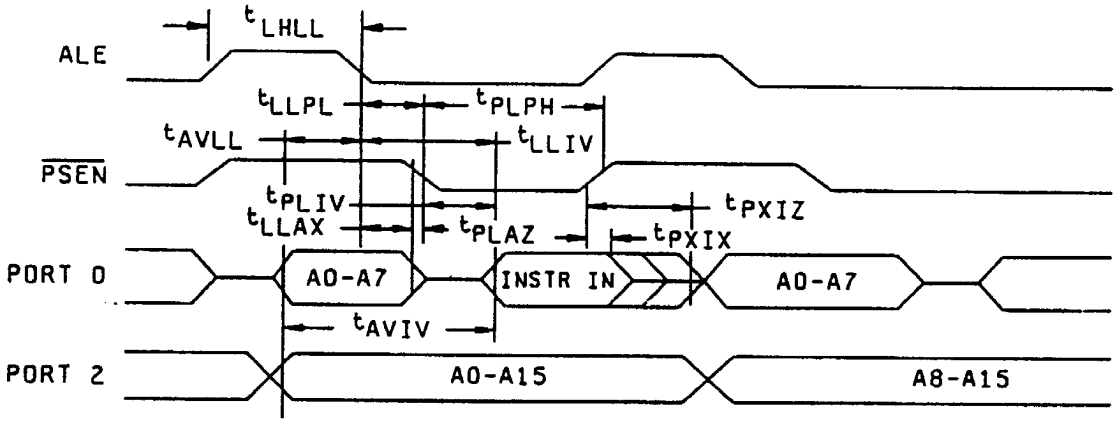
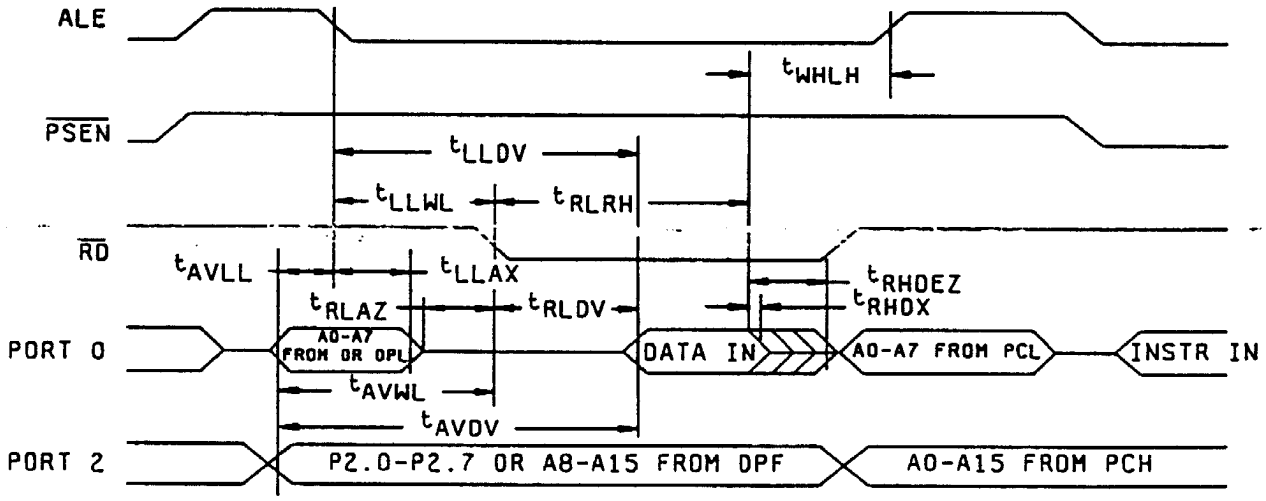


FIGURE 2. Block diagram.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91576
		REVISION LEVEL B	SHEET 14

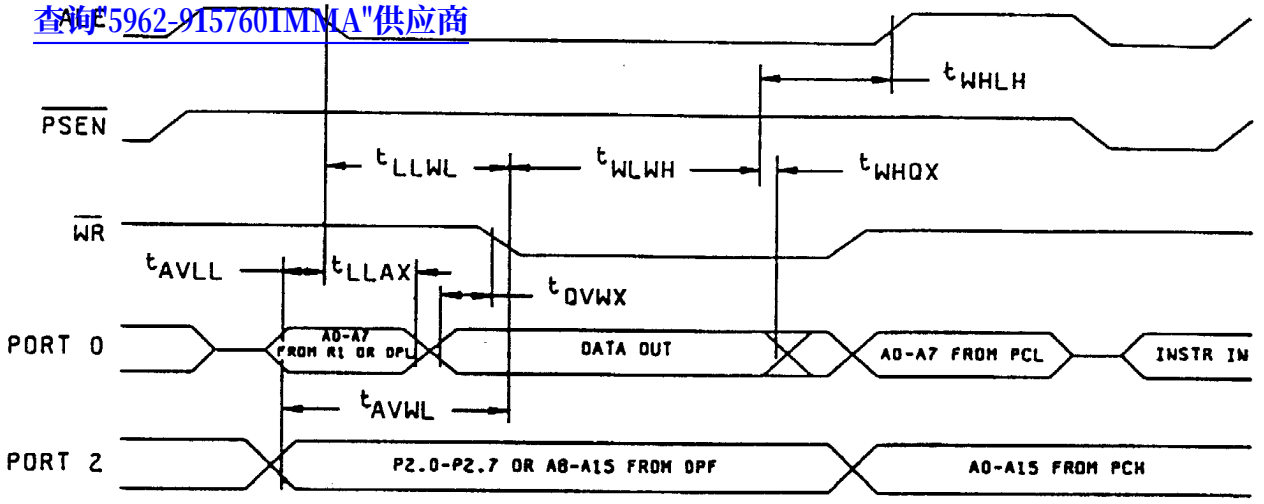


External Program Memory Read Cycle

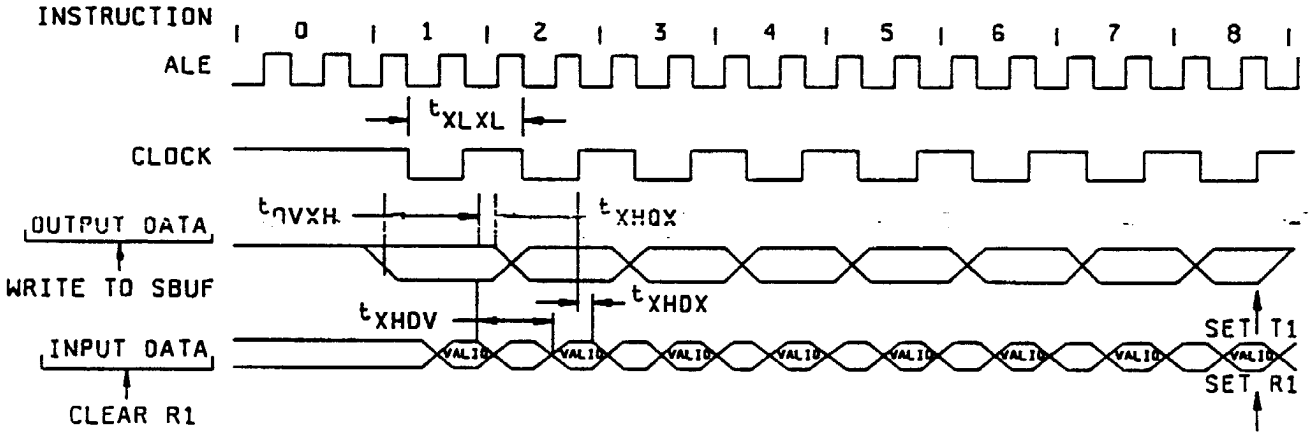


External Data Memory Read Cycle

FIGURE 3. Switching waveforms and test circuit.

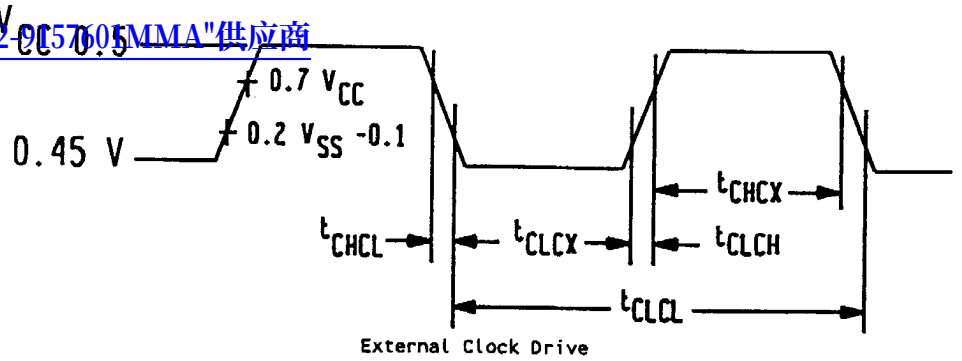


External Data Memory Write Cycle



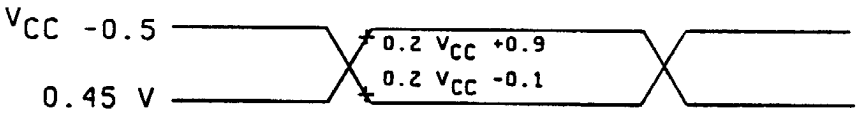
Shift Register Mode Timing

FIGURE 3. Switching waveforms and test circuit - Continued.



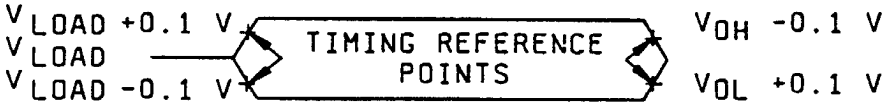
External Clock Drive

NOTE: AC: Testing
input and output waveforms



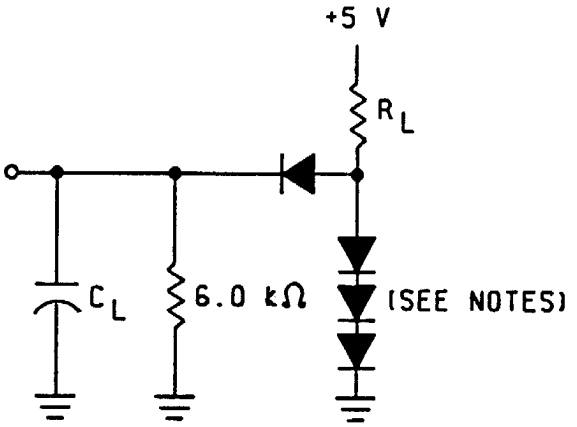
NOTE: AC inputs during testing are driven at V_{CC} -0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at V_{IH} minimum for a logic '1' and V_{IL} maximum for a logic '0'.

Float waveforms



NOTE: For timing purposes, a port pin ceases floating when a 100 mV change from load voltage occurs and begins floating when a 100 mV change from loaded V_{OH} or V_{OL} level occurs. I_{OL} or I_{OH} ≥ ±20 mA.

FIGURE 3. Switching waveforms and test circuit - Continued.



Output	R_L	C_L
Port 0, ALE, PSEN	1.2 kΩ	100 pF
All other outputs	2.4 kΩ	80 pF

NOTES:
1. All diodes are 1N914 or equivalent.
2. C_L includes tester and fixture capacitance.

Test circuit or equivalent

FIGURE 3. Switching waveforms and test circuit - Continued.

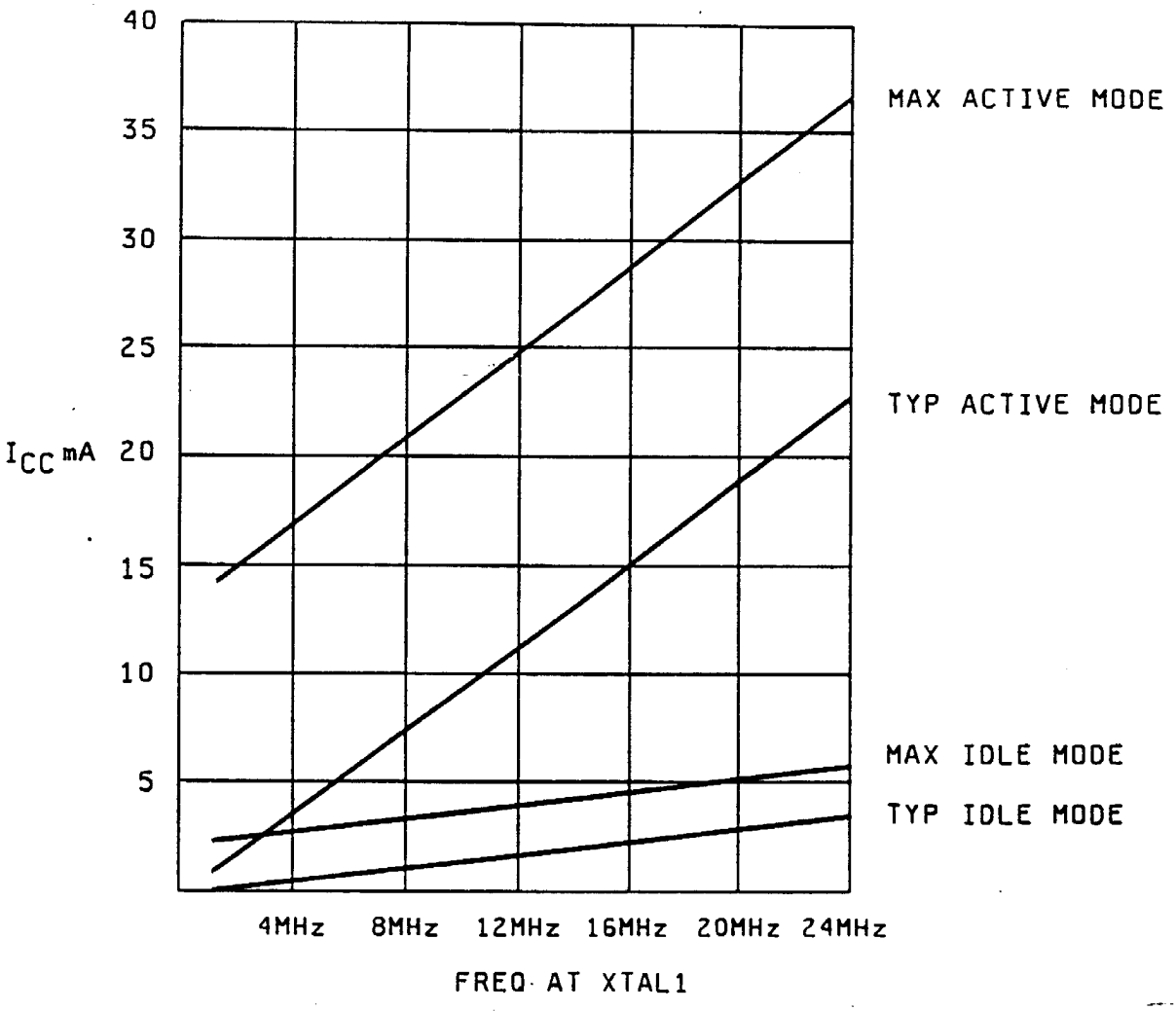


FIGURE 4. ICC versus frequency.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes N, Q, and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes N, Q, and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps:

Margin test method A.

(1) Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.12.2). The remaining cells shall provide a worst case speed pattern.

(2) Bake, unbiased, for 72 hours at 140°C to screen for data retention lifetime.

(3) Perform a margin test using V_m = 5.9 V at 25°C using loose timing (i.e., T_{ACC} > 1 µs).

(4) Perform dynamic burn-in (see 4.2.1a).

(5) Margin at V_m = 5.9 V.

(6) Perform electrical tests (see 4.2).

(7) Erase (see 3.11.1), except devices submitted for groups A, B, C, and D testing.

(8) Verify erasure (see 3.11.3).

Margin test method B.

(1) Program at +25°C, 100 percent of the bits.

(2) Bake, unbiased, for 24 hours at +250°C.

(3) Perform margin test at V_m = 5.9 V.

(4) Erase (see 3.11.1).

(5) Perform interim electrical tests in accordance with table II.

(6) For device types 01, and 02 program 100 percent of the bits and verify (see 3.11.2).

(7) Perform burn-in (see 4.2.1a).

(8) One-hundred percent test at 25°C (group A, subgroups 1 and 7). V_m = 5.9 V with loose timing, apply PDA for device types 03, 04, 05 and 06 the virgin state of the device must be verified.

(9) Perform remaining final electrical subgroups and group A testing.

(10) For device types 01, 02 erase, devices may be submitted for groups B, C, and D at this time.

(11) For device types 01, 02 verify erasure (see 3.11.3).

(12) Steps 1 through 4 are performed at wafer level.

4.2.2 Additional criteria for device classes N, Q, and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes N, Q, and V. Qualification inspection for device classes N, Q, and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes N, Q, and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes N, Q, and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes N, Q, and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)		
	Device class M	Device class N	Device class Q	Device class V
Interim electrical parameters (see 4.2)				1,7
Final electrical parameters (see 4.2)	1,2,3,7,8,9,10,11 1/	1,2,3,7,8, 9,10,11 1/	1,2,3,7,8, 9,10,11 1/	1,2,3,7,8, 9,10,11 2/
Group A test requirements (see 4.4)	1,2,3,4,7,8,9,10,11	1,2,3,4,7,8, 9,10,11	1,2,3,4,7,8, 9,10,11	1,2,3,4,7,8, 9,10,11
Group C end-point electrical parameters (see 4.4)	2,8A,10	2,8A,10	2,8A,10	2,8A,10
Group D end-point electrical parameters (see 4.4)	2,8A,10	2,8A,10	2,8A,10	2,8A,10
Group E end-point electrical parameters (see 4.4)	2,8A,10	2,8A,10	2,8A,10	2,8A,10

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes N, Q, and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes N, Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Erasing procedure. The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-s/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 µW/cm^2 rating for 20 to 30 minutes, at a distance of about 1 inch, should be sufficient.

4.6 Programming procedures. The programming characteristics in table III and the following procedures shall be used for programming the device.

a. Connect the device in the electrical configuration (see figure 5) for programming. The waveforms on figure 6 and programming characteristics of table III shall apply.

b. Initially and after each erasure, all bits are in the high "H" state. Information is introduced by selectively programming "L" into the desired bit locations. A programmed "L" can be changed to an "H" by ultraviolet light erasure (see 4.5).

TABLE III. Programming verification characteristics.

Parameter	Symbol	Conditions	Limits		Units
			Min	Max	
Programming supply voltage	V_{PP}	See figure 7 1/	12.5	13.0	V
Programming supply current	I_{PP}			50	mA
Oscillator frequency	t_{CLCL} 1/		4	6	MHz
Address setup to PROG low	2/ t_{AVGL}		$48t_{CLCL}$		ns
Address hold after PROG	2/ t_{GHAX}		$48t_{CLCL}$		
Data setup to $\overline{\text{PROG}}$ low	2/ t_{DVGL}		$48t_{CLCL}$		
Data hold after PROG	2/ t_{GHDX}		$48t_{CLCL}$		
P2.7 ($\overline{\text{ENABLE}}$) high to V_{PP}	2/ t_{EHSH}		$48t_{CLCL}$		
V_{PP} setup to $\overline{\text{PROG}}$ low	2/ t_{SHGL}		10		µs
V_{PP} hold after $\overline{\text{PROG}}$	2/ t_{GSHL}		10		
$\overline{\text{PROG}}$ width	2/ t_{GLGH}		90	110	
Address to data	2/ t_{AVQV}			$48t_{CLCL}$	ns
$\overline{\text{ENABLE}}$ low to data valid	2/ t_{ELQV}			$48t_{CLCL}$	
Data float after $\overline{\text{ENABLE}}$	2/ t_{EHQZ}		0	$48t_{CLCL}$	
$\overline{\text{PROG}}$ high to $\overline{\text{PROG}}$ low	2/ t_{GHGL}		10		µs

1/ For programming specifications, T_C = 21°C to 27°C, V_{CC} = 5 V ±10 percent, V_{SS} = 0 V.

2/ Due to test equipment limitations, actual tested values may differ from those specified, but specified limits are guaranteed.

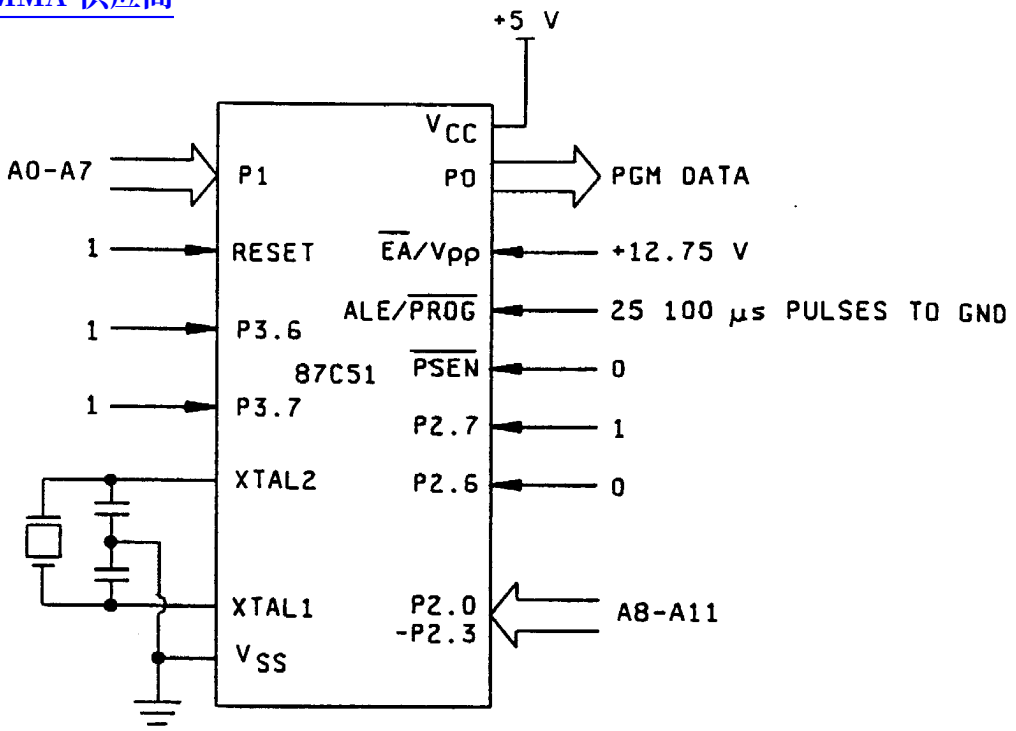


FIGURE 5. Program configuration.

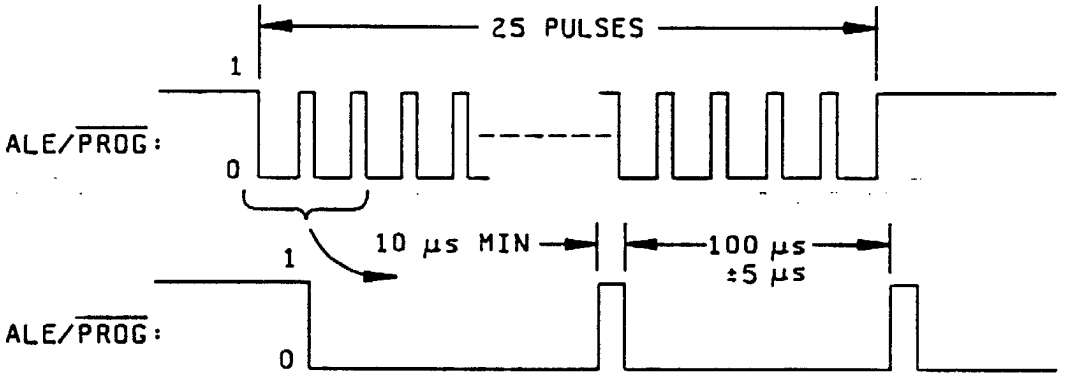
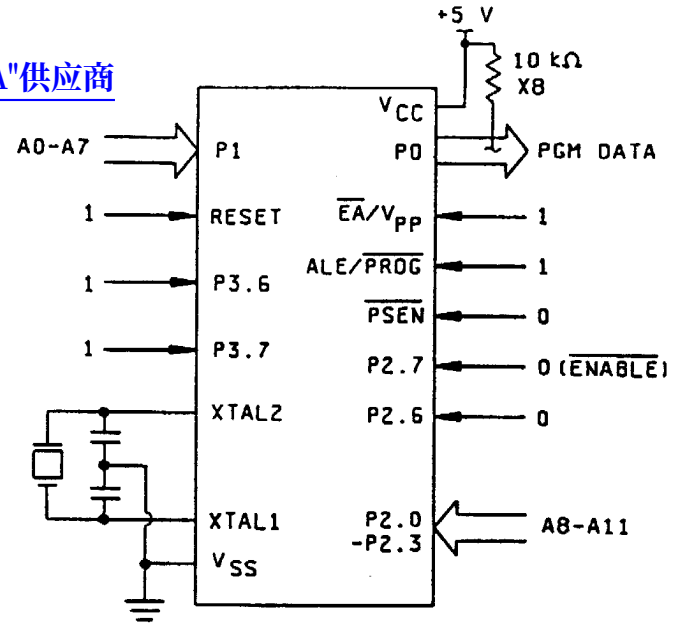


FIGURE 6. Programming waveforms.



EPROM PROGRAMMING AND VERIFICATION WAVEFORMS

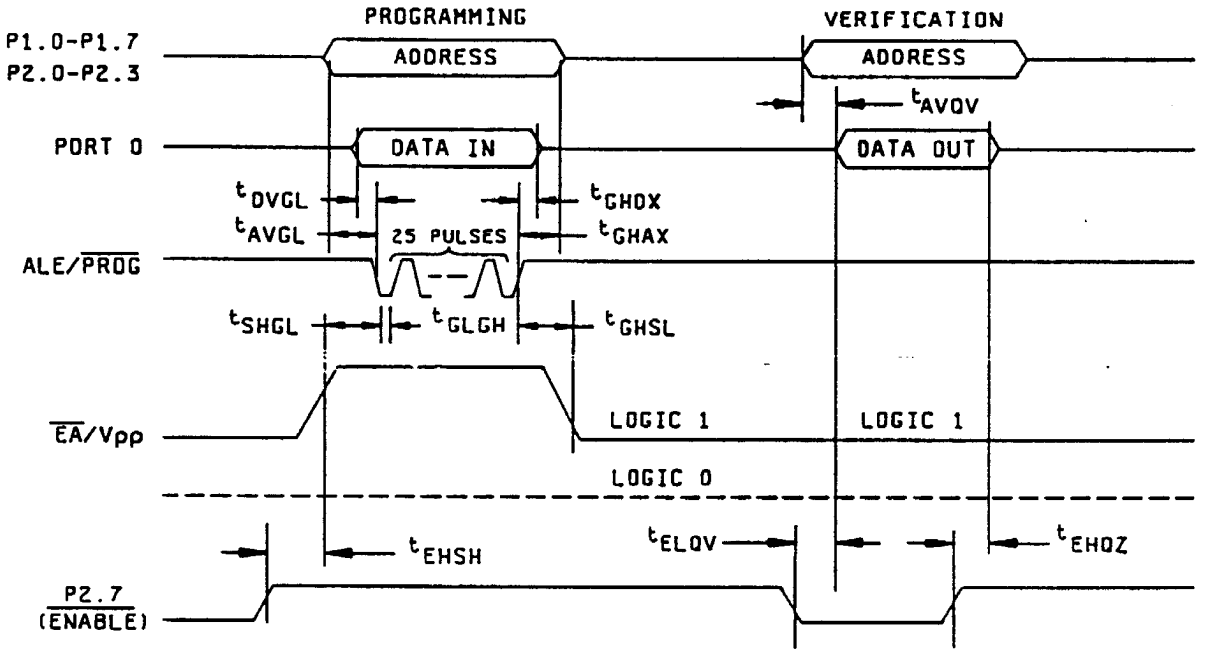


FIGURE 7. Programming verification.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes N, Q, and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Symbols, definitions, and functional descriptions.

Mnemonic	Type	Name and function
V_{SS}		GROUND: 0 V reference
V_{CC}		Power Supply: + 5 V
P0.0-P0.7	I/O	Port 0: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification in the device. External pull-ups are required during program verification.
P1.0-P1.7	I/O	Port 1. Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Pins P1.0 and P1.1 also. Port 1 also receives the low-order address byte during program memory verification. Port 1 also serves alternate functions for timer 2:
	I	T2 (P1.0): Timer/counter 2 external count input.
	I	T2EX (P1.1): Timer/counter 2 trigger input.
P2.0-P2.7	I/O	Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX@DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register.

Mnemonic	Type	Name and function - Continued.
P3.0-P3.7	I/O	Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1's written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (see DC Electrical Characteristics: I_{IL}). Port 3 also serves the special features of the MCS-51 family, as listed below:
	I	RxD (P3.0): Serial input port
	O	TxD (P3.1): Serial output port
	I	INT0 (P3.2): External interrupt
	I	INT1 (P3.3): External interrupt
	I	T0 (P3.4): Timer 0 external input
	I	T1 (P3.5): Timer 1 external input
	O	WR (P3.6): External data memory write strobe
	O	RD (P3.7): External data memory read strobe.
RST	I	Reset: A high on this pin for two machine cycles while the oscillator is running, resetsthe device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC}.
ALE/$\overline{PROG}$	I/O	Address Latch Enable/Program Pulse: Output pulse for latching the low byte of the address during ac access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input (PROG) during EPROM programming.
$\overline{PSEN}$	O	Program Store Enable: The read strobe to external program memory. When the device is executing code from the external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory. PSEN is not activated during fetches from internal program memory.
$\overline{EA}/V_{PP}$		External Access Enable/Programming Supply Voltage: EA must be externally held low to enable the device to fetch from internal program memory locations 0000H to 1FFFH. If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than 1FFFH. This pin also receives the 12.75 V programming supply voltage (V_{PP}) during EPROM programming.
XTAL1	I	Crystal 1: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	O	Crystal 2: Output from the inverting oscillator amplifier.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part-number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(N, Q, or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes N, Q, and V. Sources of supply for device classes N, Q, and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 96-06-26

Approved sources of supply for SMD 5962-91576 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standard microcircuit drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-9157601MMA	18324	87C52/BMA
5962-9157601MQA	18324	87C52/BQA
5962-9157601MUA	18324	87C52/BUA
5962-9157602MMA	18324	87C52-16/BMA
5962-9157602MQA	18324	87C52-16/BQA
5962-9157602MUA	18324	87C52-16/BUA
5962-9157603MMA	18324	87C52/BMA-OT
5962-9157603MQA	18324	87C52/BQA-OT
5962-9157603MUA	18324	87C52/BUA-OT
5962-9157603NXA	18324	87C52/CN40A
5962-9157603NYA	18324	87C52/CA44A
5962-9157604MMA	18324	87C52-16/BMA-OT
5962-9157604MQA	18324	87C52-16/BQA-OT
5962-9157604MUA	18324	87C52-16/BUA-OT
5962-9157604NXA	18324	87C52-16/CN40A
5962-9157604NYA	18324	87C52-16/CA44A
5962-9157605NXA	18324	87C52/IN40A
5962-9157605NYA	18324	87C52/IA44A
5962-9157606NXA	18324	87C52-16/IN40A
5962-9157606NYA	18324	87C52-16/IA44A

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
18324	Philips Semiconductors 811 East Arques Avenue Sunnyvale, CA 94088-3409

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