

# Power MOSFET

## 3.0 A, 60 V, Logic Level, N-Channel SOT-223

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

### Features

- Pb-Free Packages are Available

### Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

### MAXIMUM RATINGS (T<sub>C</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V <sub>DSS</sub>	60	Vdc
Drain-to-Gate Voltage (R <sub>GS</sub> = 1.0 MΩ)	V <sub>DGR</sub>	60	Vdc
Gate-to-Source Voltage	V <sub>GS</sub>	± 15	Vdc
– Continuous		± 20	Vpk
– Non-repetitive (t <sub>p</sub> ≤ 10 ms)			
Drain Current	I <sub>D</sub>	3.0	Adc
– Continuous @ T <sub>A</sub> = 25°C		1.4	Apk
– Continuous @ T <sub>A</sub> = 100°C		9.0	
– Single Pulse (t <sub>p</sub> ≤ 10 μs)	I <sub>DM</sub>		
Total Power Dissipation @ T <sub>A</sub> = 25°C (Note 1)	P <sub>D</sub>	2.1	Watts
Total Power Dissipation @ T <sub>A</sub> = 25°C (Note 2)		1.3	Watts
Derate above 25°C		0.014	W/°C
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	–55 to 175	°C
Single Pulse Drain-to-Source Avalanche Energy – Starting T <sub>J</sub> = 25°C (V <sub>DD</sub> = 25 Vdc, V <sub>GS</sub> = 5.0 Vdc, I <sub>L(pk)</sub> = 7.0 Apk, L = 3.0 mH, V <sub>DS</sub> = 60 Vdc)	E <sub>AS</sub>	74	mJ
Thermal Resistance	R <sub>θJA</sub>	72.3	°C/W
– Junction-to-Ambient (Note 1)		114	
– Junction-to-Ambient (Note 2)			
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T <sub>L</sub>	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

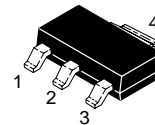
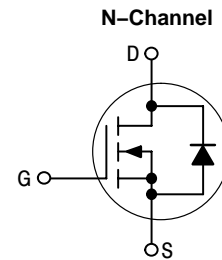
1. When surface mounted to an FR4 board using 1" pad size, 1 oz. (Cu. Area 0.0995 in<sup>2</sup>).
2. When surface mounted to an FR4 board using minimum recommended pad size, 2–2.4 oz. (Cu. Area 0.272 in<sup>2</sup>).



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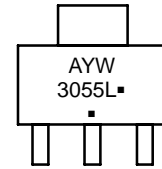
**3.0 A, 60 V**  
**R<sub>DS(on)</sub> = 120 mΩ**



**SOT-223**  
**CASE 318E**  
**STYLE 3**

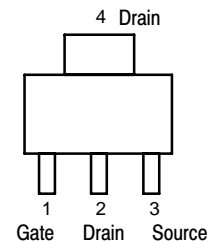
### MARKING DIAGRAM

3055L = Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
▪ = Pb-Free Package



(Note: Microdot may be in either location)

### PIN ASSIGNMENT



### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

**Preferred** devices are recommended choices for future use and best overall value.

# NTF3055L108

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

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Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 250 μAdc) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	60 -	68 68	- -	Vdc mV/°C
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 60 Vdc, V <sub>GS</sub> = 0 Vdc) (V <sub>DS</sub> = 60 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 150°C)	I <sub>DSS</sub>	- -	- -	1.0 10	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = ± 15 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	-	-	± 100	nAdc

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μAdc) Threshold Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	1.0 -	1.68 4.6	2.0 -	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 3) (V <sub>GS</sub> = 5.0 Vdc, I <sub>D</sub> = 1.5 Adc)	R <sub>DS(on)</sub>	-	92	120	mΩ
Static Drain-to-Source On-Resistance (Note 3) (V <sub>GS</sub> = 5.0 Vdc, I <sub>D</sub> = 3.0 Adc) (V <sub>GS</sub> = 5.0 Vdc, I <sub>D</sub> = 1.5 Adc, T <sub>J</sub> = 150°C)	V <sub>DS(on)</sub>	-	0.290 0.250	0.43 -	Vdc
Forward Transconductance (Note 3) (V <sub>DS</sub> = 7.0 Vdc, I <sub>D</sub> = 3.0 Adc)	g <sub>fs</sub>	-	5.7	-	Mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 25 Vdc, V <sub>GS</sub> = 0 V, f = 1.0 MHz)	C <sub>iss</sub>	-	313	440	pF
Output Capacitance		C <sub>oss</sub>	-	112	160	
Transfer Capacitance		C <sub>rss</sub>	-	40	60	

### SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	(V <sub>DD</sub> = 30 Vdc, I <sub>D</sub> = 3.0 Adc, V <sub>GS</sub> = 5.0 Vdc, R <sub>G</sub> = 9.1 Ω) (Note 3)	t <sub>d(on)</sub>	-	11	25	ns
Rise Time		t <sub>r</sub>	-	35	70	
Turn-Off Delay Time		t <sub>d(off)</sub>	-	22	45	
Fall Time		t <sub>f</sub>	-	27	60	
Gate Charge	(V <sub>DS</sub> = 48 Vdc, I <sub>D</sub> = 3.0 Adc, V <sub>GS</sub> = 5.0 Vdc) (Note 3)	Q <sub>T</sub>	-	7.6	15	nC
		Q <sub>1</sub>	-	1.4	-	
		Q <sub>2</sub>	-	4.0	-	

### SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I <sub>S</sub> = 3.0 Adc, V <sub>GS</sub> = 0 Vdc) (I <sub>S</sub> = 3.0 Adc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 150°C) (Note 3)	V <sub>SD</sub>	- -	0.87 0.72	1.0 -	Vdc
Reverse Recovery Time	(I <sub>S</sub> = 3.0 Adc, V <sub>GS</sub> = 0 Vdc, dI <sub>S</sub> /dt = 100 A/μs) (Note 3)	t <sub>rr</sub>	-	35	-	ns
		t <sub>a</sub>	-	21	-	
		t <sub>b</sub>	-	14	-	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	-	0.044	-	μC

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

4. Switching characteristics are independent of operating junction temperatures.

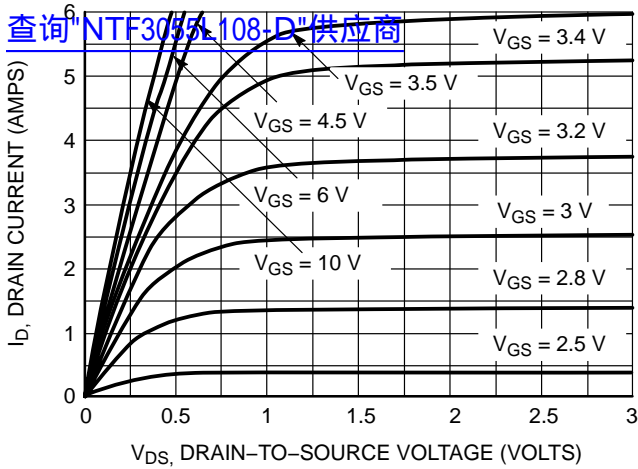


Figure 1. On-Region Characteristics

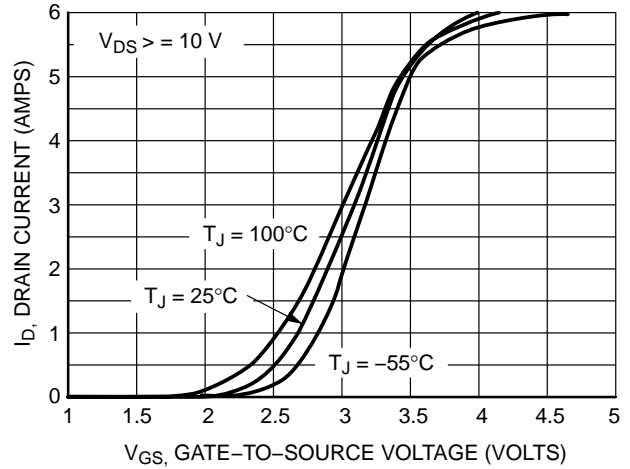


Figure 2. Transfer Characteristics

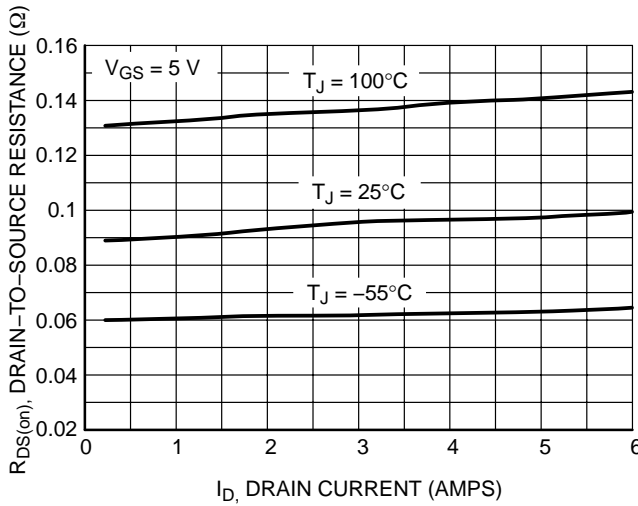


Figure 3. On-Resistance vs. Gate-to-Source Voltage

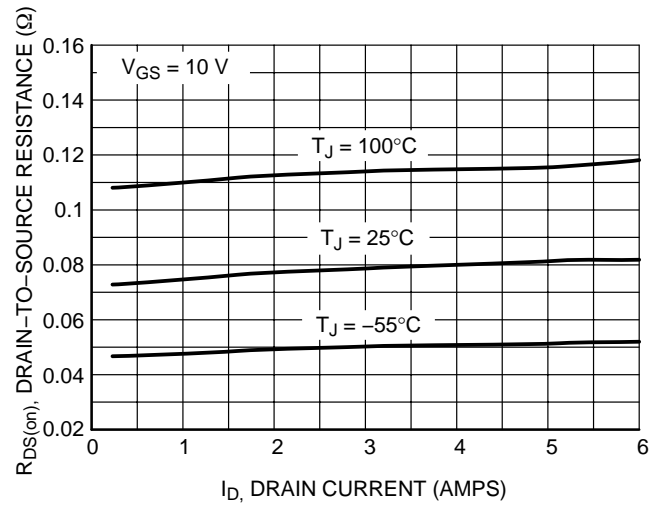


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

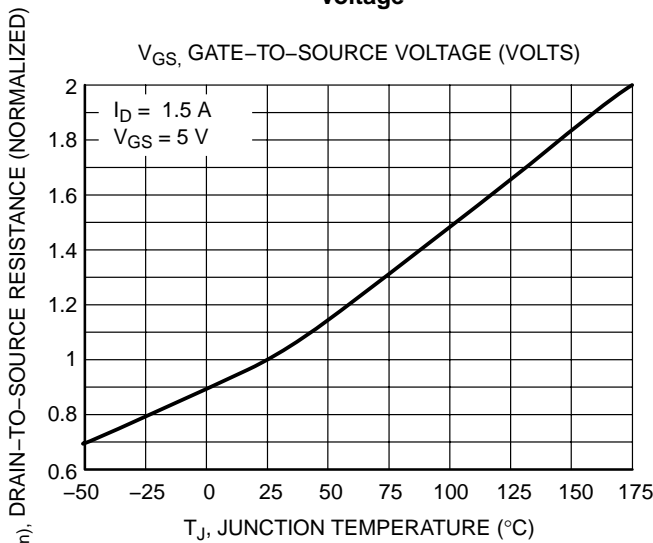


Figure 5. On-Resistance Variation with Temperature

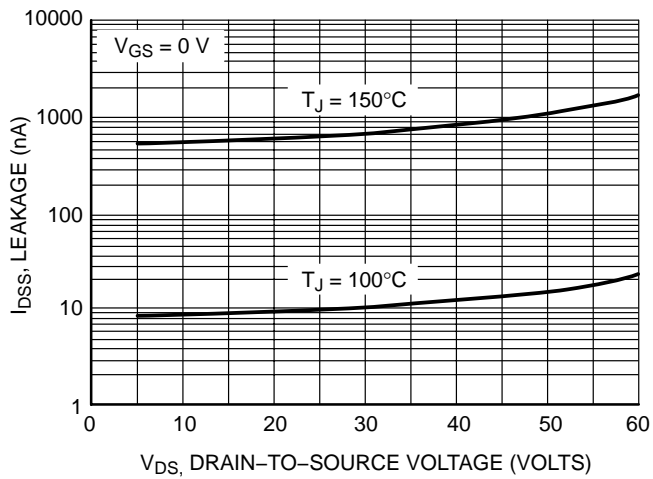


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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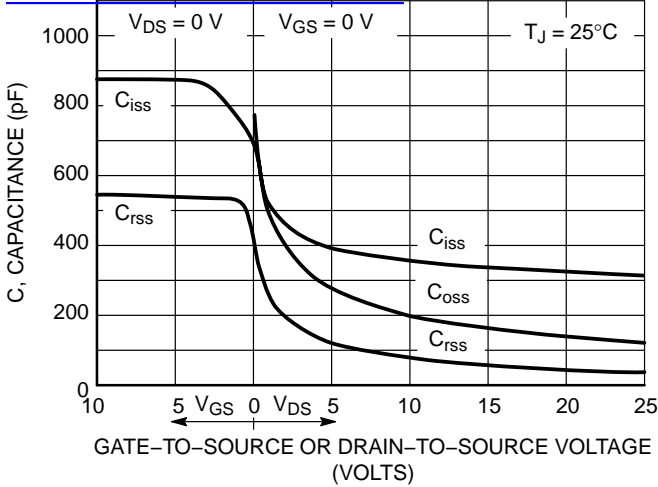


Figure 7. Capacitance Variation

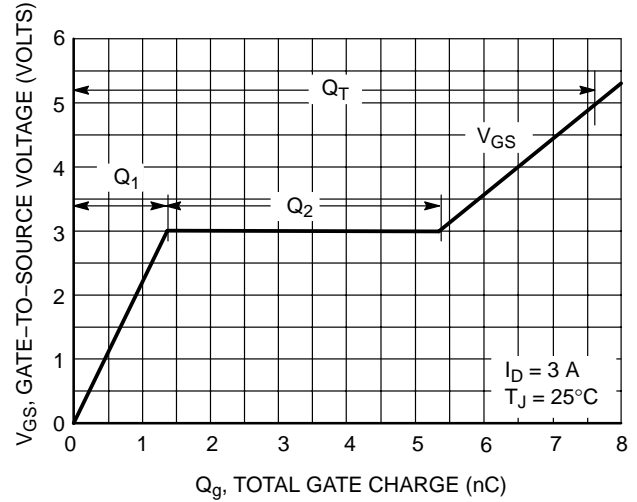


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

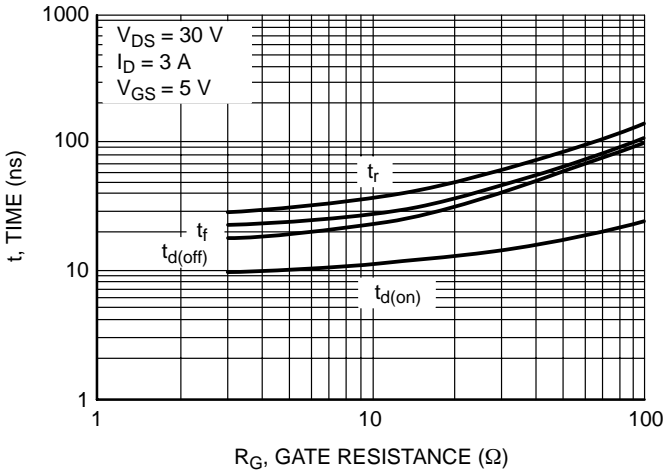


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

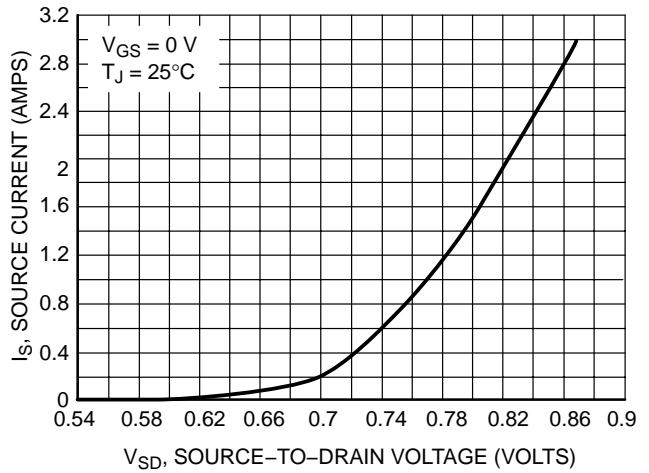


Figure 10. Diode Forward Voltage vs. Current

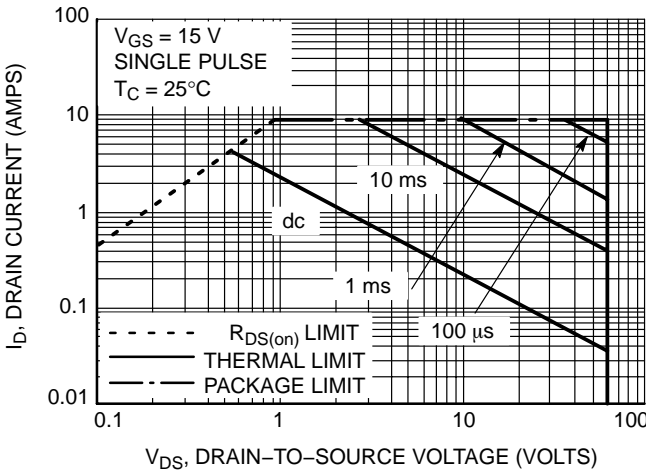


Figure 11. Maximum Rated Forward Biased Safe Operating Area

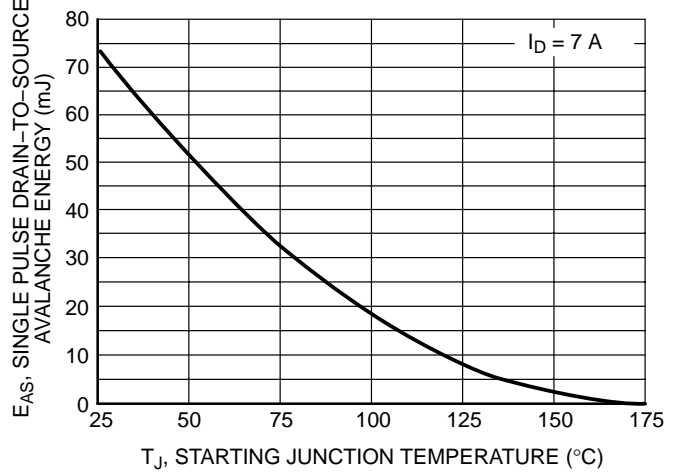


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

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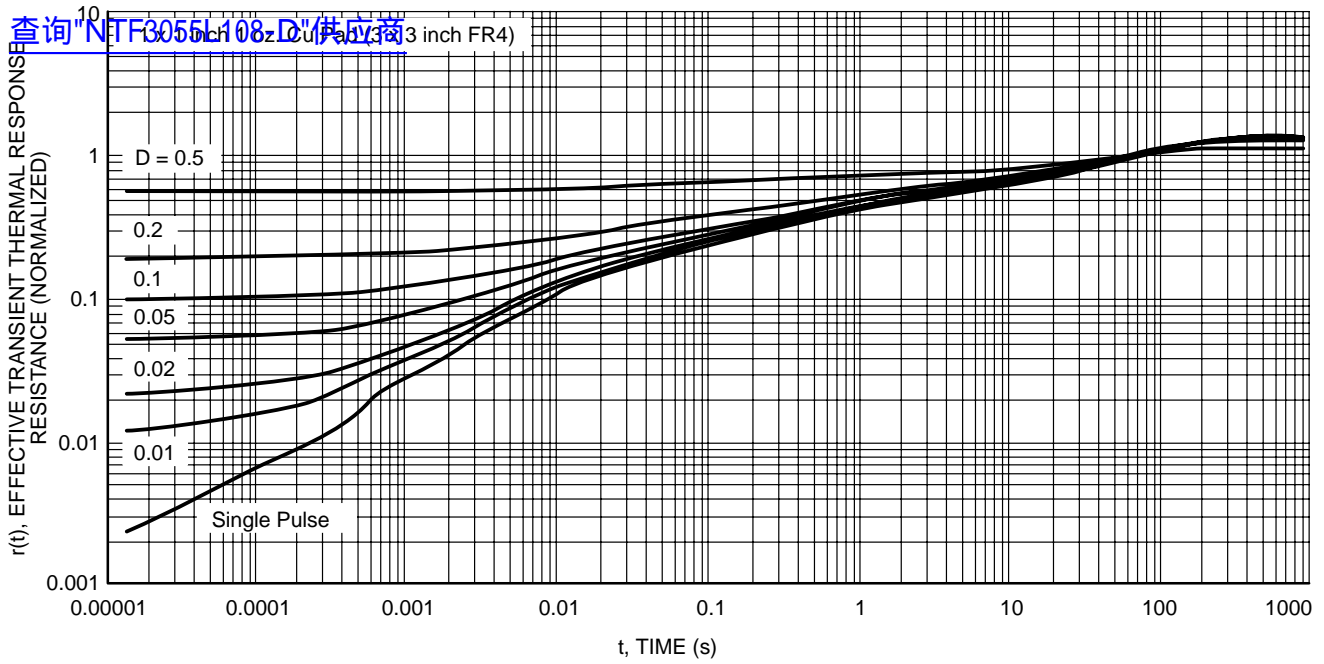


Figure 13. Thermal Response

## ORDERING INFORMATION

Device	Package	Shipping†
NTF3055L108T1	SOT-223 (TO-261)	1000 / Tape & Reel
NTF3055L108T1G	SOT-223 (TO-261) (Pb-Free)	1000 / Tape & Reel
NTF3055L108T3	SOT-223 (TO-261)	4000 / Tape & Reel
NTF3055L108T3G	SOT-223 (TO-261) (Pb-Free)	4000 / Tape & Reel
NTF3055L108T3LF	SOT-223 (TO-261)	4000 / Tape & Reel
NTF3055L108T3LFG	SOT-223 (TO-261) (Pb-Free)	4000 / Tape & Reel

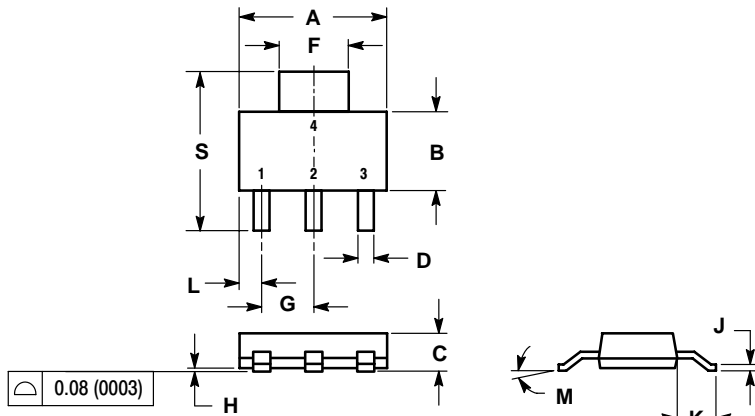
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTF3055L108

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## PACKAGE DIMENSIONS

SOT-223 (TO-261)  
CASE 318E-04  
ISSUE K

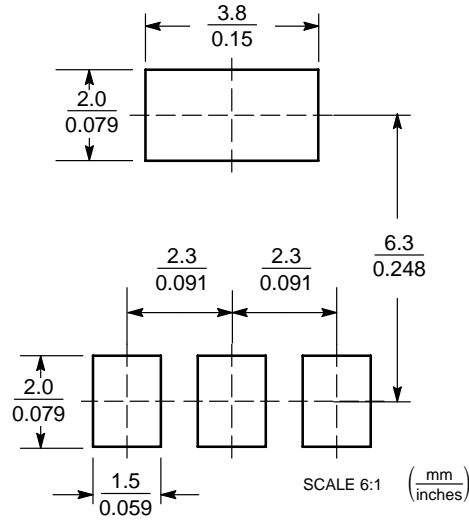


- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.249	0.263	6.30	6.70
B	0.130	0.145	3.30	3.70
C	0.060	0.068	1.50	1.75
D	0.024	0.035	0.60	0.89
F	0.115	0.126	2.90	3.20
G	0.087	0.094	2.20	2.40
H	0.0008	0.0040	0.020	0.100
J	0.009	0.014	0.24	0.35
K	0.060	0.078	1.50	2.00
L	0.033	0.041	0.85	1.05
M	0 <sup>°</sup>	10 <sup>°</sup>	0 <sup>°</sup>	10 <sup>°</sup>
S	0.264	0.287	6.70	7.30

- STYLE 3:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

### SOLDERING FOOTPRINT\*



### SOT-223

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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