查询"TPS61310"供应商

1.5A Multiple LED Camera Flash and Video Light Driver With I²C™ Compatible Interface

Check for Samples: TPS61310

FEATURES

- **Operational Modes:**
  - **Video Light and Flash Strobe**
  - **Voltage Regulated Converter: 3.8V...5.7V with Down Mode**
  - **Standby: 2μA (typ.)**
- **LED V_F Measurement**
- **Power-Save Mode for Improved Efficiency at Low Output Power, Up to 95% Efficiency**
- **I²C Compatible Interface up to 3.4Mbits/s**
- **Dual Wire Camera Module Interface**
- **Zero Latency Tx-Masking Input**
- **Hardware Reset Input**
- **Privacy Indicator LED Output**
- **GPIO/Power Good Output**
- **Various Safe Operation and Robust Handling Features:**
  - **LED Temperature Monitoring**
  - **Open/Short LED Detection/Protection**
  - **Integrated LED Safety Timer**
  - **Automatic Battery Voltage Droop Monitoring and Protection**
  - **Smooth LED Current Ramp-Up/Down**
  - **Undervoltage Lockout**
- **Total Solution Size of Less Than 25mm²**
- **Available in a 20-Pin NanoFree™ (CSP)**

APPLICATIONS

- **Single/Dual/Triple White LED Flash Supply for Cell Phones and Smart-Phones**
- **Video Lighting for Digital Video Applications**
- **General Lighting Applications**
- **Audio Amplifier Power Supply**

DESCRIPTION

The TPS6131x family is an integrated solution with a wide feature set for driving up to three LEDs for still-camera flash strobe and video-camera lighting applications. It is based on a high efficiency synchronous boost topology with combinable current sinks to drive up to three white LEDs in parallel. The 2MHz switching frequency allows the use of small and low-profile 2.2μH inductors. To optimize overall efficiency, the device operates with a low LED-feedback voltage and regulated output-voltage adaptation.

The device integrates a control scheme that automatically optimizes the LED current flash budget as a function of the battery voltage condition.

The TPS6131x not only operates as a regulated current source, but also as a standard voltage boost regulator. The device enters power-save mode operation at light load currents to maintain high efficiency over the entire load current range. These operating modes can be useful to supply other high power devices in the system (e.g. hands-free audio PA).

To simplify video light and flash synchronization with the camera module, the device offers a dedicated control interface (STRB0, STRB1) for zero latency LED turn-on time.

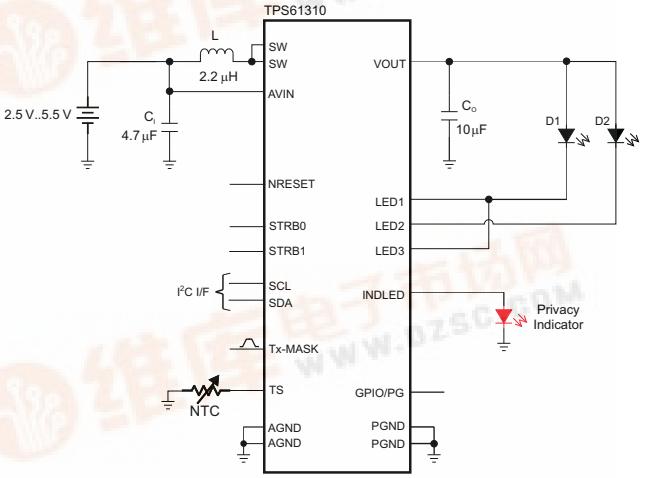


Figure 1. Typical Application

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.
I²C is a trademark of NXP Semiconductors.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2010, Texas Instruments Incorporated

pdf.dzsc.com

查询 TPS61310 供应商

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Table 1. AVAILABLE OPTIONS

PART NUMBER(1)	PACKAGE MARKING	PACKAGE	DEVICE SPECIFIC FEATURES(2)
TPS61310YFF	TPS61310	CSP-20	

(1) The YFF package is available in tape and reel. Add R suffix (TPS6131xYFFR) to order quantities of 3000 parts per reel, T suffix for 250 parts per reel.
(2) For more details, refer to the section *Application Diagrams*.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
V_I	Voltage range on AVIN, VOUT, SW, LED1, LED2, LED3(2)	–0.3 to 7	V
	Voltage range on SCL, SDA, STRB0, STRB1, NRESET, GPIO/PG(2)	–0.3 to 7	V
	Voltage range on Tx-MASK, TS (2)	–0.3 to 7	V
	Current on GPIO/PG	±25	mA
	Power dissipation	Internally limited	
T_A (3)	Operating ambient temperature range	–40 to 85	°C
$T_{J\ (MAX)}$	Maximum operating junction temperature	150	°C
T_{stg}	Storage temperature range	–65 to 150	°C
ESD rating (4)	Human body model	2	kV
	Charge device model	500	V
	Machine model	100	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} – (\theta_{JA} \times P_{D(max)})$
(4) The human body model is a 100-pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin.

DISSIPATION RATINGS

PACKAGE	THERMAL RESISTANCE(1) θ_{JA}	THERMAL RESISTANCE(1) θ_{JB}	POWER RATING T_A = 25°C	DERATING FACTOR ABOVE(2) T_A = 25°C
YFF	71°C/W	21°C/W	1.4 W	14mW/°C

(1) Simulated with high-K board
(2) Maximum power dissipation is a function of $T_J(max)$, θ_{JA} and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_A)/ \theta_{JA}$.

Copyright © 2010, Texas Instruments Incorporated

查询"TPS61310"供应商

ELECTRICAL CHARACTERISTICS

Unless otherwise noted the specification applies for V_{IN} = 3.6V over an operating junction temp. –40°C ≤ T_J ≤ 125°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are for T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{IN}	Input voltage range		2.5		5.5	V
I_Q	Operating quiescent current into AVIN	I_{OUT} = 0 mA, device not switching (Power Safe Mode) –40°C ≤ T_J ≤ +85°C		590	700	µA
		$I_{OUT(DC)}$ = 0mA, PWM operation V_{OUT} = 4.95V, voltage regulation mode		11.3		mA
I_{SD}	Shutdown current	–40°C ≤ T_J ≤ +85°C		1	5	µA
V_{UVLO}	Undervoltage lockout threshold (analog circuitry)	V_{IN} falling		2.3	2.35	V
OUTPUT						
V_{OUT}	Output voltage range	Current regulation mode	VIN		5.5	V
		Voltage regulation mode	3.825		5.7	V
	Internal feedback voltage accuracy	2.5V ≤ V_{IN} ≤ 4.8V, –20°C ≤ T_J ≤ +125°C Boost mode, PWM voltage regulation	–2%		2%	
	Power-save mode ripple voltage	I_{OUT} = 10 mA		0.015 V_{OUT}		V_{P-P}
OVP	Output overvoltage protection	V_{OUT} rising, 0000 ≤ OV[3:0] ≤ 0100	4.5	4.65	4.8	V
		V_{OUT} rising, 0101 ≤ OV[3:0] ≤ 1111	5.8	6.0	6.2	V
	Output overvoltage protection hysteresis	V_{OUT} falling		0.15		V
POWER SWITCH						
$r_{DS(on)}$	Switch MOSFET on-resistance	V_{OUT} = V_{GS} = 3.6 V		90		mΩ
	Rectifier MOSFET on-resistance	V_{OUT} = V_{GS} = 3.6 V		135		mΩ
$I_{lkg(SW)}$	Leakage into SW	V_{OUT} = 0V, SW = 3.6V, –40°C ≤ T_J ≤ +85°C		0.3	4	µA
I_{lim}	Rectifier valley current limit (open-loop)	VOUT = 4.95V –20°C ≤ T_J ≤ +85°C PWM operation, relative to selected ILIM	–15		+15	%
OSCILLATOR						
f_{OSC}	Oscillator frequency			1.92		MHz
f_{ACC}	Oscillator frequency		–10		+7	%
THERMAL SHUTDOWN, HOT DIE DETECTOR						
	Thermal shutdown(1)		140	160		°C
	Thermal shutdown hysteresis(1)			20		°C
	Hot die detector accuracy(1)		–8		8	°C

(1) Verified by characterization. Not tested in production.

Copyright © 2010, Texas Instruments Incorporated

查询"TPS61310"供应商

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise noted the specification applies for V_{IN} = 3.6V over an operating junction temp. –40°C ≤ T_J ≤ 125°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are for T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LED CURRENT REGULATOR						
	LED1/3 current accuracy(1)	0.4V ≤ $V_{LED1/3}$ ≤ 2.0V, 0mA ≤ $I_{LED1/3}$ ≤ 100mA, T_J = +85°C	–10		+10	%
		0.4V ≤ $V_{LED1/3}$ ≤ 2.0V, 100mA < $I_{LED1/3}$ ≤ 400mA, T_J = +85°C	–7.5		+7.5	%
	LED2 current accuracy(1)	0.4V ≤ V_{LED2} ≤ 2.0V, 0mA ≤ I_{LED2} ≤ 250mA, T_J = +85°C	–10		+10	%
		0.4V ≤ V_{LED2} ≤ 2.0V, 250mA ≤ I_{LED2} ≤ 800mA, T_J = +85°C	–7.5		+7.5	%
	LED1/3 current matching(1)		–10		+10	%
	LED1/2/3 current temperature coefficient			0.05		%/°C
	INDLED current accuracy	1.5V ≤ (V_{IN}-V_{INDLED}) ≤ 2.5V 2.6mA ≤ I_{INDLED} ≤ 15.8mA, T_J = +25°C	–20		+20	%
	INDLED current temperature coefficient			0.05		%/°C
V_{DO}	LED1/2/3 sense voltage	I_{LED1-3} = full-scale current		400		mV
	VOUT dropout voltage	I_{OUT} = -15.8mA, device not switching			200	mV
	LED1/2/3 input leakage current	$V_{LED1/2/3}$ = V_{OUT} = 5V, –40°C ≤ T_J ≤ +85°C		0.1	4	µA
	INDLED input leakage current	V_{INDLED} = 0V, –40°C ≤ T_J ≤ +85°C		0.1	1	µA
LED TEMPERATURE MONITORING						
$I_{O(TS)}$	Temperature Sense Current Source	Thermistor bias current		23.8		µA
	TS Resistance (Warning Temperature)	LEDWARN bit = 1	39	44.5	50	kΩ
	TS Resistance (Hot Temperature)	LEDHOT bit = 1	12.5	14.5	16.5	kΩ
SDA, SCL, GPIO/PG, Tx-MASK, STRB0, STRB1, NRESET						
$V_{(IH)}$	High-level input voltage		1.2			V
$V_{(IL)}$	Low-level input voltage				0.4	V
$V_{(OL)}$	Low-level output voltage (SDA)	I_{OL} = 8mA			0.3	V
	Low-level output voltage (GPIO)	DIR = 1, I_{OL} = 5mA			0.3	V
$V_{(OH)}$	High-level output voltage (GPIO)	DIR = 1, GPIOTYPE = 0, I_{OH} = 8mA	V_{IN}–0.4			V
$I_{(LKG)}$	Logic input leakage current	Input connected to VIN or GND, –40°C ≤ T_J ≤ +85°C		0.01	0.1	µA
R_{PD}	STRB0, STRB1 pull-down resistance	STRB0, STRB1≤ 0.4 V		400		kΩ
	NRESET pull-down resistance	NRESET ≤ 0.4 V		400		kΩ
	Tx-MASK pull-down resistance	Tx-MASK ≤ 0.4 V		400		kΩ
$C_{(IN)}$	SDA Input Capacitance	SDA = VIN or GND		9		pF
	SCL Input Capacitance	SCL = VIN or GND		4		pF
	GPIO/PG Input Capacitance	DIR = 0, GPIO/PG = VIN or GND		9		pF
	STRB0 Input Capacitance	STRB0 = VIN or GND		3		pF
	STRB1 Input Capacitance	STRB1 = VIN or GND		3		pF
	NRESET Input Capacitance	NRESET = VIN or GND		3.5		pF
	Tx-MASK Input Capacitance	Tx-MASK = VIN or GND		4		pF

(1) Verified by characterization. Not tested in production.

Copyright © 2010, Texas Instruments Incorporated

查询"TPS61310"供应商

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise noted the specification applies for V_{IN} = 3.6V over an operating junction temp. –40°C ≤ T_J ≤ 125°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are for T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TIMING						
t_{NRESET}	Reset pulse width		10			µs
	Start-up time [ref to verified by char]	From shutdown into video light mode I_{LED} = 150mA		1.2		ms
	LED current settling time(1) triggered by a rising edge on STRB0	MODE_CTRL[1:0] = 10 I_{LED2} = from 0mA to 950mA		500		µs
	LED current settling time(1) triggered by Tx-MASK	MODE_CTRL[1:0] = 10 I_{LED2} = from 950mA to 150mA		20		µs

(1) Settling time to ±15% of the target value.

I²C INTERFACE TIMING CHARACTERISTICS(1)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$f_{(SCL)}$	SCL Clock Frequency	Standard mode		100	kHz
		Fast mode		400	kHz
		High-speed mode (write operation), C_B – 100pF max		3.4	MHz
		High-speed mode (read operation), C_B – 100pF max		3.4	MHz
		High-speed mode (write operation), C_B – 400pF max		1.7	MHz
		High-speed mode (read operation), C_B – 400pF max		1.7	MHz
t_{BUF}	Bus Free Time Between a STOP and START Condition	Standard mode	4.7		µs
		Fast mode	1.3		µs
t_{HD}, t_{STA}	Hold Time (Repeated) START Condition	Standard mode	4		µs
		Fast mode	600		ns
		High-speed mode	160		ns
t_{LOW}	LOW Period of the SCL Clock	Standard mode	4.7		µs
		Fast mode	1.3		µs
		High-speed mode, C_B – 100pF max	160		ns
		High-speed mode, C_B – 400pF max	320		ns
t_{HIGH}	HIGH Period of the SCL Clock	Standard mode	4		µs
		Fast mode	600		ns
		High-speed mode, C_B – 100pF max	60		ns
		High-speed mode, C_B – 400pF max	120		ns
t_{SU}, t_{STA}	Setup Time for a Repeated START Condition	Standard mode	4.7		µs
		Fast mode	600		ns
		High-speed mode	160		ns
t_{SU}, t_{DAT}	Data Setup Time	Standard mode	250		ns
		Fast mode	100		ns
		High-speed mode	10		ns
t_{HD}, t_{DAT}	Data Hold Time	Standard mode	0	3.45	µs
		Fast mode	0	0.9	µs
		High-speed mode, C_B – 100pF max	0	70	ns
		High-speed mode, C_B – 400pF max	0	150	ns
t_{RCL}	Rise Time of SCL Signal	Standard mode	20 + 0.1 C_B	1000	ns
		Fast mode	20 + 0.1 C_B	300	ns
		High-speed mode, C_B – 100pF max	10	40	ns
		High-speed mode, C_B – 400pF max	20	80	ns

(1) Specified by design. Not tested in production.

Copyright © 2010, Texas Instruments Incorporated

查询 TPS61310 供应商

I²C INTERFACE TIMING CHARACTERISTICS(1) (continued)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{RCL1}	Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge BIT	Standard mode	20 + 0.1 C_B	1000	ns
		Fast mode	20 + 0.1 C_B	300	ns
		High-speed mode, C_B – 100pF max	10	80	ns
		High-speed mode, C_B – 400pF max	20	160	ns
t_{FCL}	Fall Time of SCL Signal	Standard mode	20 + 0.1 C_B	300	ns
		Fast mode	20 + 0.1 C_B	300	ns
		High-speed mode, C_B – 100pF max	10	40	ns
		High-speed mode, C_B – 400pF max	20	80	ns
t_{RDA}	Rise Time of SDA Signal	Standard mode	20 + 0.1 C_B	1000	ns
		Fast mode	20 + 0.1 C_B	300	ns
		High-speed mode, C_B – 100pF max	10	80	ns
		High-speed mode, C_B – 400pF max	20	160	ns
t_{FDA}	Fall Time of SDA Signal	Standard mode	20 + 0.1 C_B	300	ns
		Fast mode	20 + 0.1 C_B	300	ns
		High-speed mode, C_B – 100pF max	10	80	ns
		High-speed mode, C_B – 400pF max	20	160	ns
t_{SU}, t_{STO}	Setup Time for STOP Condition	Standard mode	4		µs
		Fast mode	600		ns
		High-speed mode	160		ns
C_B	Capacitive Load for SDA and SCL			400	pF

I²C TIMING DIAGRAMS

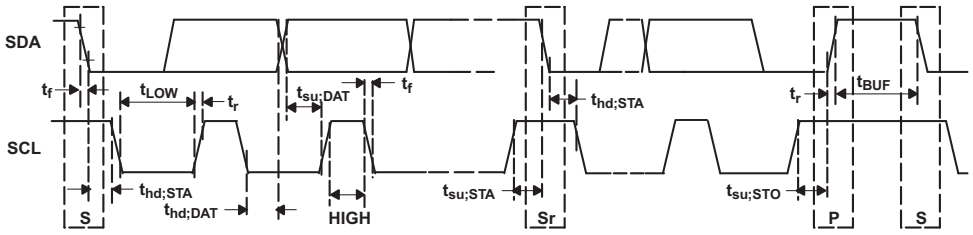
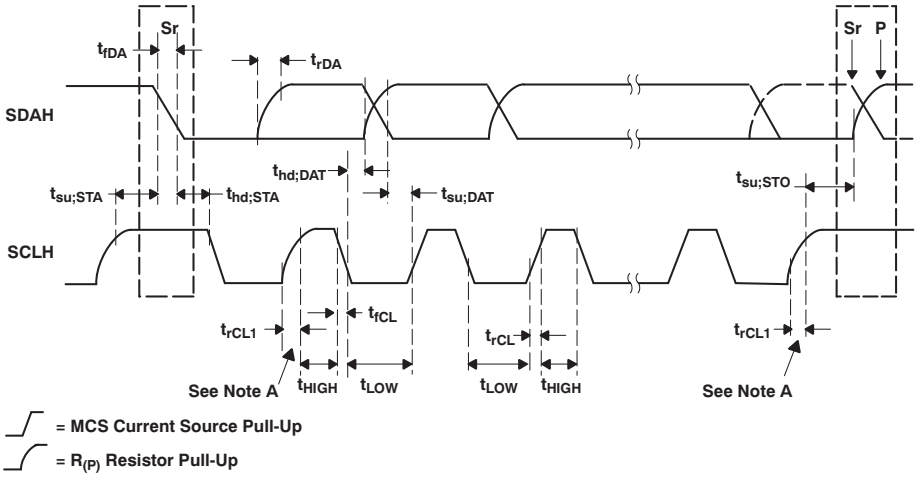


Figure 2. Serial Interface Timing for F/S-Mode



Note A: First rising edge of the SCLH signal after Sr and after each acknowledge bit.

Figure 3. Serial Interface Timing for H/S-Mode

Copyright © 2010, Texas Instruments Incorporated

查询"TPS61310"供应商

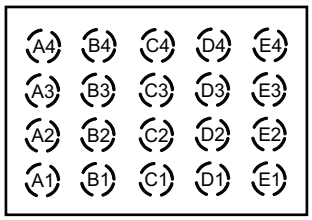
DEVICE INFORMATION

Table 2. PIN FUNCTIONS

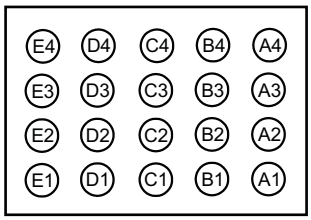
PIN		I/O	DESCRIPTION
NAME	NO.		
AVIN	E4	I	This is the input voltage pin of the device. Connect directly to the input bypass capacitor.
VOUT	A2	O	This is the output voltage pin of the converter.
LED1	E2	I	LED return input (current sinks). This feedback pin regulates the LED current through the internal sense resistor by regulating the voltage across it. Connect to the cathode of the white LEDs.
LED2	E1	I	
LED3	E3	I	
STRB0	B4	I	LED1/2/3 enable logic input. This pin can be used to enable/disable the high-power LEDs connected to the device. STRB0 = LOW: LED1, LED2 and LED3 current regulators are turned off. STRB0 = HIGH: LED2, LED2 and LED3 current regulators are active. The LED current level (video light or flash current) is defined according to the STRB1 logic level.
NRESET	B3	I	Master hardware reset input. NRESET = LOW: The device is forced in shutdown mode and the I^2C control I/F and all internal control registers are reset. NRESET = HIGH: The device is operating normally under the control of the I^2C interface.
SCL	B2	I	Serial interface clock line. This pin must not be left floating and must be terminated.
SDA	B1	I/O	Serial interface address/data line. This pin must not be left floating and must be terminated.
GPIO/PG	D4	I/O	This pin can either be configured as a general purpose input/output pin (GPIO) or either as an open-drain or a push-pull output to signal when the converters output voltage is within the regulation limits (PG). Per default, the pin is configured as an open-drain power-good output.
TS	C4	I	NTC resistor connection. This pin can be used to monitor the LED temperature. Connect a 220kΩ NTC resistor from the TS input to ground. In case this functionality is not desired, the TS input should be tied to AVIN or left floating.
INDLED	A1	O	This pin provides a constant current source to drive low V_F LEDs. Connect to LED anode.
STRB1	D3	I	LED current level selection input. Pulling this input high disables the video light watchdog timer. STRB1 = LOW: flash mode is enabled. STRB1 = HIGH: video light mode is enabled.
Tx-MASK	C3	I	RF PA synchronization control input. Pulling this pin high turns the LED from flash to video light operation, thereby reducing almost instantaneously the peak current loading from the battery.
SW	C1 C2	I/O	Inductor connection. Drain of the internal power MOSFET. Connect to the switched side of the inductor. SW is high impedance during shutdown.
PGND	D1 D2		Power ground. Connect to AGND underneath IC.
AGND	A3 A4		Analog ground.

PIN ASSIGNMENTS

CSP-20
(TOP VIEW)



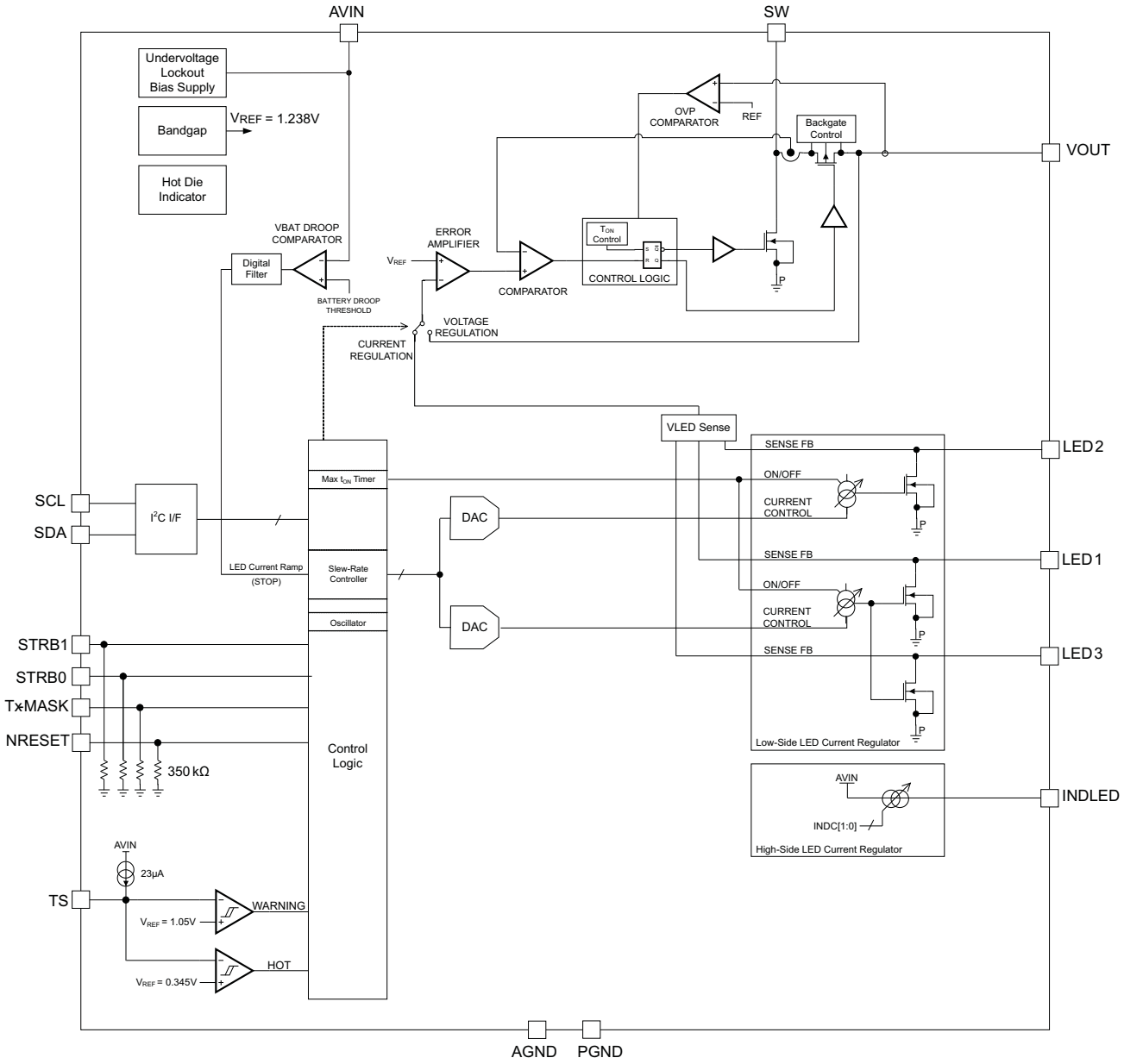
CSP-20
(BOTTOM VIEW)



Copyright © 2010, Texas Instruments Incorporated

查询"TPS61310"供应商

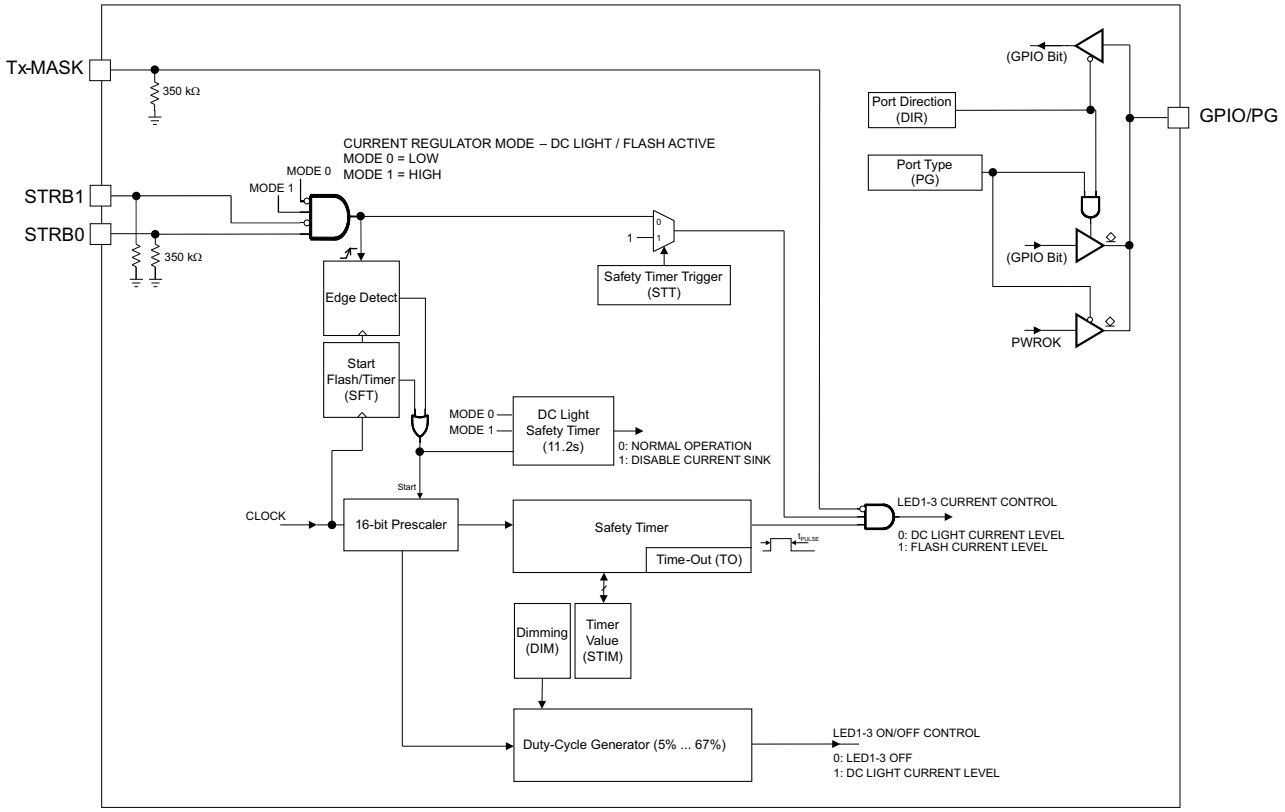
FUNCTIONAL BLOCK DIAGRAM



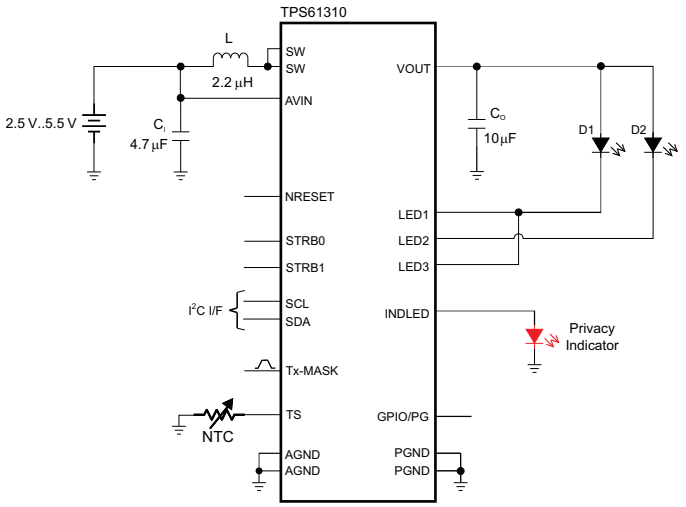
Copyright © 2010, Texas Instruments Incorporated

查询"TPS61310"供应商

TIMER BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION



List of Components:
L = 2.2µH, Wuerth Elektronik WE-TPC Series
C_I, C_O = 10µF 6.3V X5R 0603 – TDK C1605X5R0J106MT
Storage Capacitor = TDK EDLC262020-500mF
NTC = 220kΩ, muRata NCP18WM224J03RB

查询 TPS61310 供应商

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
LED Power Efficiency	vs. Input Voltage	Figure 4, Figure 5
DC Input Current	vs. Input Voltage	Figure 6
LED Current	vs. LED Pin Headroom Voltage	Figure 7, Figure 8
LED Current	vs. LED Current Digital Code	Figure 9, Figure 10, Figure 11, Figure 12
INDLED Current	vs. LED Pin Headroom Voltage	Figure 13
Voltage Mode Efficiency	vs. Output Current	Figure 14, Figure 15
DC Output Voltage	vs. Output Current	Figure 16, Figure 17
Maximum Output Current	vs. Input Voltage	Figure 18
DC Pre-Charge Current	vs. Differential Input-Output Voltage	Figure 19, Figure 20
Supply Current	vs. Input Voltage	Figure 21
Temperature Detection Threshold		Figure 22, Figure 23
Junction Temperature	vs. Port Voltage	Figure 24
Flash Sequence		Figure 25
Tx-Masking Operation		Figure 26, Figure 27, Figure 28
Low-Light Dimming Mode Operation		Figure 29
PWM Operation		Figure 30
PFM Operation		Figure 31
Down-Mode Operation (Voltage Mode)		Figure 32
Voltage Mode Load Transient Response		Figure 33
Start-up Into video Light Operation		Figure 34
Start-up Into Voltage Mode Operation		Figure 35

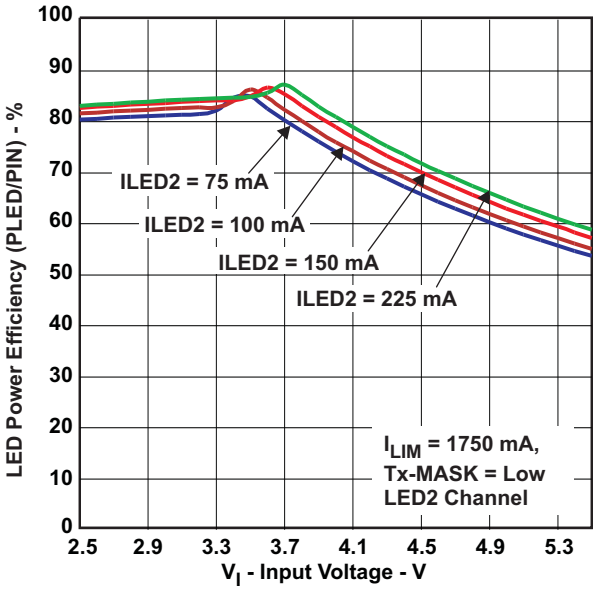


Figure 4. LED Power Efficiency vs. Input Voltage

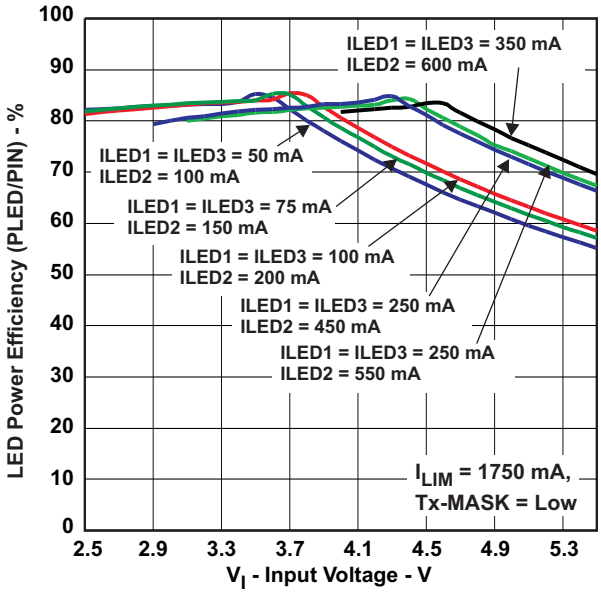


Figure 5. LED Power Efficiency vs. Input Voltage

Copyright © 2010, Texas Instruments Incorporated

查询"TPS61310"供应商

TYPICAL CHARACTERISTICS (continued)

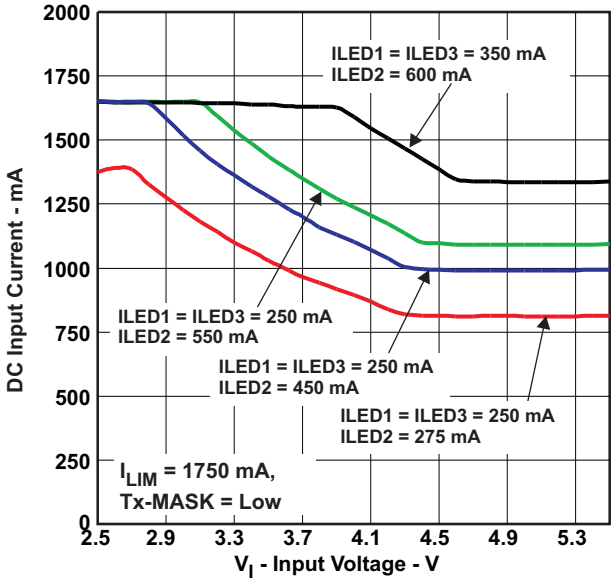


Figure 6. DC Input Current vs. Input Voltage

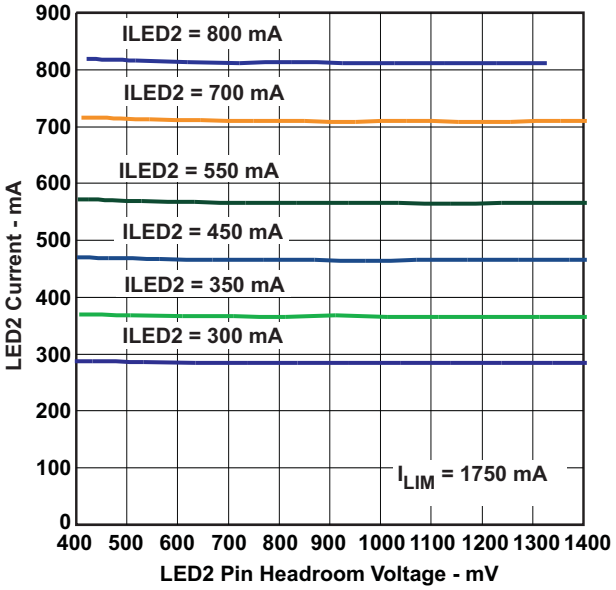


Figure 7. LED2 Current vs. LED2 Pin Headroom Voltage

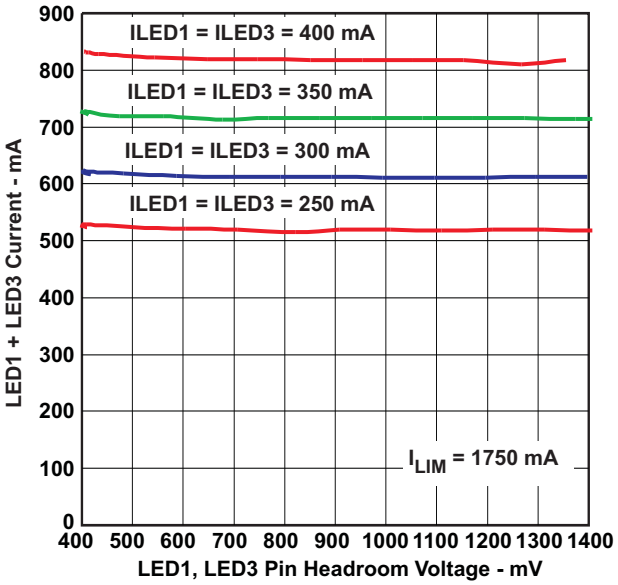


Figure 8. LED1+LED3 Current vs. LED1+LED3 Pin Headroom Voltage

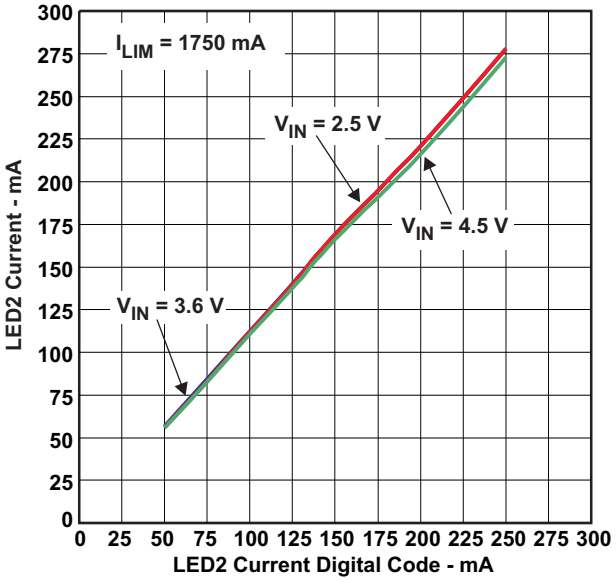


Figure 9. LED2 Current vs. LED2 Current Digital Code

查询"TPS61310"供应商

TYPICAL CHARACTERISTICS (continued)

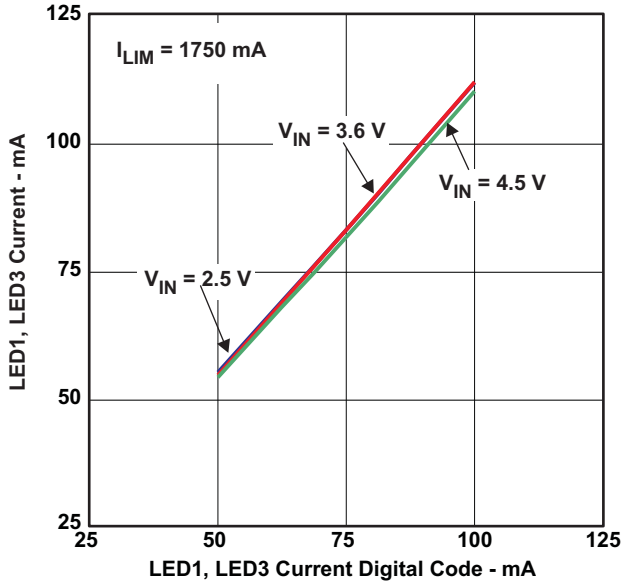


Figure 10. LED1, LED3 Current vs. LED1, LED3 Current Digital Code

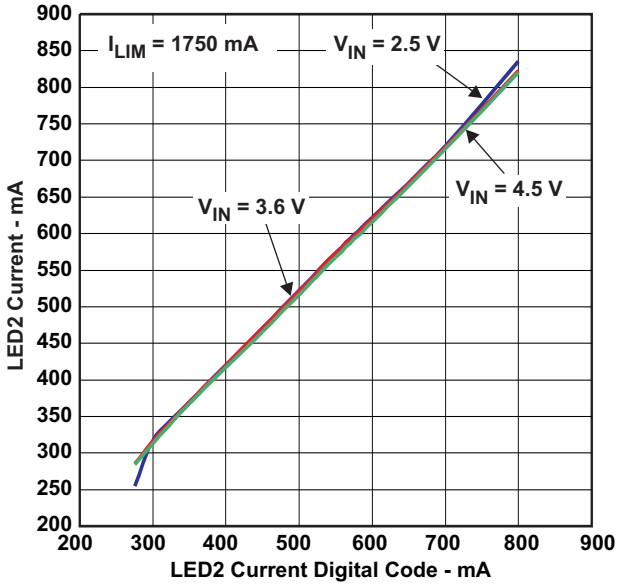


Figure 11. LED2 Current vs. LED2 Current Digital Code

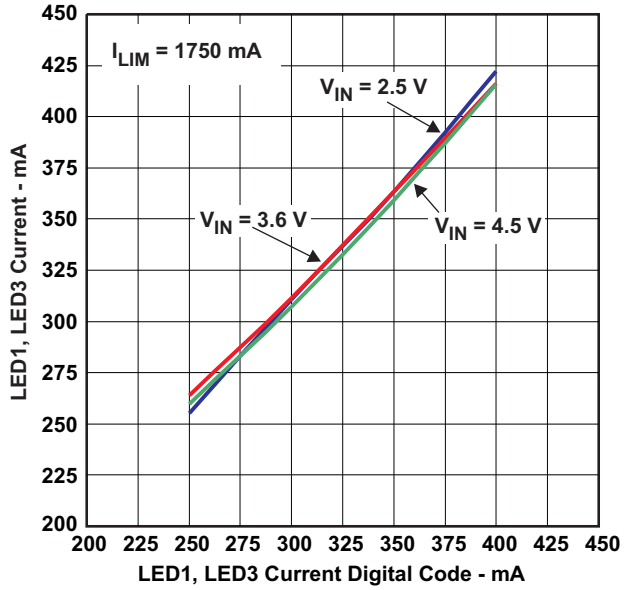


Figure 12. LED1, LED3 Current vs. LED1, LED3 Current Digital Code

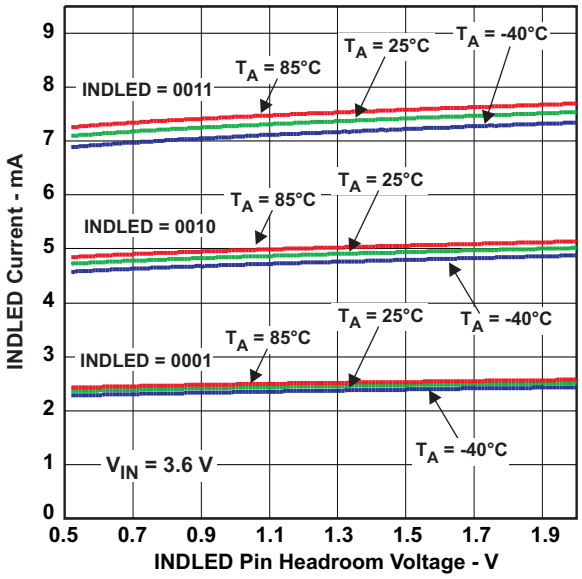


Figure 13. INDLED Current vs. INDLED Pin Headroom Voltage

Copyright © 2010, Texas Instruments Incorporated

查询"TPS61310"供应商

TYPICAL CHARACTERISTICS (continued)

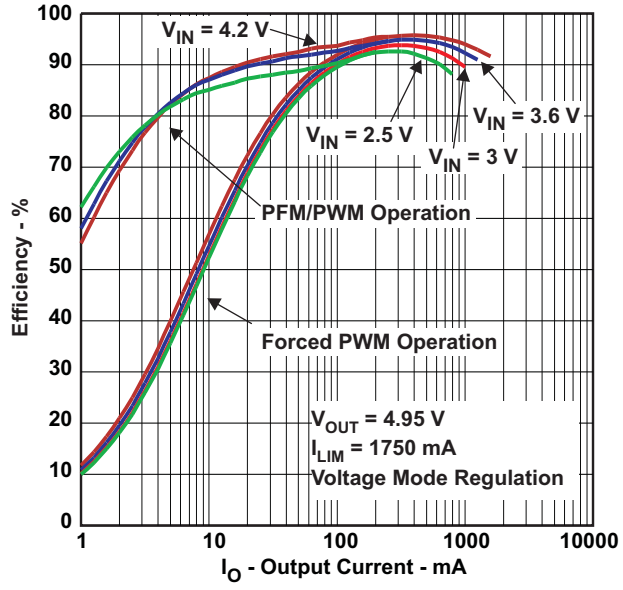


Figure 14. Efficiency vs. Output Current

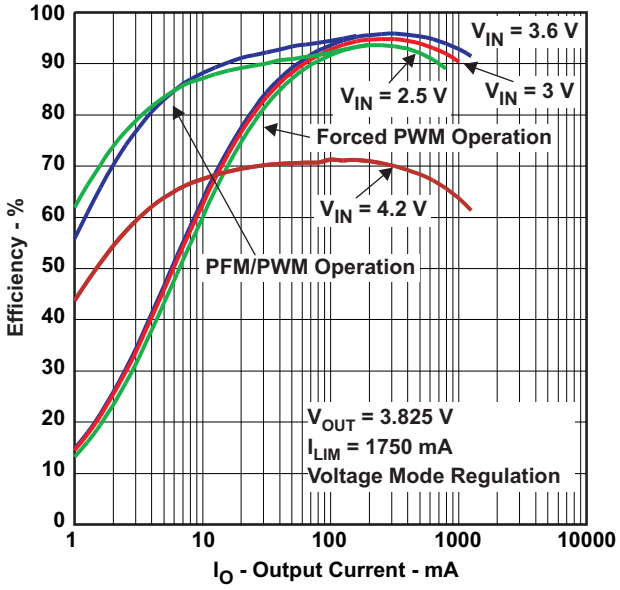


Figure 15. Efficiency vs. Output Current

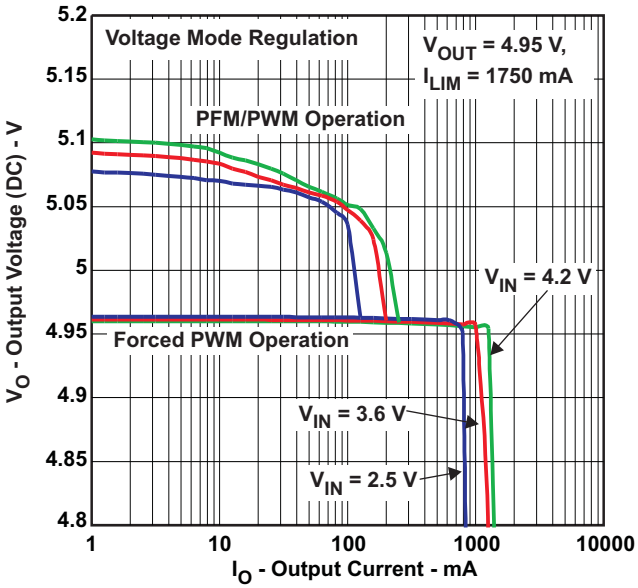


Figure 16. DC Output Voltage vs. Load Current

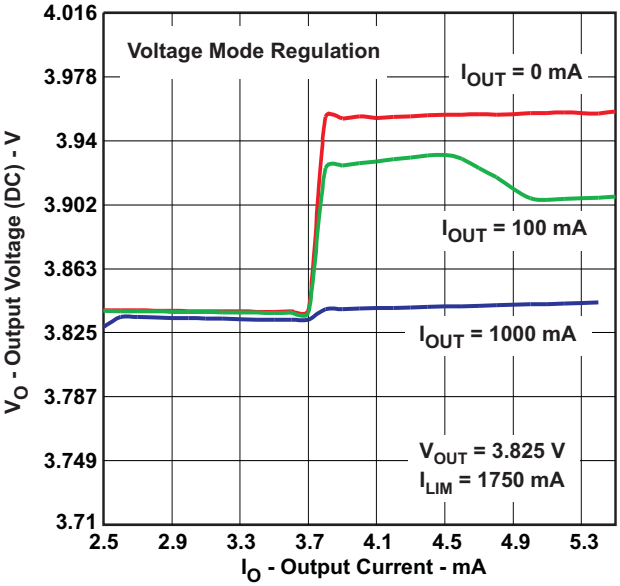


Figure 17. DC Output Voltage vs. Load Current

查询"TPS61310"供应商

TYPICAL CHARACTERISTICS (continued)

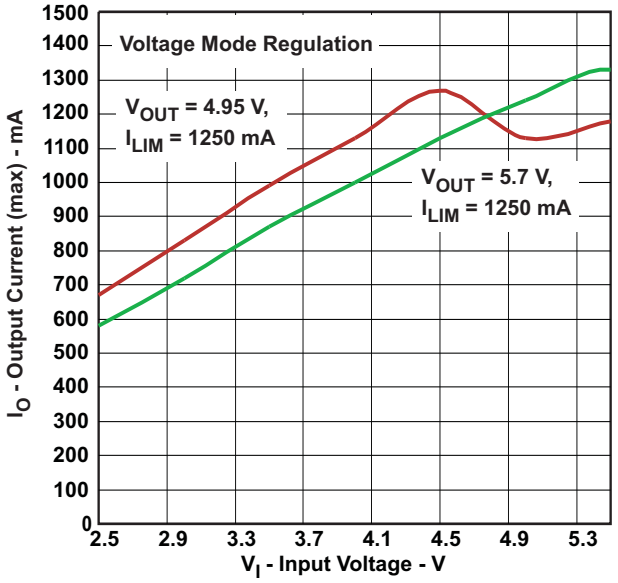


Figure 18. Maximum Output Current vs. Input Voltage

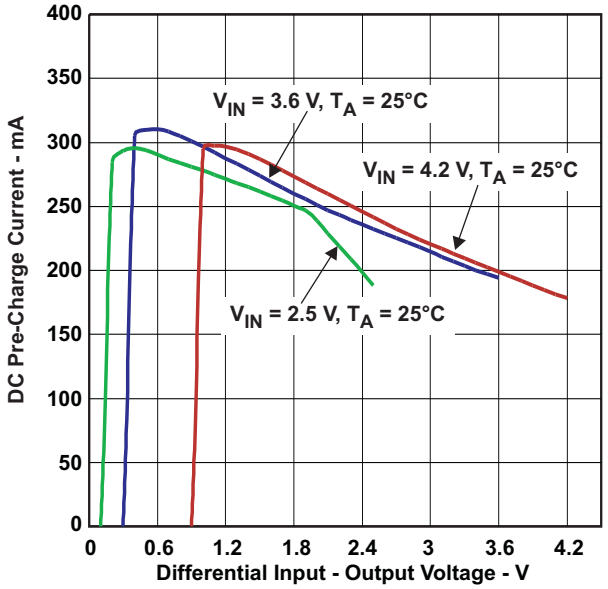


Figure 19. DC Pre-Charge Current vs. Differential Input-Output Voltage

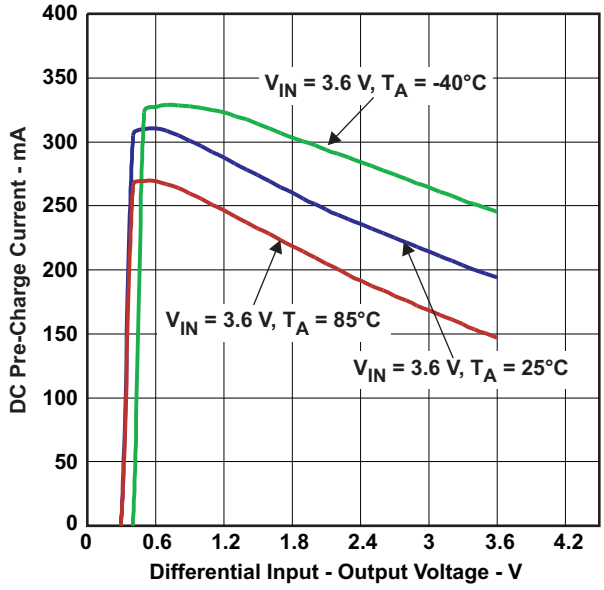


Figure 20. DC Pre-Charge Current vs. Differential Input-Output Voltage

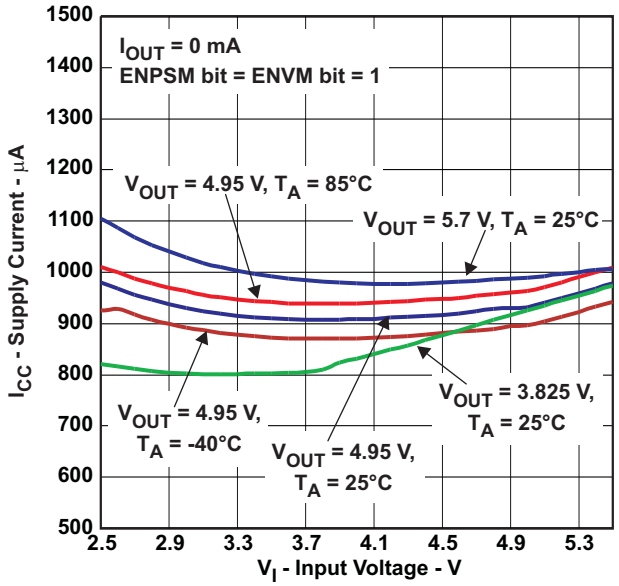


Figure 21. Supply Current vs. Input Voltage

Copyright © 2010, Texas Instruments Incorporated

查询"TPS61310"供应商

TYPICAL CHARACTERISTICS (continued)

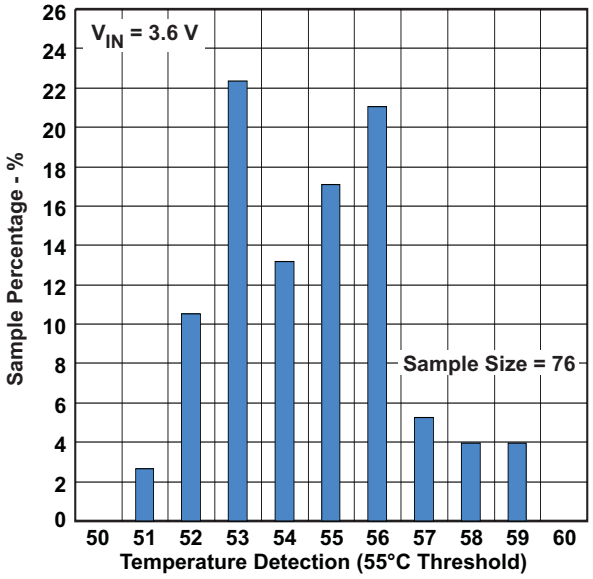


Figure 22. Temperature Detection Threshold

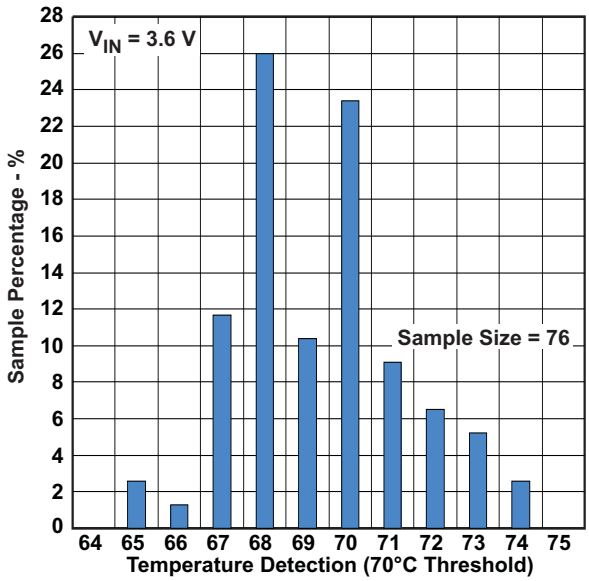


Figure 23. Temperature Detection Threshold

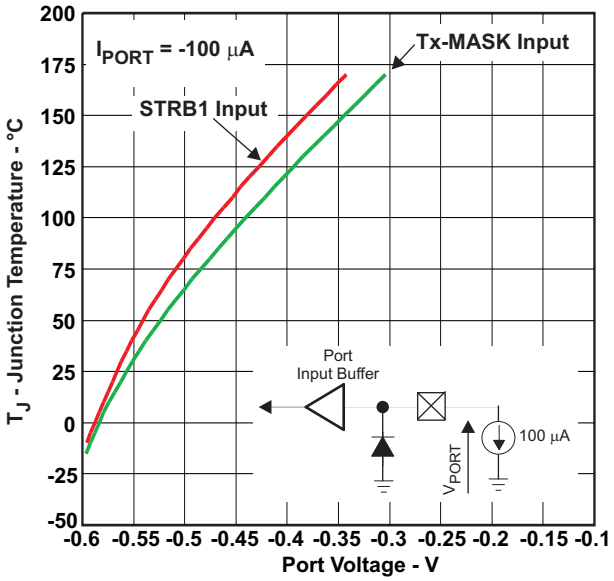


Figure 24. Junction Temperature
vs.
Port Voltage

查询"TPS61310"供应商

TYPICAL CHARACTERISTICS (continued)

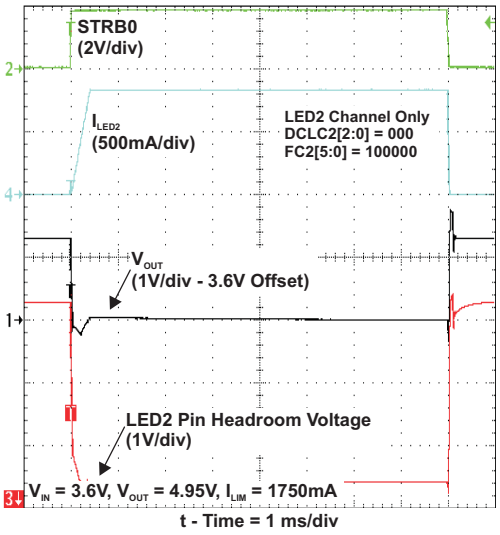


Figure 25. FLASH SEQUENCE (STRB1=0)

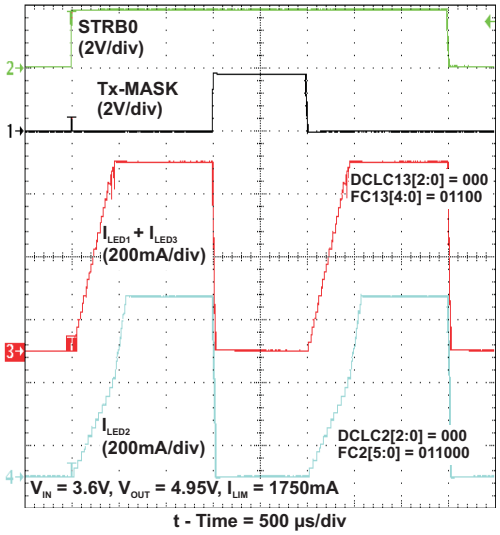


Figure 26. Tx-MASKING OPERATION (STRB1=0)

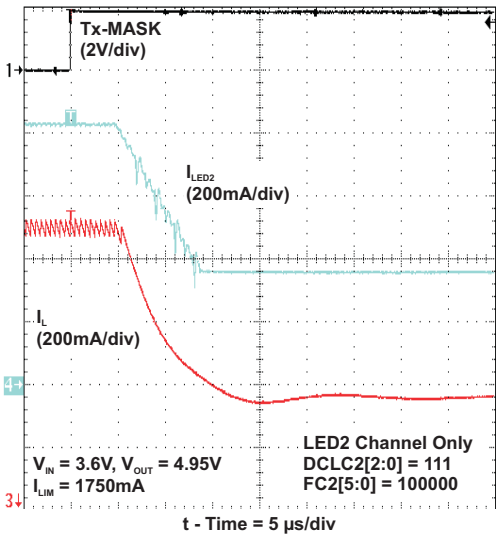


Figure 27. Tx-MASKING OPERATION (STRB1=0)

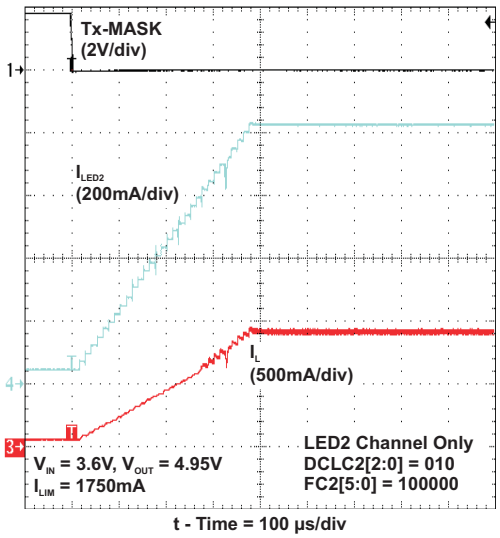


Figure 28. Tx-MASKING OPERATION (STRB1=0)

Copyright © 2010, Texas Instruments Incorporated

查询"TPS61310"供应商

TYPICAL CHARACTERISTICS (continued)

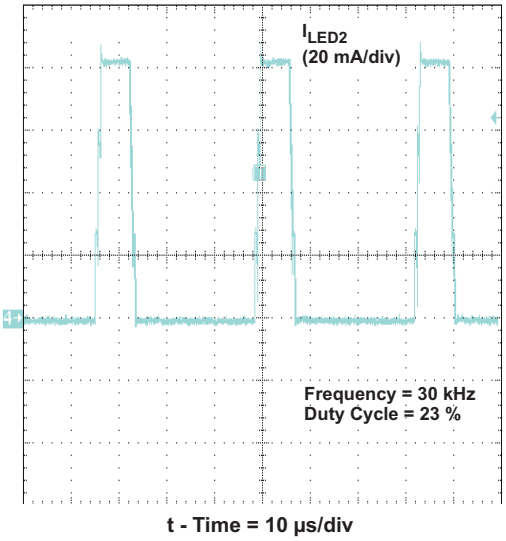


Figure 29. LOW-LIGHT DIMMING MODE OPERATION

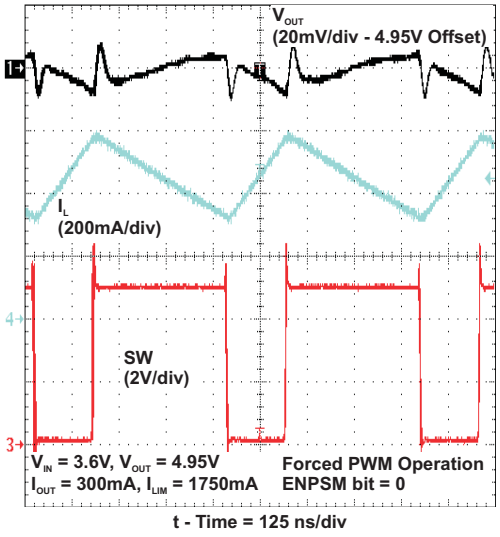


Figure 30. PWM OPERATION

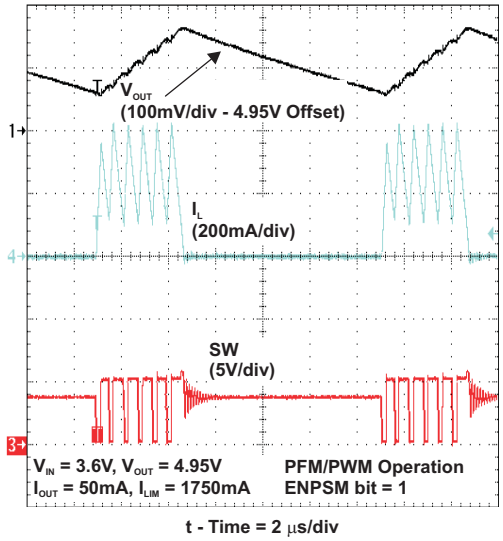


Figure 31. PFM OPERATION

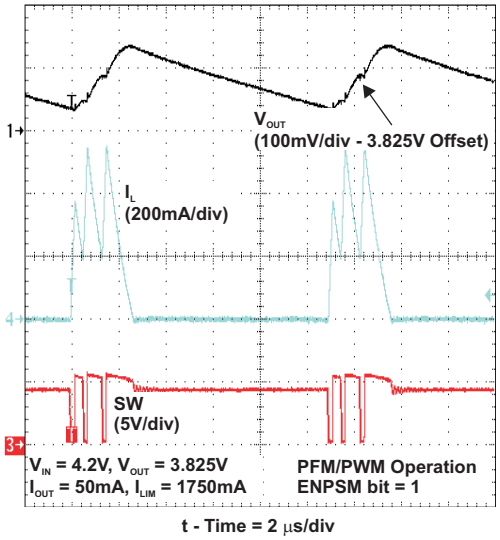


Figure 32. DOWN-MODE OPERATION (VOLTAGE MODE)

查询"TPS61310"供应商

TYPICAL CHARACTERISTICS (continued)

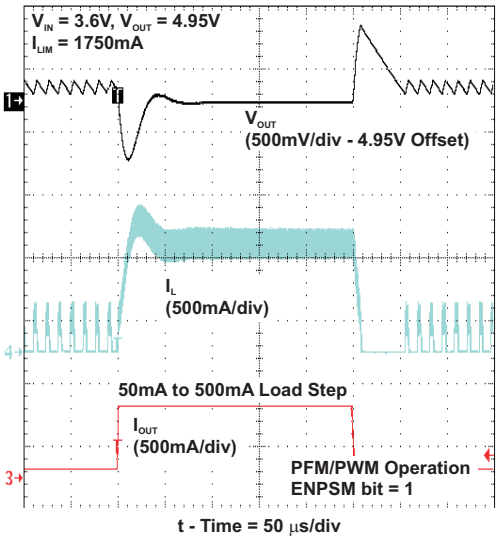


Figure 33. VOLTAGE MODE LOAD TRANSIENT RESPONSE

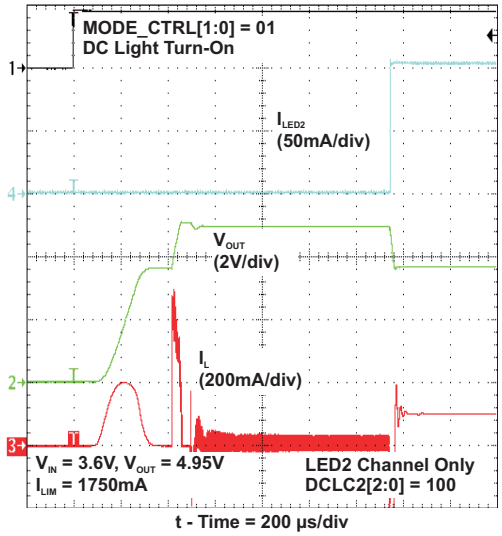


Figure 34. START-UP INTO video LIGHT OPERATION

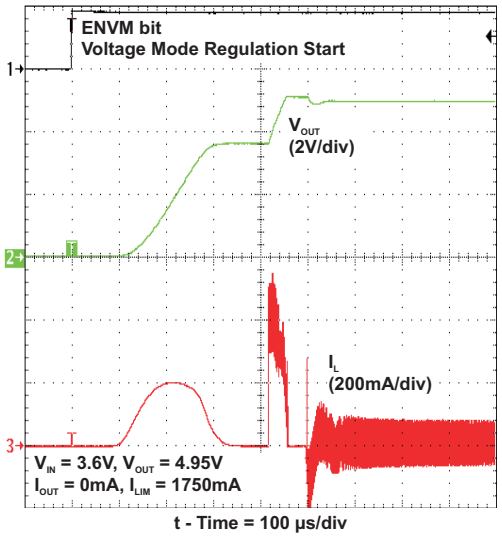


Figure 35. START-UP INTO VOLTAGE MODE OPERATION

Copyright © 2010, Texas Instruments Incorporated

查询"TPS61310"供应商

DETAILED DESCRIPTION

OPERATION

The TPS6131x family is an integrated solution with a wide feature set for driving up to three LEDs for still-camera flash and video-camera lighting applications. It employs a 2MHz fixed on-time, PWM current-mode converter to generate the output voltage required to drive up to three high-power LEDs in parallel. The device integrates an NMOS-switch power stage and a synchronous PMOS rectifier. The device also implements a set of linear low-side current regulators to control the LED current when the battery voltage is higher than the diode forward voltage.

The high efficient boost converter stage and LED forward voltage adoption ensure lowest device input current for a given LED output current.

A special circuit disconnects the load from the battery during shutdown of the converter. In conventional synchronous-rectifier circuits, the back-gate diode of the high-side PMOS is forward biased in shutdown, allowing current to flow from the battery to the output. The TPS6131x prevents this by disconnecting the cathode of the back-gate diode of the high-side PMOS from the source when the regulator is in shutdown.

The TPS6131x device not only operates as a regulated current source, but also as a standard voltage-boost regulator featuring a power-save mode for improved efficiency at light loads. If the input voltage is higher than the programmed output voltage, a down mode is implemented that acts similarly to an LDO.

The power stage is capable of supplying a maximum total current of roughly 1500mA. The TPS6131x provides three constant-current sinks, capable of sinking up to 2x 400mA (LED1 and LED3) and 800mA (LED2) in flash mode.

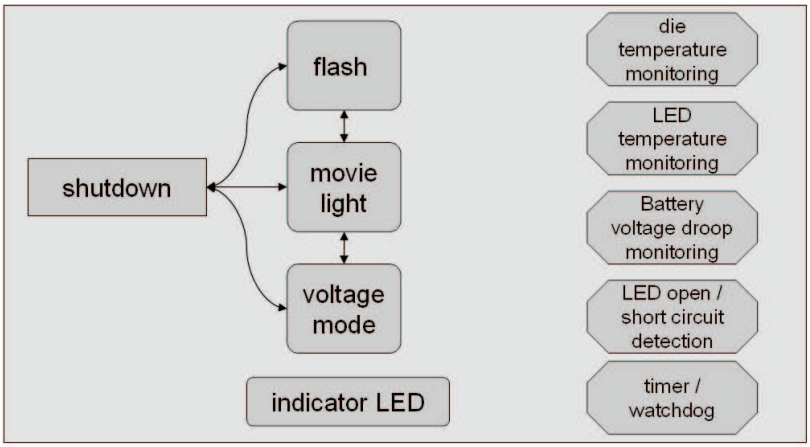


Figure 36. TPS6131x States

Special effort is taken for safe operation and robust system integration. The battery voltage can be monitored so that the flash current is not increased if the battery voltage drops by a programmable threshold. Internal timers limit the flash on-time to prevent potential camera-engine software errors, and a video light watchdog acts in a similar fashion. Multiple monitoring features (LED and die temperature, input voltage droop etc.) keep the device and LEDs operating properly.

Copyright © 2010, Texas Instruments Incorporated

The TPS6131x integrates an I²C compatible interface allowing transfers up to 3.4Mbits/s for controlling the device, featuring low-speed mode, standard mode and high-speed mode compatible operation. Additionally, basic functions can be triggered by dedicated hardware input signals, such as STRB0 and STRB1 for triggering the flash or video lighting with zero latency.

VIDEO LIGHT AND FLASH STROBE OPERATION

The TPS6131x devices drive one, two or three LEDs for video light and flash application. The video light and flash operation can either be triggered by an I²C software command or by means of dedicated, zero latency hardware signals.

LED Hardware Setup

The TPS6131x device utilizes LED forward-voltage sensing circuitry on LED1-3 pins to optimize the power-stage boost ratio for maximum efficiency. Due to the nature of the sensing circuitry, it is not recommended to leave any of the LED1-3 pins unused if the operation has been selected via ENLED[3:1] bits. Leaving LED1-3 pins unconnected, while the respective ENLEDx bits have been set, forces the control loop into high gain, and eventually trips the output overvoltage protection. Figure 37 shows the recommend LED setup for a single, dual or triple-LED application.

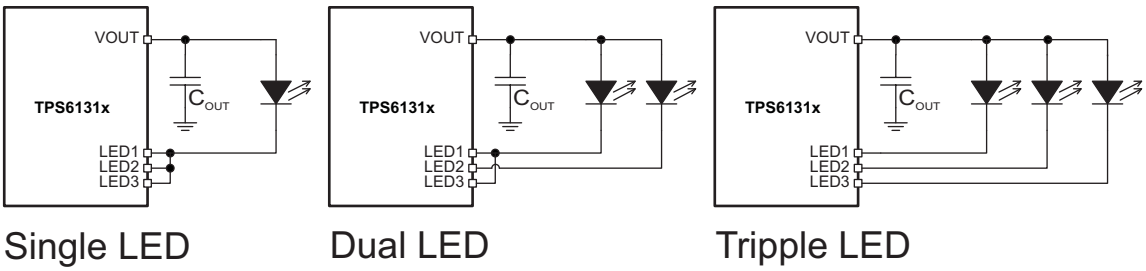


Figure 37. White LED Hardware Setup Options

The LED1-3 inputs may be connected together to drive one or two LEDs at higher currents. Connecting the current sink inputs in parallel does not affect the internal operation of the TPS6131x. For best operation, it is recommended to disable the LED inputs that are not connected. (see the ENLED[3:1] bits description in REGISTER5 DESCRIPTION).

The video light currents are individually programmed via the video light control bits DCL13[2:0] and DCL2[2:0] , the flash currents via FC2[5:0] and FC13[4:0] bits accordingly. If, for single or dual LED application as shown in Figure 37, current sinks are connected to each other and enabled, the resulting video / flash current will be the sum of the programmed currents.

Triggering Video Light and Flash

For most flexible system integration, the TPS6131x offers several options for activating the video light and flash. Depending on the settings of the MODE_CTRL[1:0] bits, the device can enter different modes of operation. It offers the option of triggering the video light and flash via hardware signals (STRB0, STRB1) or software I²C command. The flash-signal hardware trigger can be on the leading-edge, turning on for the programmed flash on time, or level sensitive, turning on for as long as the signal is logic high.

The TPS6131x flash timer is programmed via the STIM[2:0] and SELSTIM bits. If the flash is fired by a rising-edge trigger or by an I²C command, the timer defines the flash duration. If the flash is fired by a level-sensitive trigger, the timer defines the maximum flash-on duration, and overrides the hardware signal if the programmed on-time is exceeded.

For video lighting, a watchdog timer is implemented; this must be refreshed within 13.0 seconds. This function can be disabled, as described below.

Copyright © 2010, Texas Instruments Incorporated

查询"TPS61310"供应商

MODE_CTRL[1:0] = 01:	The STRB0, STRB1 inputs are disabled. The device regulates the LED current in video light mode (DCLC bits) regardless of the STRB0, STRB1 inputs and the START_FLASH/TIMER (SFT) bit. To avoid device shutdown because of the video light safety timeout, MODE_CTRL[1:0] must be refreshed within less than 13.0 seconds (STRB1 = 0). The video light watchdog timer can be disabled by pulling the STRB1 signal high.
MODE_CTRL[1:0] = 10:	The STRB0, STRB1 inputs are enabled. The flash pulse can be triggered by these synchronization signals, or by a software command (START_FLASH/TIMER (SFT) bit). The LEDs are enabled/disabled according to the STRB0, STRB1 input. The flash safety timer is activated, and the video light watchdog timer is disabled.

The dual-wire camera-module interface STRB0 and STRB1 inputs are used for selecting the video light (STRB1 = 1) or flash (STRB1 = 0) mode. The STRB0 signal then triggers the video light or flash, depending on the state of STRB1. The STT bit defines if the flash trigger is level sensitive (STT = 0), or fired on the rising edge (STT = 1).

Level-Sensitive Flash Trigger (STT = 0)

In this mode, the high-power LEDs are driven at the flash-current level and the safety timer (STIM) is running. The maximum duration of the flash pulse is defined in the STIM[2:0] register.

The safety timer is triggered on rising edge and stopped by a negative logic on the synchronization source (STRB0, STRB1 = 0) or by a timeout event (TO bit).

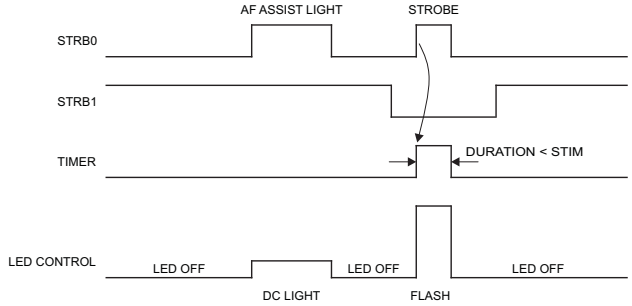


Figure 38. Hardware Synchronized Video Light and flash Strobe

Rising-Edge Flash Trigger (STT = 1)

In this mode, the high-power LEDs are driven at the flash current level and the safety timer (STIM) is running. The duration of the flash pulse is defined in the STIM[2:0] register.

The flash strobe is started either by a rising edge on the synchronization source (STRB0, STRB1 = 0) or by a positive transition on the START-FLASH/TIMER (SFT) bit. Once running, the timer ignores all kind of triggering signals and only stops after a timeout (TO). START-FLASH/TIMER (SFT) bit is being reset by the timeout (TO) signal.

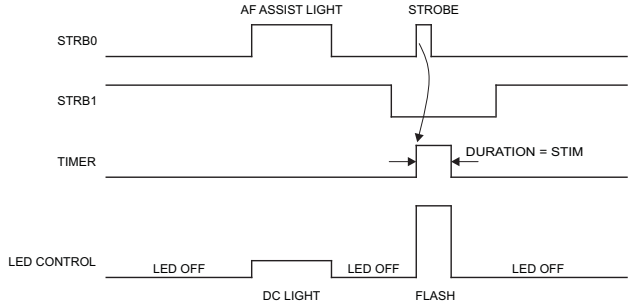


Figure 39. Edge Sensitive Timer (Single Trigger Event)

查询 TPS61310 供应商

VOLTAGE MODE

In this mode, the TPS6131x operates as a standard voltage-boost regulator, featuring power-save mode for improved efficiency under light loads. The voltage-mode operation is enabled by software control by setting the mode-control bit MODE_CTRL[1:0] = 11. The device regulates a constant output voltage according to the OV[3:0] bit settings (between 3.825V and 5.7V in 125mV steps). In voltage mode, the LED current sinks LED1-3 are turned off.

The TPS6131x integrates a software control bit (ENVM bit) that can be used to force the converter to run in voltage mode. This enables the converter to operate at a fixed programmed output voltage (according to the OV[3:0] settings) while operating the LEDs.

Table 3 provides an overview of the different voltage mode variations.

Table 3. Voltage Mode Description

INTERNAL REGISTER SETTINGS MODE_CTRL[1:0]	ENVM BIT	OPERATING MODES
11	0	LEDs are turned off and the converter operate in voltage-regulation mode (VM); the output voltage is set via register OV[3:0].
00	1	
01	1	The converter operates in voltage-regulation mode (VM); the output voltage is set via the register OV[3:0]. The LEDs are turned-on for video light operation and the energy is being directly transferred from the battery to the output. The LED currents are regulated by the means of the low-side current sinks.
10	1	The converter operates in the voltage-regulation mode (VM); the output voltage is set via the register OV[3:0]. The LED currents are regulated by the low-side current sinks. The LEDs are ready for flash operation.
11	1	LEDs are turned off and the converter operates in the voltage regulation mode (VM); the output voltage is set via the register OV[3:0].

Down mode in voltage mode operation

In general, a boost converter only regulates output voltages which are higher than the input voltage. The TPS6131x can regulate 4.2V at the output with an input voltage as high as 5.5V. To control these applications properly, a down-conversion mode is implemented.

In voltage-regulation mode, if the input voltage reaches or exceeds the output voltage, the converter changes to down-conversion mode. In this mode, the control circuit changes the behavior of the rectifying PMOS. It sets the voltage drop across the PMOS as high as needed to regulate the output voltage. This increases the power losses in the converter, and must be taken into account for thermal design. The down-conversion mode is automatically turned off as soon as the input voltage falls to approximately 200mV below the output voltage.

For proper operation in down-conversion mode the output voltage should not be programmed higher than approximately 5.3V. Care should be taken not to violate the absolute maximum ratings at the SW pins.

Power Good Indication

The TPS6131x integrates a power-good circuit that is activated when the device operates in voltage-regulation mode (MODE_CTRL[1:0] = 11 or ENVM = 1). In shutdown mode (MODE_CTRL[1:0] = 00, ENVM = 0), the GPIO/PG pin state is defined below, according to the GPIOTYPE bit:

GPIOTYPE	GPIO/PG SHUTDOWN STATE
0	Reset/pulled to ground
1	Open-drain

Depending on the GPIO/PG output stage type selection (i.e., push-pull or open-drain), the polarity of the power-good output signal (PG) can be inverted or not. The power-good software bit and hardware signal polarity is defined below:

GPIOTYPE	PG BIT	GPIO/PG OUTPUT PORT	COMMENTS
0: push-pull output	0	0	Output is active-high
	1	1	

Copyright © 2010, Texas Instruments Incorporated

查询"TPS61310"供应商

GPIOTYPE	PG BIT	GPIO/PG OUTPUT PORT	COMMENTS
1: open-drain output	0	Open-drain	Output is active-low
	1	Low	

The power-good signal is true when the output voltage is within –1.5% and +2.5% of its nominal value. Conversely, it is false when the voltage-mode operation is suspended (MODE_CTRL[1:0] ≠ 11 and ENVM = 0).

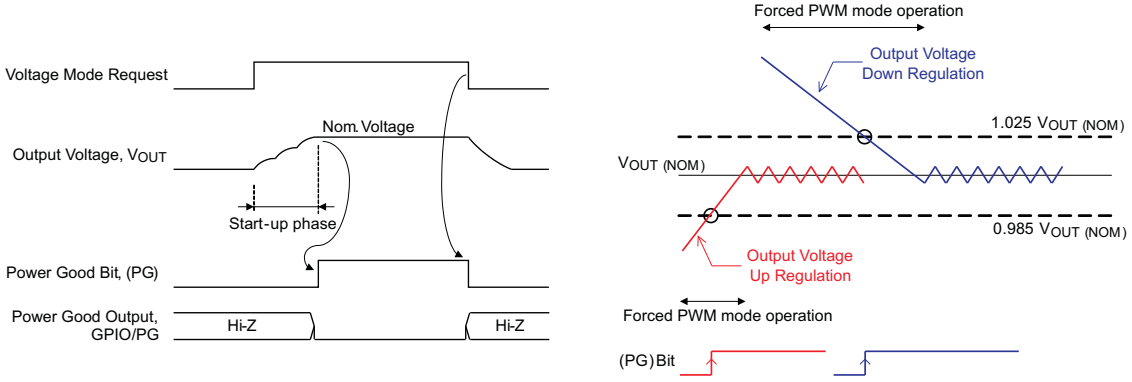


Figure 40. Power Good Operation (DIR = 1, GPIOTYPE = 1)

The TPS6131x device uses a control architecture that “recycles” excess energy that might be stored in the output capacitor. By reversing the operation of the boost power stage, the converter is capable of transferring energy from its output back into the input source. In this case, the power-good signal is de-asserted while the output voltage is decreasing towards its target value (i.e., the closest fit voltage the converter can support.

PRIVACY INDICATOR

The privacy indicator functionality can be used to indicate when a person is being photographed or filmed. The TPS6131x device offers two options of privacy indication: A dedicated pin driving an additional privacy indicator LED or using the white LEDs with pulse width modulation.

Dedicated LED Privacy Indicator

The TPS6131x device provides a high-side linear constant current source to drive low V_F LEDs. The LED current is directly regulated off the battery and can be controlled via the INDC[3:0] bits, ranging 2.6mA to 15.8mA in 7 programable current steps.

The device can drive two possible hardware configurations shown in Figure 41 and Figure 42. In Figure 41 the TPS6131x device drives a privacy indicator LED towards ground.

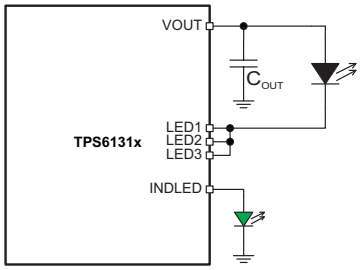


Figure 41. Configuration 1

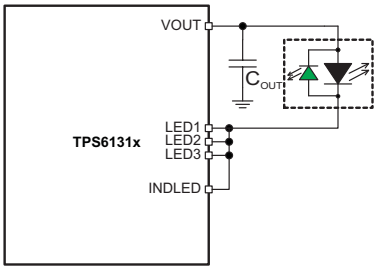


Figure 42. Configuration 2

The TPS6131x device also allows a path for driving a privacy indicator LED that is reverse biased to the white flash LED, see Figure 42. To do so, the output of the converter (VOUT) is pulled to ground thus allowing a reverse current to flow. This mode of operation is only possible when the converter’s power stage is in shutdown (MODE_CTRL[1:0] = 00, ENVM = 0).

Copyright © 2010, Texas Instruments Incorporated

查询 TPS61310 供应商

White LED Privacy Indicator

The TPS6131x device features white LED drive capability at very low light intensity. To generate a reduced LED average current, the device employs a 30kHz fixed-frequency PWM modulation scheme. The PWM timer uses the internal oscillator as reference clock, therefore the PWM modulating frequency shows the same accuracy as the internal reference clock. Operation is shown in the Timer Block Diagram.

The video light current is modulated with a duty cycle defined by the INDC[3:0] bits. The low light dimming mode can only be activated in the software-,controlled video-light-only mode (MODE_CTRL[1:0] = 01, ENVM = 1), and applies to the LEDs selected via ENLED[3:1] bits. In this mode, the video light safety-timeout feature is disabled.

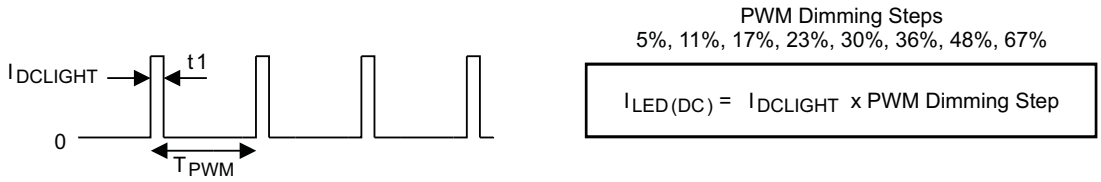


Figure 43. PWM Dimming Principle

SAFE OPERATION AND PROTECTION FEATURES

LED Temperature Monitoring (Finger-Burn Protection)

The TPS6131x device optionally monitors the LED temperature. Critical temperatures are handled in two stages reflected by two bits: LEDWARN provides an early warning to the camera engine, LEDHOT immediately suspends the flash operation.

The LED temperature is sensed by measuring the voltage drop of a negative-temperature-coefficient resistor connected between the TS and AGND pins. An internal current source provides the bias (c.a. 24 μA) for the NTC, and the TS pin voltage is compared to internal thresholds (1.05V and 0.345V) to protect the LEDs against overheating. See the Application Information section for choosing the NTC.

The temperature-monitoring blocks are explicitly active in video light or flash modes. In voltage-mode operation [MODE_CTRL[1:0] = 11], the device only activates the TS input when the ENTS bit is set high.

The LEDWARN and LEDHOT bits reflect the LED temperature. The LEDWARN bit is set when the voltage at the TS pin is lower than 1.05V. This threshold corresponds to an LED warning temperature value; device operation is still permitted. While regulating LED current (i.e. video light or flash modes), the LEDHOT bit is latched when the voltage at the TS pin is lower than 0.345V. This threshold corresponds to an excessive LED temperature value; device operation is immediately suspended, (MODE_CTRL[1:0] bits are reset, and the HOTDIE[1:0] bits are set).

LED Failure Modes (Open / Short Detection) and Overvoltage Protection

The TPS6131x devices incorporate protection features to indicate if the connected LED(s) are failing. These protections cover overvoltage conditions, which are caused by a failing LED showing open circuit behavior, as well as short circuit conditions caused by a failing LED or further reasons causing a short circuit condition. If such failure conditions occur, these are indicated by setting a failure detection flag. Furthermore, the maximum current drawn from the output is limited and can be programmed by the current-limit setting.

LED open circuit detection / Over Voltage Protection

If the connected LED(s) fail showing an open circuit behavior or are disconnected, the VOUT output voltage must be limited to prevent the step-up converter from exceeding critical values. An overvoltage protection is implemented to avoid the output voltage exceeding critical values for the device and possibly for the system it is supplying. For this protection the TPS6131x output voltage is monitored internally. The TPS6131x device limits V_{OUT} according to the overvoltage protection settings (refer to OVP specification). In this failure mode, V_{OUT} is either limited to 4.65V (typ.) or 6.0V (typ.) and the HIGH-POWER LED FAILURE [HPLF] flag is set. The OVP threshold depends on the programmed output voltage [OV].

Copyright © 2010, Texas Instruments Incorporated

查询"TPS61310"供应商

OVP THRESHOLD	OPERATING CONDITIONS
4.65 V typ.	0000 ≤ OV[3:0] ≤ 0100
6.0 V typ.	0101 ≤ OV[3:0] ≤ 1111

Short Circuit Protection

The TPS6131x devices incorporate double protection to protect the device and application circuit from short circuit conditions occurring between VOUT and the current sinks LED1..3.

If a short circuit condition occurs while the LED(s) are operated, the low side current sinks LED1, LED2, LED3 limit the maximum output current as programmed for the video-light mode or flash mode respectively. If a short circuit condition occurs, the current sinks increase their input resistance to prevent excessive current to be drawn. Furthermore, the HIGH-POWER LED FAILURE flag (HPLF) is set to indicate the short circuit condition. (HPLF) is triggered if the LED forward voltage drops below 1.23V typically. The second protection is the current limit, which generally limits the current drawn from VOUT. See the Current Limit section.

LED Current Ramp-Up/Down

To achieve smooth LED current waveforms and avoid excessive battery voltage drop, the TPS6131x device actively controls the LED current ramp-up / down sequence.

Table 4. LED Current Ramp-Up/Down Control vs Operating Mode

LED CURRENT RAMP-UP	I_{STEP} = 25mA
	t_{RISE} = 12µs
	Slew-rate × 2.1mA/µs
LED CURRENT RAMP-DOWN	I_{STEP} = 25mA
	t_{FALL} = 0.5µs
	Slew-rate × 50mA/µs

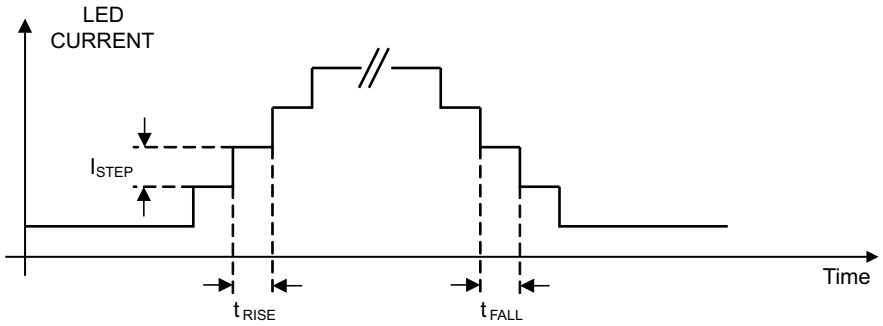


Figure 44. LED Current Slew-Rate Control

Battery Voltage Droop Monitoring and Protection

During a high-power flash strobe, the battery voltage usually drops by a few hundred millivolts. To prevent the battery voltage from collapsing too much, the TPS6131x devices integrates a battery voltage droop monitoring feature to automatically limit the flash current if the battery voltage drops more than a programmable threshold.

The battery voltage droop monitoring feature can be enabled/disabled via the ENBATMON bit.

At the very beginning of the flash strobe, the device measures the battery voltage and sets a minimum battery voltage threshold based on the tolerable droop (refer to BATDROOP[2:0] bits). While the LED current is increasing to the target flash current (see FC13[4:0] and FC2[5:0] bits), a comparator monitors the actual battery voltage and stops the ramp-up sequence when the droop exceeds the limit. Operation is understood best by referring to the functional block diagram and to Figure 45.

The battery voltage droop monitor feature is automatically disabled during a Tx-MASK event.

Copyright © 2010, Texas Instruments Incorporated

查询 TPS61310 供应商

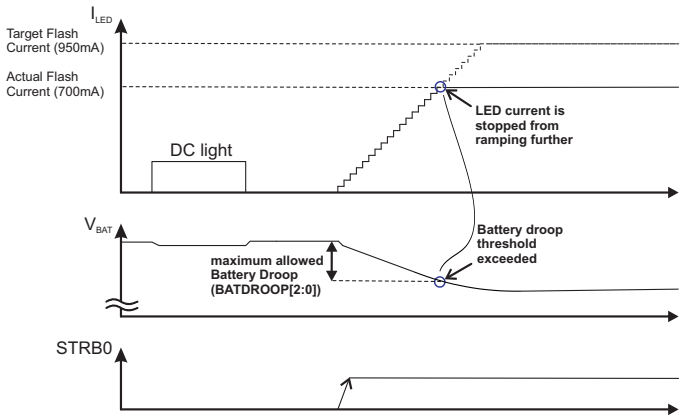


Figure 45. Battery Voltage Droop Monitoring / LED Current Control Principle (STRB1 = 0, Tx-BASE = 1)

Undervoltage Lockout

The undervoltage lockout circuit prevents the device from error conditions at low input voltages. It prevents the converter from turning on the switch–MOSFET, or rectifier–MOSFET for battery voltages below 2.3V. The I^2C compatible interface is fully functional down to 2.1V input voltage.

Hot Die Detection and Thermal Shutdown

The TPS6131x device offers two levels of die temperature monitoring and protection, which are hot die detection and thermal shutdown functionality. The hot die detector (HOTDIE[1:0] bits) reflects the instantaneous junction temperature. This functionality is always enabled except when the device is in shutdown mode.

The hot die detector monitors the junction temperature but does not shut down the device. It provides an early warning to the camera engine to avoid excessive power dissipation thus preventing from thermal shutdown during the next high-power flash strobe.

As soon as the junction temperature T_J exceeds 160°C typical, the device goes into thermal shutdown. In this mode, the power stage and the low-side current regulators are turned off, the HOTDIE[1:0] bits are set and can only be reset by a read access. In the voltage mode operation (MODE_CTRL[1:0] = 11 or ENVM = 1), the device continues its operation when the junction temperature falls below 140°C typ. again. In the current regulation mode (i.e., video light or flash modes), device operation is suspended.

Table 5. Die Temperature Bits

HOTDIE[1:0]	T_J
00	<55°C
01	55°C <= T_J <= 70°C
10	>70°C
11	Thermal shutdown tripped. The bit is reset after read access

Current Limit

The TPS6131x devices employ a programmable inductor-current limit. This allows choosing inductors with different saturation-current ratings. Furthermore, this provides protection against a shorted inductor, or if the inductance value has dramatically dropped. This protects the battery from excessively-high current drain.

The current limit circuit employs a valley current sensing scheme. The detection threshold is user selectable via the ILIM bit. The ILIM bit can only be set prior to entering operation, i.e. initial shutdown state.

Figure 46 illustrates the inductor and rectifier current waveforms during current limit operation. The output current, IOUT, is the average of the rectifier ripple current waveform. When the load current is increased such that the lower peak is above the current limit threshold, the off time is lengthened to allow the current to decrease to this threshold before the next on-time begins (so called frequency fold-back mechanism).

Copyright © 2010, Texas Instruments Incorporated

查询"TPS61310"供应商

Both the output voltage and the switching frequency are reduced as the power stage of the device operates in a constant current mode. The maximum continuous output current ($I_{OUT(CL)}$), before entering current limit operation, can be defined as:

$$I_{OUT(CL)} = (1 - D) \times \left(I_{VALLEY} + \frac{1}{2} \Delta I_L\right) \text{ with } \Delta I_L = \frac{V_{IN}}{L} \times \frac{D}{f} \text{ and } D \approx \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (1)$$

The TPS6131x device also provides a negative current limit (≈ 300mA) to prevent an excessive reverse inductor current when the power stage sinks current from the output in the forced continuous-conduction mode.

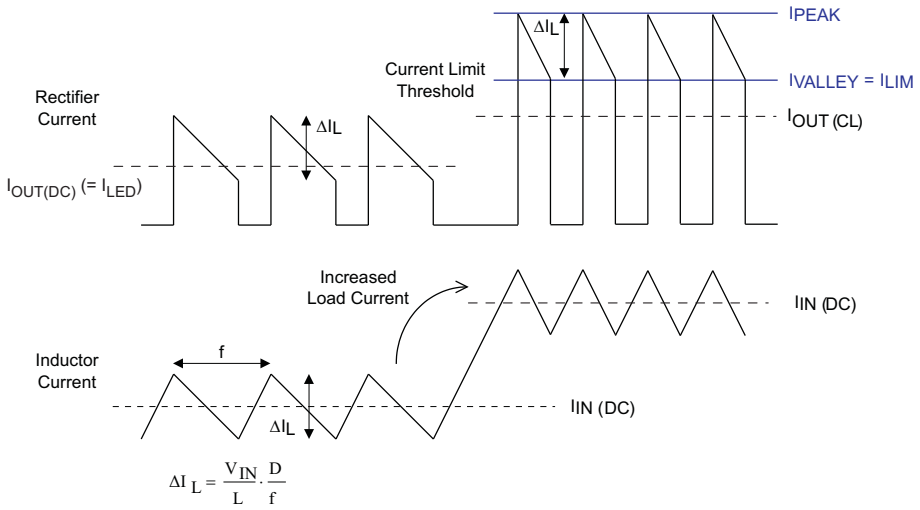


Figure 46. Inductor/Rectifier Currents in Current Limit Operation

Table 6. Inductor Current Limit Operation

CURRENT LIMIT SETTING	ILIM BIT
1250 mA	Low
1750 mA	High

Flash Blanking (Tx-Mask) for Instantaneous Flash-Current Reduction

The TPS6131x devices offer a dedicated hardware signal input (Tx-Mask) that can be used to reduce the flash current to the programmed video light level instantaneously.

This feature can be used to reduce the overall current drawn from the battery if other system components require high energy simultaneously, e.g. during a RF PA transmission pulse.

The Tx-MASK function has no influence on the safety timer duration.

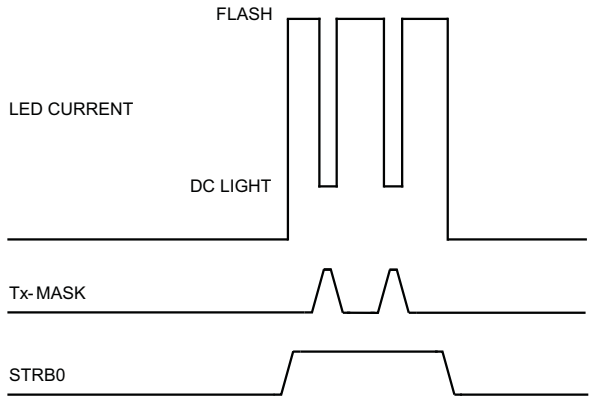


Figure 47. Synchronized Flash With Blanking Periods (STRB1 = 0)

查询 TPS61310 供应商

POWER-SAVE MODE OPERATION, EFFICIENCY

The TPS6131x integrates a power-save mode to improve efficiency under light loads. In power-save mode the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with one-to-several pulses and returns to power-save mode once the output voltage exceeds the set threshold voltage.

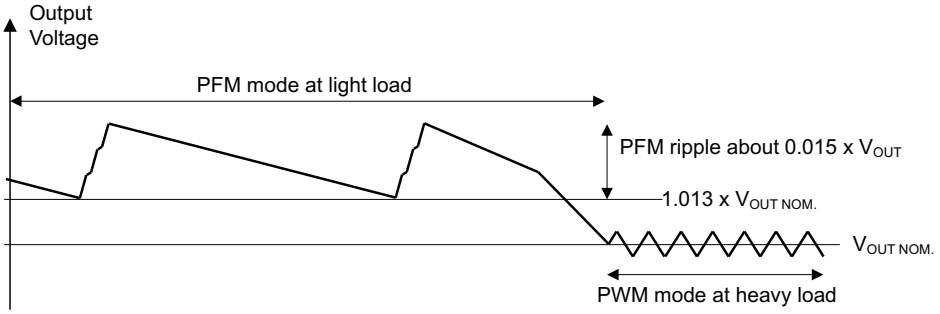


Figure 48. Operation in PFM Mode and Transfer to PWM Mode

The power-save mode can be enabled and disabled via the ENPSM bit. In down conversion mode, power-save mode is always active and the device cannot be forced into fixed frequency operation at light loads.

The LED sense voltage has a direct effect on converter efficiency. Because the voltage across the low-side current regulator does not contribute to the output power (LED brightness), the lower the sense voltage the higher the efficiency will be.

The integrated current control loop automatically selects the minimum boost ratio to maintain regulation based on the LED forward voltage and current requirements. The low-side current regulators drop the voltage difference between the input voltage and the LEDs forward voltage ($V_{F(LED)} < V_{IN}$). When running in boost mode ($V_{F(LED)} > V_{IN}$), the voltage present at the LED1-3 pins of the low-side current regulators is typically 400mV, leading to high power conversion efficiency. Depending on the input voltage and the LEDs forward voltage characteristic the converter efficiency is approximately 75% to 90%.

START-UP SEQUENCE

To avoid high inrush current during start-up, special care is taken to control the inrush current. When the device enables, the internal startup cycle starts with the first step, the pre-charge phase.

During pre-charge, the rectifying switch is turned on until the output capacitor is either charged to a value close to the input voltage or ≈ 3.3V, whichever occurs first. The rectifying switch is current-limited during that phase. The current limit increases with decreasing input-to-output voltage difference. This circuit also limits the output current under output short-circuit conditions.

After having pre-charged the output capacitor, the device starts switching, and increases its current limit in three steps of typically 25mA, 250mA and full current limit (ILIM setting). The current-limit transition from the first to the second step occurs after 1ms of operation. Full current limit operation is set once the output voltage has reached its regulation limits. In this mode, the active balancing circuit is disabled.

NRESET INPUT: HARDWARE ENABLE / DISABLE

The TPS6131x family features a hardware reset pin (NRESET). This reset pin allows the device to be disabled by an external controller without requiring an I^2C write command. Under normal operation, the NRESET pin should be held high to prevent an unwanted reset. When the NRESET is driven low, the I^2C control interface and all internal control registers are reset to the default states and the part enters shutdown mode.

SHUTDOWN

Writing 00 to MODE_CTRL[1:0] bits forces the device into shutdown. The shutdown state can only be entered when the voltage regulation (ENVM = 0) and light modes are both turned off.

In the shutdown state:

- The regulator stops switching.

Copyright © 2010, Texas Instruments Incorporated

查询"TPS61310"供应商

- The high-side PMOS disconnects the load from the input.
- The LEDx pins are high impedance thus eliminating any DC conduction path.
- The TPS6131x device actively discharges the output capacitor when it turns off.

SERIAL INTERFACE DESCRIPTION

I²C™ is a 2-wire serial interface developed by Philips Semiconductor, now NXP Semiconductors (see I²C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is *idle*, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A *master* device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A *slave* device receives and/or transmits data on the bus under control of the master device.

The TPS6131x device works as a *slave* and supports the following data transfer *modes*, as defined in the I²C-Bus Specification: standard mode (100 kbps) and fast mode (400 kbps), and high-speed mode (3.4 Mbps). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as supply voltage remains above 2.1V.

The data transfer protocol for standard and fast modes is exactly the same, therefore they are referred to as F/S-mode in this document. The protocol for high-speed mode is different from F/S-mode, and it is referred to as HS-mode. The TPS6131x device supports 7-bit addressing; 10-bit addressing and general call address are not supported. The device 7bit address is defined as '011 0011'.

F/S-Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 49. All I²C-compatible devices should recognize a start condition.

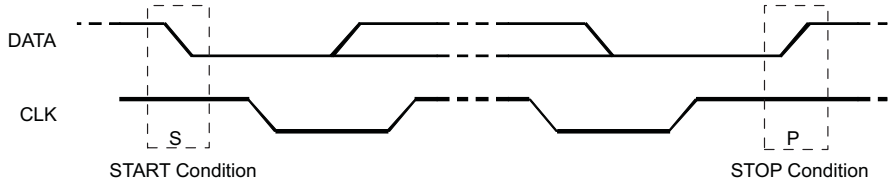


Figure 49. START and STOP Conditions

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master checks for valid data. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 50). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 51) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.

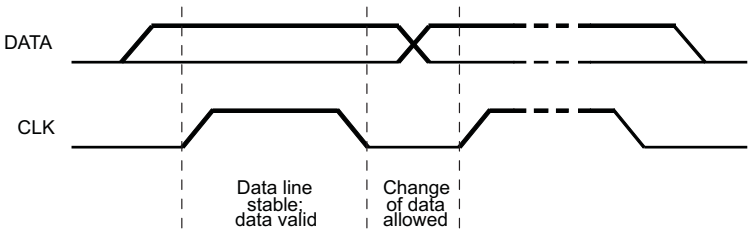


Figure 50. Bit Transfer on the Serial Interface

The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 49). This releases the bus and stops the communication link with the addressed slave. All I^{2}C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section will result in 00h being read out.

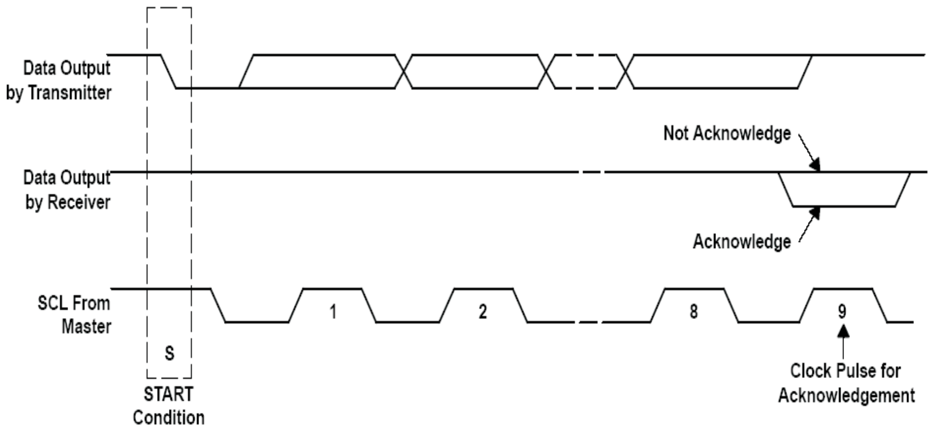


Figure 51. Acknowledge on the I^{2}C Bus

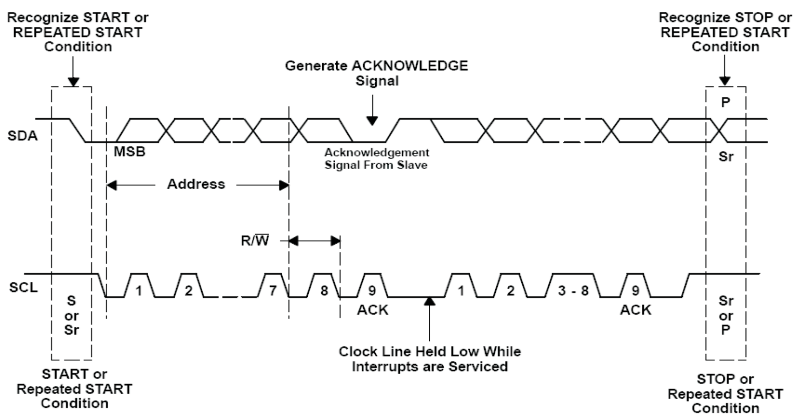


Figure 52. Bus Protocol

H/S-Mode Protokoll

The master generates a start condition followed by a valid serial byte containing HS master code 00001XXX. This transmission is made in F/S-mode at no more than 400 Kbps. No device is allowed to acknowledge the HS master code, but all devices must recognize it and switch their internal setting to support 3.4 Mbps operation.

The master then generates a *repeated start condition* (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S-mode, except that transmission speeds up to 3.4 Mbps are allowed. A stop condition ends the HS-mode and switches all the internal settings of the slave devices to support the F/S-mode. Instead of using a stop condition, repeated start conditions should be used to secure the bus in HS-mode.

Attempting to read data from register addresses not listed in this section will result in 00h being read out.

 Copyright © 2010, Texas Instruments Incorporated

查询"TPS61310"供应商

TPS6131x I²C Update Sequence

The TPS6131x requires a start condition, a valid I²C address, a register address byte, and a data byte for a single update. After the receipt of each byte, TPS6131x device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the TPS6131x. TPS6131x performs an update on the falling edge of the acknowledge signal that follows the LSB byte.

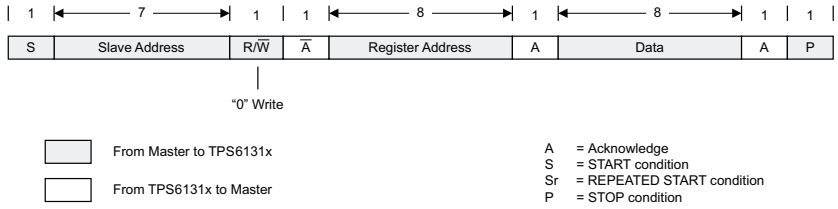


Figure 53. : "Write" Data Transfer Format in F/S-Mode

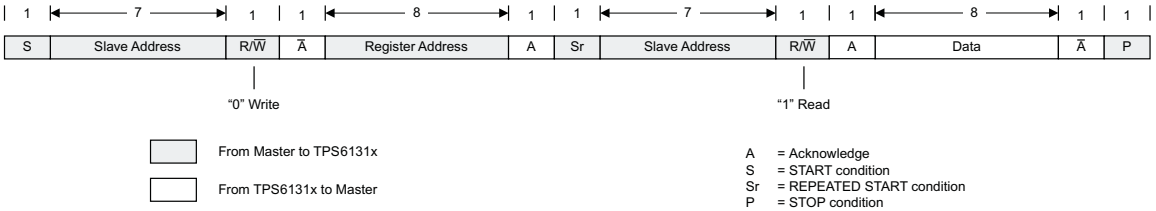


Figure 54. "Read" Data Transfer Format in F/S-Mode

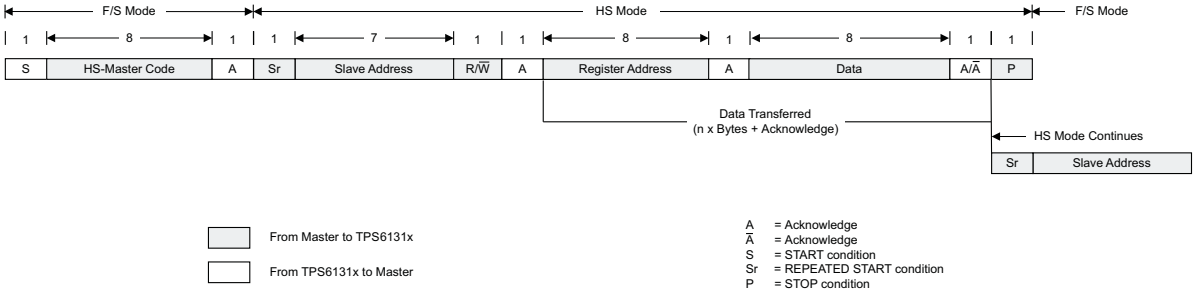


Figure 55. Data Transfer Format in H/S-Mode

Slave Address Byte

MSB							LSB
X	X	X	X	X	X	A1	A0

The slave address byte is the first byte received following the START condition from the master device.

Register Address Byte

MSB							LSB
0	0	0	0	00	D2	D1	D0

Following the successful acknowledgment of the slave address, the bus master will send a byte to the TPS6131x, which will contain the address of the register to be accessed.

Copyright © 2010, Texas Instruments Incorporated

查询 TPS61310 供应商

REGISTER DESCRIPTIONS

REGISTER0 DESCRIPTION

Memory location: 0x00

Description	RESET	FREE	DCLC13[2:0]			DCLC2[2:0]		
Bits	D7	D6	D5	D4	D3	D2	D1	D0
Memory type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default value	0	0	0	0	1	0	1	0

Bit	Description
RESET	**Register Reset bit.** 0: Normal operation. 1: Default values are set to all internal registers.
DCLC13[2:0]	**Video Light Current Control bits (LED1/3).** 000: 0mA. (1) (2) 001: 25mA 010: 50mA 011: 75mA 100: 100mA 101: 125mA 110: 150mA 111: 175mA
DCLC2[2:0]	**Video Light Current Control bits (LED2).** 000: 0mA. (1) (2) 001: 25mA 010: 50mA 011: 75mA 100: 100mA 101: 125mA 110: 150mA, 225mA current level can be activated simultaneously with Tx-MASK = 1 111: 175mA, 325mA current level can be activated simultaneously with Tx-MASK = 1

(1) LEDs are off, V_{OUT} set according to OV[3:0].
(2) When DCLC2[2:0] and DCLC13[2:0] are both reset, the device operates in voltage regulation mode. The output voltage is set according to OV[3:0].

Copyright © 2010, Texas Instruments Incorporated

查询"TPS61310"供应商

REGISTER1 DESCRIPTION

Memory location: 0x01

Description	MODE_CTRL[1:0]		FC2[5:0]					
Bits	D7	D6	D5	D4	D3	D2	D1	D0
Memory type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default value	0	0	0	1	0	0	0	0

Bit	Description
MODE_CTRL[1:0]	**Mode Control bits.** 00: Device in shutdown mode. 01: Device operates in video light mode. 10: Device operates in flash mode. 11: Device operates as constant voltage source. To avoid device shutdown by video light safety timeout, MODE_CTRL[1:0] bits need to be refreshed within less than 13.0s. Writing to REGISTER1[7:6] automatically updates REGISTER2[7:6].
FC2[5:0]	**Flash Current Control bits (LED2).** 000000: 0mA.(1) (2) 000001: 25mA 000010: 50mA 000011: 75mA 000100: 100mA 000101: 125mA 000110: 150mA 000111: 175mA 001000: 200mA 001001: 225mA 001010: 250mA 001011: 275mA 001100: 300mA 001101: 325mA 001110: 350mA 001111: 375mA 010000: 400mA 010001: 425mA 010010: 450mA 010011: 475mA 010100: 500mA 010101: 525mA 010110: 550mA 010111: 575mA 011000: 600mA 011001: 625mA 011010: 650mA 011011: 675mA 011100: 700mA 011101: 725mA 011110: 750mA 011111: 775mA 100000 ... 111111: 800mA

(1) LEDs are off, V_{OUT} set according to OV[3:0].
(2) When FC13[4:0] and FC2[5:0] are both reset, the device operates in voltage regulation mode. The output voltage is set according to OV[3:0].

Copyright © 2010, Texas Instruments Incorporated

查询 TPS61310 供应商

REGISTER2 DESCRIPTION

Memory location: 0x02

Description	MODE_CTRL[1:0]		ENVM	FC13[4:0]				
Bits	D7	D6	D5	D4	D3	D2	D1	D0
Memory type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default value	0	0	0	0	1	0	0	0

Bit	Description
MODE_CTRL[1:0]	**Mode Control bits.** 00: Device in shutdown mode. 01: Device operates in video light mode. 10: Device operates in flash mode. 11: Device operates as constant voltage source. To avoid device shutdown by video light safety timeout, MODE_CTRL[1:0] bits need to be refreshed within less than 13.0s. Writing to REGISTER2[6:5] automatically updates REGISTER1[6:5].
ENVM	Enable Voltage Mode bit. 0: Normal operation. 1: Forces the device into a constant voltage source. In read mode, the ENVM bit is automatically updated to reflect the logic state of the ENVM input pin.
FC13[4:0]	**Flash Current Control bits (LED1/3).** 00000: 0mA.(1) (2) 00001: 25mA 00010: 50mA 00011: 75mA 00100: 100mA 00101: 125mA 00110: 150mA 00111: 175mA 01000: 200mA 01001: 225mA 01010: 250mA 01011: 275mA 01100: 300mA 01101: 325mA 01110: 350mA 01111: 375mA 10000 ... 11111: 400mA

(1) LEDs are off, V_{OUT} set according to OV[3:0].
(2) When FC13[4:0] and FC2[5:0] are both reset, the device operates in voltage regulation mode. The output voltage is set according to OV[3:0].

Copyright © 2010, Texas Instruments Incorporated

查询"TPS61310"供应商

REGISTER3 DESCRIPTION

Memory location: 0x03

Description	STIM[2:0]			HPLF	SELSTIM (W) TO ®)	STT	SFT	Tx-MASK
Bits	D7	D6	D5	D4	D3	D2	D1	D0
Memory type	R/W	R/W	R/W	R	R	R/W	R/W	R/W
Default value	1	1	0	0	0	0	0	1

Bit	Description
STIM[2:0]	**Safety Timer bits.**

STIM[2:0]	RANGE 0	RANGE 1
000	68.2ms	5.3ms
001	102.2ms	10.7ms
010	136.3ms	16.0ms
011	170.4ms	21.3ms

STIM[2:0]	RANGE 0	RANGE 1
100	204.5ms	26.6ms
101	340.8ms	32.0ms
110	579.3ms	37.3ms
111	852ms	71.5ms

HPFL — **High-Power LED Failure flag.**
0: Proper LED operation.
1: LED failed (open or shorted).
High-power LED failure flag is reset after readout

SELSTIM — **Safety Timer Selection Range (Write Only).**
0: Safety timer range 0.
1: Safety timer range 1.

TO — **Time-Out Flag (Read Only).**
0: No time-out event occurred.
1: Time-out event occurred. Time-out flag is reset at re-start of the safety timer.

STT — **Safety Timer Trigger bit.**
0: LED safety timer is level sensitive.
1: LED safety timer is rising edge sensitive.
This bit is only valid for MODE_CTRL[1:0] = 10.

SFT — **Start/Flash Timer bit.**
In write mode, this bit initiates a flash strobe sequence.
0: No change in the high-power LED current.
1: High-power LED current ramps to the flash current level.
In read mode, this bit indicates the high-power LED status.
0: High-power LEDs are idle.
1: Ongoing high-power LED flash strobe.

Tx-MASK — **Flash Blanking Control bit.**
In write mode, this bit enables/disables the flash blanking/LED current reduction function.
0: Flash blanking disabled.
1: LED current is reduced to video light level when Tx-MASK input is high.
In read mode, this flag indicates whether or not the flash masking input has been activated. Tx-MASK flag is reset after readout of the flag.
0: No flash blanking event occurred.
1: Tx-MASK input triggered.

Copyright © 2010, Texas Instruments Incorporated

查询 TPS61310 供应商

REGISTER4 DESCRIPTION

Memory location: 0x04

Description	PG	HOTDIE[1:0]		ILIM	INC[3:0]			
Bits	D7	D6	D5	D4	D3	D2	D1	D0
Memory type	R/W	R	R	R/W	R/W	R/W	R/W	R/W
Default value	0	0	0	0	0	0	0	0

Bit	Description
PG	**Power Good bit.** In write mode, this bit selects the functionality of the GPIO/PG output. 0: PG signal is routed to the GPIO port. 1: GPIO PORT VALUE bit is routed to the GPIO port. In read mode, this bit indicates the output voltage conditions. 0: The converter is not operating within the voltage regulation limits. 1: The output voltage is within its nominal value.
HOTDIE[1:0]	**Instantaneous Die Temperature bits.** 00: T_J < +55°C 01: +55°C < T_J < +70°C 10: T_J > +70°C 11: Thermal shutdown tripped. Indicator flag is reset after readout.
ILIM	**Inductor Valley Current Limit bit.** The ILIM bit can only be set before the device enters operation (i.e. initial shutdown state).

VALLEY CURRENT LIMIT SETTING	ILIM BIT SETTING
1250mA	Low
1750mA	High

INDC[3:0] **Indicator Light Control bits.**

INDC[3:0]	PRIVACY INDICATOR INDLED CHANNEL
0000	Privacy indicator turned off
0001	INDLED current = 2.6mA(2)
0010	INDLED current = 5.2mA(2)
0011	INDLED current = 7.9mA(2)
0100	Privacy indicator turned off
0101	INDLED current = 5.2mA(2)
0110	INDLED current = 10.4mA(2)
0111	INDLED current = 15.8mA (2)

INDC[3:0]	PRIVACY INDICATOR LED1-3 CHANNELS (1)
1000	5% PWM dimming ratio
1001	11% PWM dimming ratio
1010	17% PWM dimming ratio
1011	23% PWM dimming ratio
1100	30% PWM dimming ratio
1101	36% PWM dimming ratio
1110	48% PWM dimming ratio
1111	67% PWM dimming ratio

(1) This mode of operation can only be activated for MODE_CTRL[1:0] = 01 & ENVM = 1.
(2) The output node (VOUT) is internally pulled to ground.

Copyright © 2010, Texas Instruments Incorporated

查询"TPS61310"供应商

REGISTER5 DESCRIPTION

Memory location: 0x05

Description	SELFCAL	ENPSM	DIR (W) STSTRB1 ®)	GPIO	GPIOTYPE	ENLED3	ENLED2	ENLED1
Bits	D7	D6	D5	D4	D3	D2	D1	D0
Memory type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default value	0	1	1	0	1	0	1	0

Bit	Description
SELFCAL	**High-Current LED Forward Voltage Self-Calibration Start bit.** In write mode, this bit enables/disables the output voltage vs. LED forward voltage/current self-calibration procedure. 0: Self-calibration disabled. 1: Self-calibration enabled. In read mode, this bit returns the status of the self-calibration procedure. 0: Self-calibration ongoing 1: Self-calibration done Notice that this bit is only being reset at the (re-)start of a calibration cycle.
ENPSM	**Enable / Disable Power-Save Mode bit.** 0: Power-save mode disabled. 1: Power-save mode enabled.
STSTRB1	**STRB1 Input Status bit (Read Only).** This bit indicates the logic state on the STRB1 state.
DIR	**GPIO Direction bit.** 0: GPIO configured as input. 1: GPIO configured as output.
GPIO	**GPIO Port Value.** This bit contains the GPIO port value.
GPIOTYPE	**GPIO Port Type.** 0: GPIO is configured as push-pull output. 1: GPIO is configured as open-drain output.
ENLED3	**Enable / Disable High-Current LED3 bit.** 0: LED3 input is disabled. 1: LED3 input is enabled.
ENLED2	**Enable / Disable High-Current LED2 bit.** 0: LED2 input is disabled. 1: LED2 input is enabled.
ENLED1	**Enable / Disable High-Current LED1 bit.** 0: LED1 input is disabled. 1: LED1 input is enabled.

Copyright © 2010, Texas Instruments Incorporated

查询 TPS61310 供应商

REGISTER6 DESCRIPTION

Memory location: 0x06

Description	ENTS	LEDHOT	LEDWARN	LEDHDR	OV[3:0]			
Bits	D7	D6	D5	D4	D3	D2	D1	D0
Memory type	R/W	R/W	R	R	R/W	R/W	R/W	R/W
Default value	0	0	0	0	1	0	0	1

Bit	Description
ENTS	**Enable / Disable LED Temperature Monitoring.** 0: LED temperature monitoring disabled. 1: LED temperature monitoring enabled.
LEDHOT	**LED Excessive Temperature Flag.** This bit can be reset by writing a logic level zero. 0: TS input voltage > 0.345V. 1: TS input voltage < 0.345V.
LEDWARN	**LED Temperature Warning Flag (Read Only).** This flag is reset after readout. 0: TS input voltage > 1.05V. 1: TS input voltage < 1.05V.
LEDHDR	**LED High-Current Regulator Headroom Voltage Monitoring bit.** This bit returns the headroom voltage status of the LED high-current regulators. This value is being updated at the end of a flash strobe, prior to the LED current ramp-down phase. 0: Low headroom voltage. 1: Sufficient headroom voltage.
0V[3:0]	**Output Voltage Selection bits.** In read mode, these bits return the result of the high-current LED forward voltage self-calibration procedure. In write mode, these bits are used to set the target output voltage (refer to voltage regulation mode). In applications requiring dynamic voltage control, care should be take to set the new target code after voltage mode operation has been enabled (MODE_CTRL[1:0] = 11 and/or ENVM bit = 1).

OV[3:0]	Target Output Voltage
0000	3.825V
0001	3.950V
0010	4.075V
0011	4.200V
0100	4.325V
0101	4.450V
0110	4.575V
0111	4.700V
1000	4.825V
1001	4.950V
1010	5.075V
1011	5.200V
1100	5.325V
1101	5.450V
1110	5.575V
1111	5.700V

Copyright © 2010, Texas Instruments Incorporated

查询"TPS61310"供应商

REGISTER7 DESCRIPTION

Memory location: 0x07

Description	ENBATMON	BATDROOP[2:0]			FREE	REVID[2:0]		
Bits	D7	D6	D5	D4	D3	D2	D1	D0
Memory type	R/W	R/W	R/W	R/W	R/W	R	R	R
Default value	0	1	0	0	0	1	1	0

Bit	Description
ENBATMON	**Enable / Disable Battery Voltage Droop Monitoring Bit** 0: Battery voltage droop monitoring disabled. 1: Battery voltage droop monitoring enabled.
BATDROOP[2:0]	**Battery Voltage Droop** 000: 50mV 001: 75mV 010: 100mV 011: 125mV 100: 150mV 101: 175mV 110: 200mV 111: 225mV
REVID[2:0]	**Silicon Revision ID**

APPLICATION INFORMATION

INDUCTOR SELECTION

A boost converter requires two main passive components for storing energy during the conversion. A boost inductor and a storage capacitor at the output are required.

The TPS6131x device integrates current-limit protection circuitry. The valley current of the PMOS rectifier is sensed to limit the maximum current flowing through the synchronous rectifier and the inductor. The valley peak current limit (1250mA/1750mA) is user selectable via the I^2C interface.

In order to optimize solution size the TPS6131x device has been designed to operate with inductance values between a minimum of 1.3 μH and maximum of 2.9 μH. In typical high-current white LED applications a 2.2μH inductance is recommended.

The highest peak current through the inductor and the power switch depends on the output load, the input and output voltages. The maximum average inductor current and the maximum inductor peak current can be estimated using Equation 2 and Equation 3:

$$I_L \approx I_{OUT} \times \frac{V_{OUT}}{\eta \times V_{IN}} \quad (2)$$

$$I_{L(PEAK)} = \frac{V_{IN} \times D}{2 \times f \times L} + \frac{I_{OUT}}{(1-D) \times \eta} \quad \text{with } D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (3)$$

With

f = switching frequency (2MHz)
L = inductance value (2.2μH)
η = estimated efficiency (85%)

The losses in the inductor caused by magnetic hysteresis losses and copper losses are a major parameter for total circuit efficiency.

Table 7. List of Inductors

MANUFACTURER	SERIES	DIMENSIONS	ILIM SETTINGS
TDK	VLF3014AT	2.6mm x 2.8mm x 1.4mm max. height	1250mA (typ.)
COILCRAFT	LPS3015	3.0mm x 3.0mm x 1.5mm max. height	
MURATA	LQH2HPN	2.5mm x 2.0mm x 1.2mm max. height	
TOKO	FDSE0312	3.0mm x 3.0mm x 1.2mm max. height	1750mA (typ.)
MURATA	LQM32PN	3.2mm x 2.5mm x 1.0mm max. height	

Copyright © 2010, Texas Instruments Incorporated

查询"TPS61310"供应商

INPUT CAPACITOR

For good input-voltage filtering, low ESR ceramic capacitors are recommended. A 10μF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. The input capacitor should be placed as close as possible to the input pin of the converter.

OUTPUT CAPACITOR

The major parameter necessary to define the output capacitor is the maximum allowed output-voltage ripple of the converter. This ripple is determined by two parameters of the capacitor, the capacitance and the ESR. It is possible to calculate the minimum capacitance needed for the defined ripple, supposing that the ESR is zero, by using Equation 4:

$$C_{min} \approx \frac{I_{OUT} \times (V_{OUT} - V_{IN})}{f \times \Delta V \times V_{OUT}} \quad (4)$$

Parameter f is the switching frequency and ΔV is the maximum allowed ripple.

With a chosen ripple voltage of 10mV, a minimum capacitance of 10μF is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using Equation 5:

$$\Delta V_{ERR} = I_{OUT} \times R_{ESR} \quad (5)$$

The total ripple is the sum of the ripple caused by the capacitance and the ripple caused by the ESR of the capacitor. Additional ripple is caused by load transients. This means that the output capacitor has to completely supply the load during the charging phase of the inductor. A reasonable value of the output capacitance depends on the speed of the load transients and the load current during the load change.

For the standard current white LED application, a minimum of 3μF effective output capacitance is usually required when operating with 2.2μH (typ) inductors. For solution size reasons, this is usually one or more X5R/X7R ceramic capacitors.

Depending on the material, size and therefore margin to the rated voltage of the used output capacitor, degradation on the effective capacitance can be observed. This loss of capacitance is related to the DC bias voltage applied. It is therefore always recommended to check that the selected capacitors are showing enough effective capacitance under real operating conditions.

Copyright © 2010, Texas Instruments Incorporated

查询"TPS61310"供应商

NTC SELECTION

The TPS6131x requires a negative thermistor (NTC) for sensing the LED temperature. Once the temperature monitoring feature is activated, a regulated bias current (c.a. 24μA) is driven out of the TS port to produce a voltage across the thermistor.

If the temperature of the NTC-thermistor rises due to the heat dissipated by the LED, the voltage on the TS input pin decreases. When this voltage goes below the “warning threshold”, the LEDWARN bit in REGISTER6 is set. This flag is cleared by reading the register.

If the voltage on the TS input decreases further and falls below “hot threshold”, the LEDHOT bit in REGISTER6 is set and the device goes automatically in shutdown mode to avoid damaging the LED. This status is latched until the LEDHOT flag gets cleared by software.

The selection of the NTC-thermistor value strongly depends on the power dissipated by the LED and all components surrounding the temperature sensor and on the cooling capabilities of each specific application. With a 220kΩ (at 25°C) thermistor, the valid temperature window is set between 60°C to 90°C. The temperature window can be enlarged by adding external resistors to the TS pin application circuit. In order to obtain proper triggering of the LEDWARN and LEDHOT flags in noisy environments, the TS signal may require additional filtering capacitance.

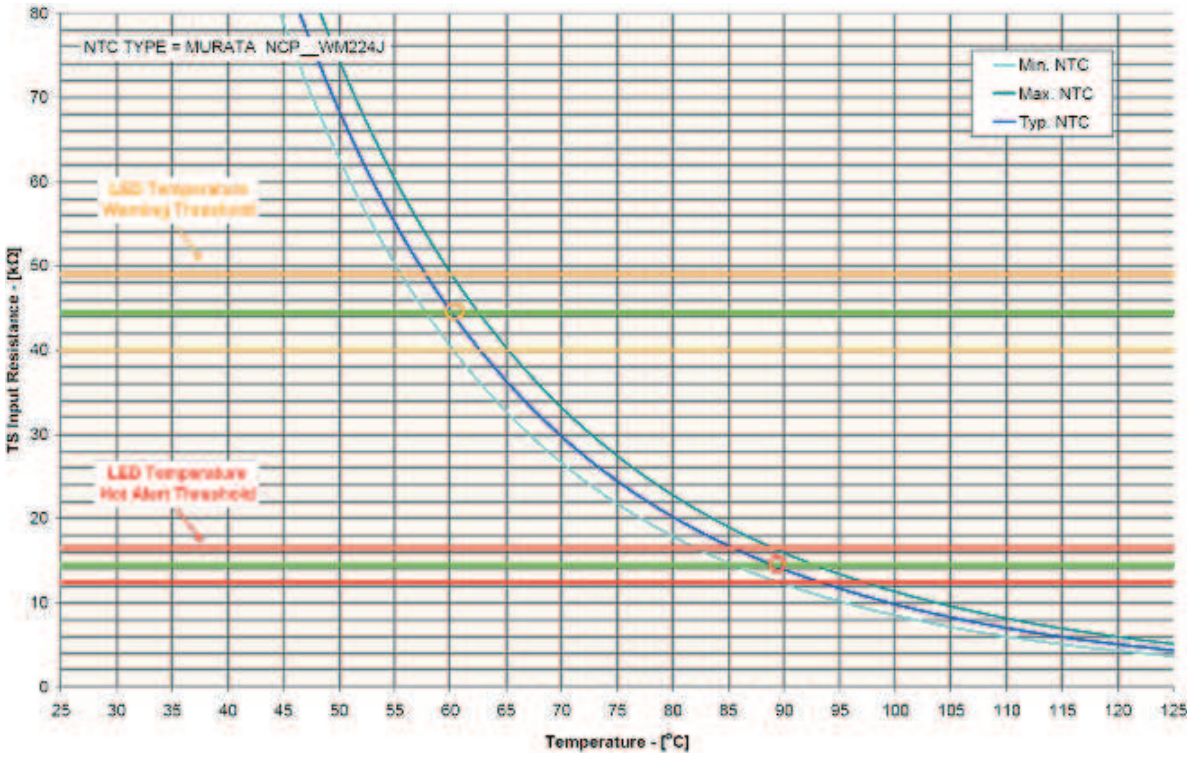


Figure 56. Temperature Monitoring Characteristic

Table 8. List of Negative Thermistor (NTC)

MANUFACTURER	PART NUMBER	VALUE
MURATA	NCP18WM224J03RB	220kΩ

Copyright © 2010, Texas Instruments Incorporated

查询"TPS61310"供应商

CHECKING LOOP STABILITY

The first step of circuit and stability evaluation is to examine the following signals from a steady-state perspective:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{OUT(AC)}$

These are the basic signals that must be measured when evaluating a switching converter. If the switching waveform shows large duty-cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of improper board layout and/or L-C combination.

As a next step in the evaluation of the regulation loop, test the load transient response. VOUT can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. With no ringing, the loop has usually more than 45° of phase margin.

Because the damping factor of the circuitry is directly related to several resistive parameters (e.g., MOSFET $r_{DS(on)}$) that are temperature dependant, the loop stability should be analyzed over the input voltage range, output current range, and temperature range.

LED FLASH CURRENT LEVEL OPTIMIZATION vs. BATTERY DROOP

In cell phone applications, the camera engine is normally specified over an operating temperature range down to 0°C or –10°C. In order to achieve a reliable system operation, the LED flash current needs to be rated according to the maximum tolerable battery voltage drop (i.e. highest battery impedance, lowest ambient temperature).

To dynamically optimize the LED flash current (i.e. light output) vs. battery state-of-charge and temperature, we could consider the following self-adjustment procedure. This algorithm could be embedded into the auto-exposure, auto white-balance or red-eye reduction pre-flash algorithms.

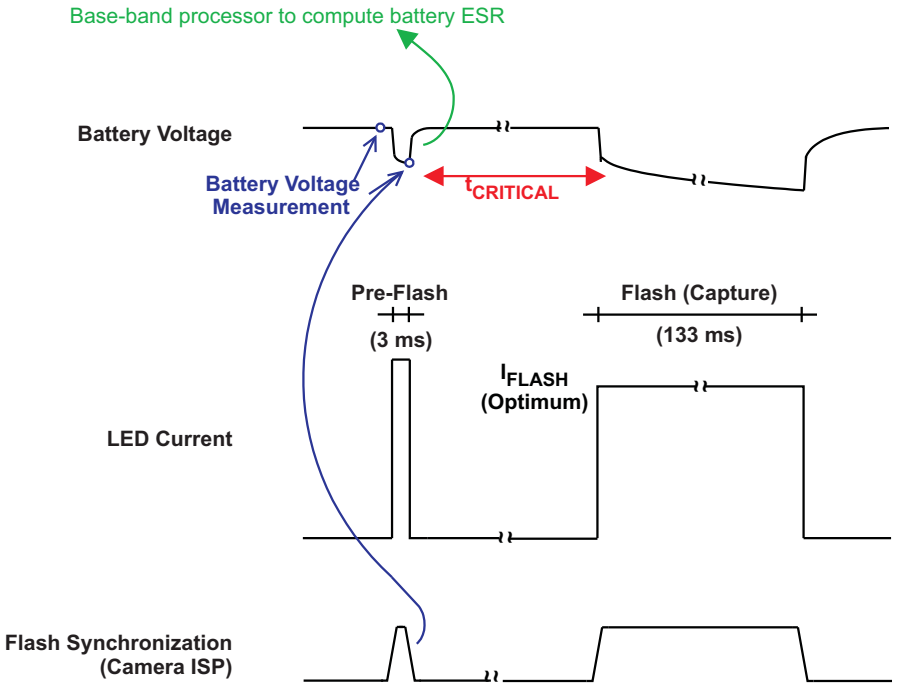


Figure 57. Image Capture Sequence

- **Phase 1: Pre-Flash, Battery Impedance Estimation**

  The battery voltage usually drops by a few hundreds of millivolts during a high-power flash strobe. For short durations, this voltage droop should not be subject to the battery intrinsic capacitance (i.e. relaxation effect) but rather to its cell impedance.

  Based on the state of the Tx-MASK input, the battery voltage drop (during pre-flash) and the LED current level, the base-band processor can compute an estimated cell-impedance value (ESR).

查询 TPS61310 供应商

Depending on the ambient temperature, the battery state-of-charge (SoC), the flash (capture) duration and the actual status of the various RF interfaces, the base-band processor can determine a safe battery voltage droop (to be tolerated during the forthcoming strobe sequence) as well as a maximum flash current rating. The maximum flash current setting can be estimated by considering nominal LEDs and approximately 85% power efficiency in the driver.

- **Phase 2: Battery Loading Monitoring Prior To Image Capture**

  For a reliable system operation, the base-band processor should make sure that no 'parasitic' high-current load suddenly impacts the budgeted battery voltage sag. The most critical timing is referenced as $t_{CRITICAL}$.

  The interrupt subroutine (running on the base-band processor) should be ready to detect any 'parasitic' battery load event that could occur prior to the image capture (refer to SFT bit description). In such a situation, the battery voltage droop budget and the maximum LED current settings would need to be revised.

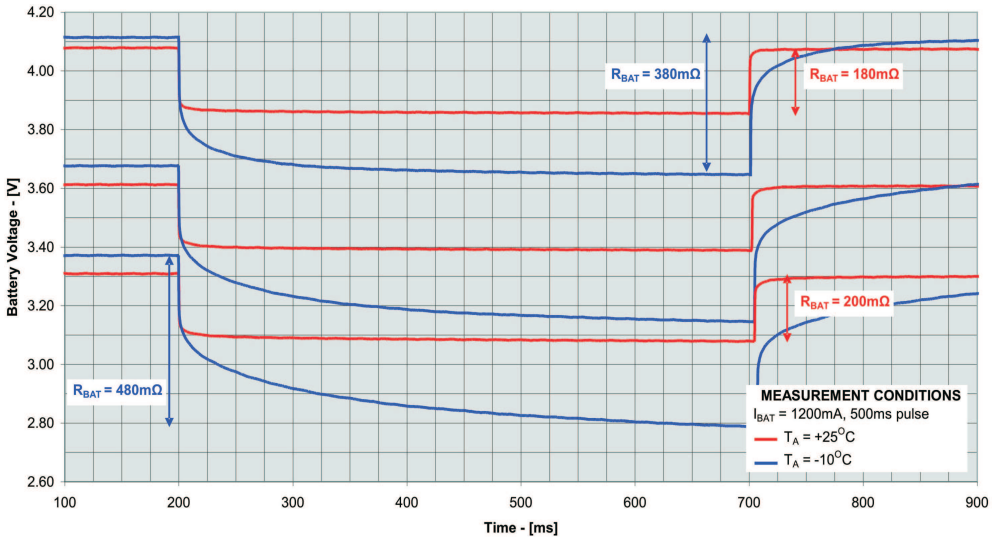


Figure 58. 900mAh, Li-Ion Battery Transient Response vs. SoC and Temperature

Copyright © 2010, Texas Instruments Incorporated

查询"TPS61310"供应商

LED FORWARD VOLTAGE CALIBRATION

High-power LEDs tend to exhibit a wide forward voltage distribution. The TPS6131x device integrates a self-calibration procedure that can be used to determine the optimum super-capacitor pre-charge voltage based on the actual worst case LED forward voltage and ESR of the storage capacitor. This calibration procedure is meant to start at a minimum output voltage, and can be initiated by writing the SELFCAL bit (preferably with MODE_CTRL[1:0] = 00, ENVM = 0).

The calibration procedure monitors the sense voltage across the low-side current regulators (according to ENLED[3:1] bits setting) and registers the worst case LED (i.e. the LED featuring the largest forward voltage). The TPS6131x device automatically sweeps through its output voltage range and performs a short duration flash strobe for each step (refer to FC13[4:0] and FC2[5:0] bits settings).

The sequence is stopped as soon as the device detects that each of the low-side current regulators have enough headroom voltage (i.e. 400mV typ.). The device returns the according output voltage in the register OV[3:0] and sets the SELFCAL bit. This bit is only being reset at the (re-)start of a calibration cycle. In other words, when SELFCAL is asserted the output voltage register (OV[3:0]) returns the result of the last calibration sequence.

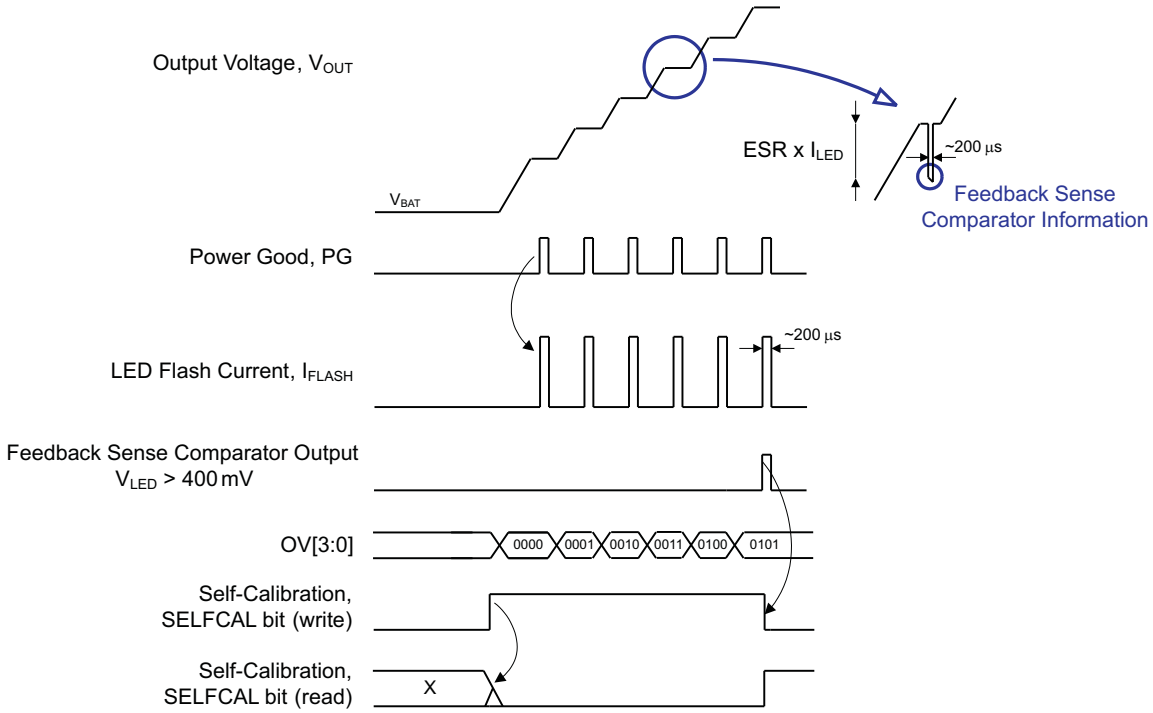


Figure 59. LED Forward Voltage Calibration Principle

查询 TPS61310 供应商

LAYOUT CONSIDERATIONS

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks.

The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

To lay out the control ground, it is recommended to use short traces as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

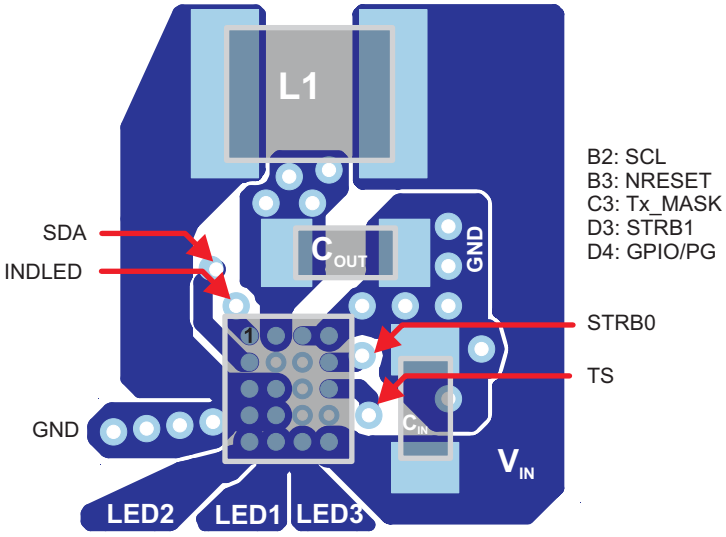


Figure 60. Suggested Layout (Top)

Copyright © 2010, Texas Instruments Incorporated

查询"TPS61310"供应商

THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependant issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

Junction-to-ambient thermal resistance is highly dependent on application and board layout. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. The maximum junction temperature (T_J) of the TPS6131x is 150°C.

The maximum power dissipation is especially critical when the device operates in the linear down mode at high LED current. For single-pulse power thermal analysis (e.g., flash strobe), the allowable power dissipation for the device is given by Figure 61. These values are derived using the reference design.

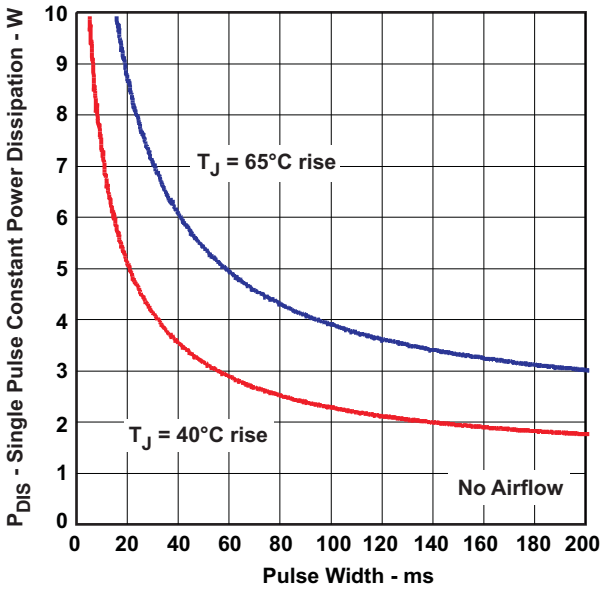


Figure 61. Single Pulse Power Capability

Copyright © 2010, Texas Instruments Incorporated

查询 TPS61310 供应商

TYPICAL APPLICATIONS

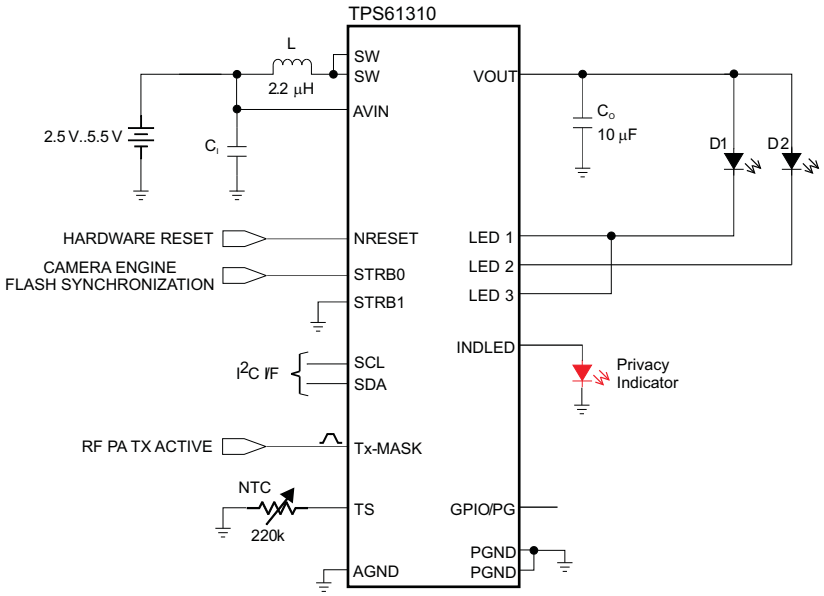


Figure 62. 2x 600mA High Power White LED Solution Featuring Privacy Indicator

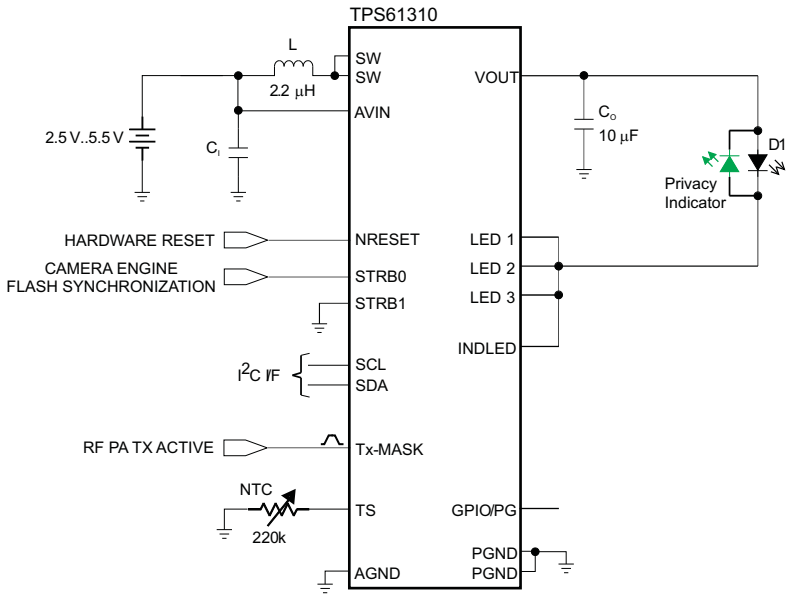


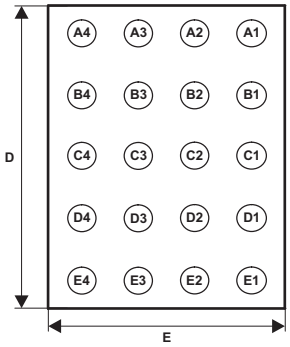
Figure 63. 1200mA High Power White LED Solution Featuring 'Back-Drive' Privacy Indicator

Copyright © 2010, Texas Instruments Incorporated

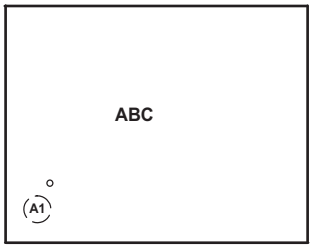
查询"TPS61310"供应商

PACKAGE SUMMARY

CHIP SCALE PACKAGE (BOTTOM VIEW)



CHIP SCALE PACKAGE (TOP VIEW)



Note: "ABC" is a place holder for the actual package marking. (See Table 1)

CHIP SCALE PACKAGE DIMENSIONS

The TPS6131x device is available in a 20-bump chip scale package (YFF, NanoFree™). The package dimensions are given as:

- D = 2170 ±30 μm
- E = 1928 ±30 μm

查询 TPS61310 供应商

REVISION HISTORY

Changes from Revision Initial (March 2010) to Revision A	Page
• Minor typos corrected throughout.	1

Copyright © 2010, Texas Instruments Incorporated

查询"TPS61310"供应商

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Communications and Telecom	www.ti.com/communications
DSP	dsp.ti.com	Computers and Peripherals	www.ti.com/computers
Clocks and Timers	www.ti.com/clocks	Consumer Electronics	www.ti.com/consumer-apps
Interface	interface.ti.com	Energy	www.ti.com/energy
Logic	logic.ti.com	Industrial	www.ti.com/industrial
Power Mgmt	power.ti.com	Medical	www.ti.com/medical
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Space, Avionics & Defense	www.ti.com/space-avionics-defense
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video and Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless-apps

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2010, Texas Instruments Incorporated