

查询"74HC533D-T"供应商

OCTAL D-TYPE TRANSPARENT LATCH, 3-STATE; INVERTING

FEATURES

- 3-state inverting outputs for bus oriented applications
- Common 3-state output enable input
- Output capability: bus driver
- I^{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT533 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT533 are octal D-type transparent latches featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE) input and an output enable (OE) input are common to all latches.

The "533" consists of eight D-type transparent latches with 3-state inverting outputs. When LE is HIGH, data at the D_n inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When OE is LOW, the contents of the 8 latches are available at the outputs. When OE is HIGH, the outputs go to the high impedance OFF-state. Operation of the OE input does not affect the state of the latches.

The "533" is functionally identical to the "373", "563" and "573", but the "373" and "573" have non-inverted outputs and the "563" and "573" have a different pin arrangement.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PHL} / t _{PLH}	propagation delay D _n to $\bar{Q}_n$ LE to $\bar{Q}_n$	C _L = 15 pF V _{CC} = 5 V	14 18	16 19	ns ns
C _I	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per latch	notes 1 and 2	34	34	pF

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μ W):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz C_L = output load capacitance in pF
f_o = output frequency in MHz V_{CC} = supply voltage in V
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

PACKAGE OUTLINES

20-lead DIL; plastic (SOT146).

20-lead mini-pack; plastic (SO20; SOT163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	OE	3-state output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	$\bar{Q}_0$ to $\bar{Q}_7$	3-state latch outputs
3, 4, 7, 8, 13, 14, 17, 18	D ₀ to D ₇	data inputs
10	GND	ground (0 V)
11	LE	latch enable input (active HIGH)
20	V _{CC}	positive supply voltage

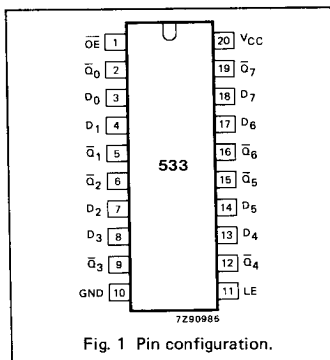


Fig. 1 Pin configuration.

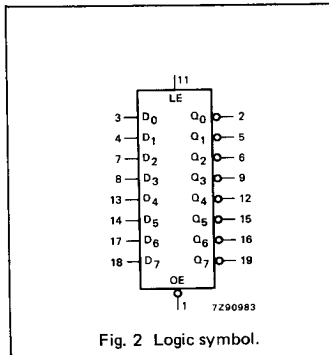


Fig. 2 Logic symbol.

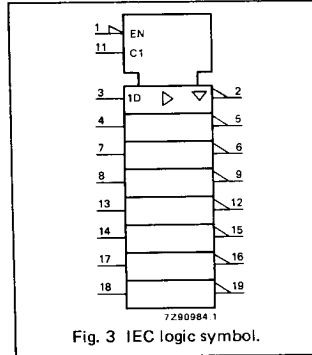
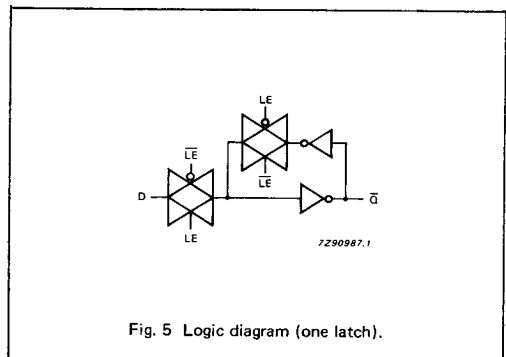
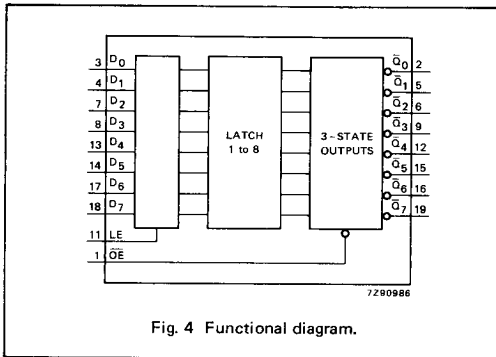


Fig. 3 IEC logic symbol.

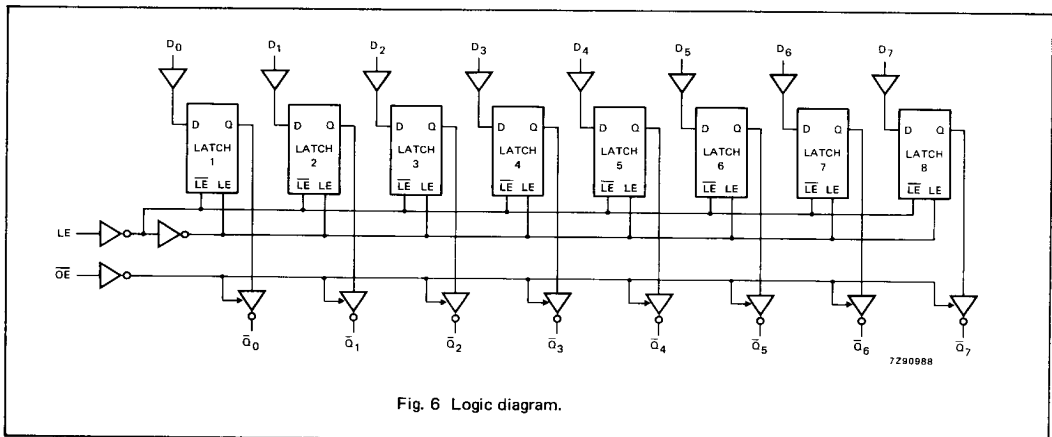
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FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS $\bar{Q}_0$ to $\bar{Q}_7$
	$\bar{OE}$	LE	D_n		
enable and read register. (transparent mode)	L	H	L	L	H
latch and read register	L	L	h	L	H
latch register and disable outputs	H	X	X	X	Z

H = HIGH voltage level
h = HIGH voltage level one set-up prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up prior to the HIGH-to-LOW LE transition
X = don't care
Z = high impedance OFF-state



[查询"74HC533D-T"供应商](#)**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I_{CC} category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS	
		74HC									V _{CC} V	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} / t _{PLH}	propagation delay D _n to Q _n		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7	
t _{PHL} / t _{PLH}	propagation delay LE to Q _n		58 21 17	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 8	
t _{PZH} / t _{PZL}	3-state output enable time OE to Q _n		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 9	
t _{PHZ} / t _{PLZ}	3-state output disable time OE to Q _n		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 9	
t _{THL} / t _{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 7	
t _W	LE pulse width HIGH	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8	
t _{su}	set-up time D _n to LE	50 10 9	3 1 1		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 10	
t _h	hold time D _n to LE	35 7 6	3 1 1		45 9 8		55 11 9		ns	2.0 4.5 6.0	Fig. 10	

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.

To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D _n	0.15
LE	0.30
OE	0.55

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V _{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay D _N to Q _N		19	34		43		51	ns	4.5	Fig. 7
t _{PHL} / t _{PLH}	propagation delay LE to Q _N		22	38		48		57	ns	4.5	Fig. 8
t _{PZH} / t _{PZL}	3-state output enable time OE to Q _N		19	35		44		53	ns	4.5	Fig. 9
t _{PHZ} / t _{PLZ}	3-state output disable time OE to Q _N		18	30		38		45	ns	4.5	Fig. 9
t _{THL} / t _{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 7
t _W	LE pulse width HIGH	16	5		20		24		ns	4.5	Fig. 8
t _{su}	set-up time D _N to LE	10	3		13		15		ns	4.5	Fig. 10
t _h	hold time D _N to LE	8	2		10		12		ns	4.5	Fig. 10

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AC WAVEFORMS

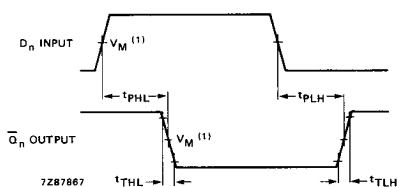


Fig. 7 Waveforms showing the data input (D_n) to output ($\overline{Q}_n$) propagation delays and the output transition times.

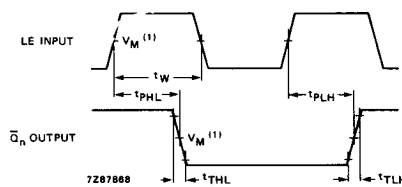


Fig. 8 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output ($\overline{Q}_n$) propagation delays and the output transition times.

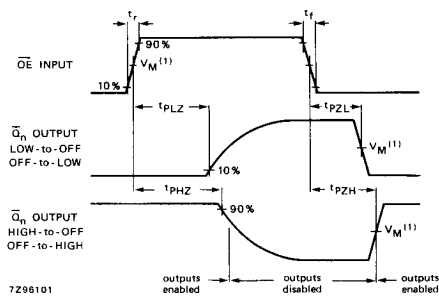


Fig. 9 Waveforms showing the 3-state enable and disable times.

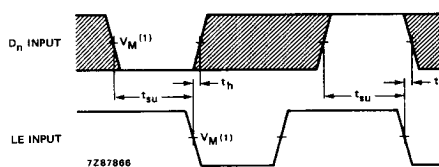


Fig. 10 Waveforms showing the data set-up and hold times for D_n input to LE input.

Note to Fig. 10

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.

HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.