

OKI Semiconductor

MSM514800D/DSL

524,288-Word x 8-Bit DYNAMIC RAM : FAST PAGE MODE TYPE

DESCRIPTION

The MSM514800D/DSL is a 524,288-word $\times$ 8-bit dynamic RAM fabricated in Oki's silicon-gate CMOS technology. The MSM514800D/DSL achieves high integration, high-speed operation, and low-power consumption because Oki manufactures the device in a quadruple-layer polysilicon/single-layer metal CMOS process. The MSM514800D/DSL is available in a 28-pin plastic SOJ. The MSM514800DSL (the self-refresh and lower-power version) is specially designed for lower-power applications.

FEATURES

- 524,288-word $\times$ 8-bit configuration
- Single 5V power supply, $\pm 10\%$ tolerance
- Input : TTL compatible, low input capacitance
- Output : TTL compatible, 3-state
- Refresh : 1,024 cycles/16 ms, 1,024 cycles/128 ms (SL Version)
- Fast page mode, read modify write capability
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, hidden refresh, $\overline{\text{RAS}}$ -only refresh capability
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self-refresh capability (SL version)
- Package options:

28-pin 400mil plastic SOJ

(SOJ28-P-400-1.27)

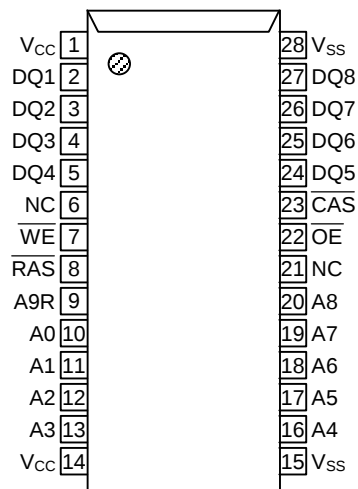
(Product : MSM514800D/DSL-xxJS)

xx : indicates speed rank.

PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}		Operating (Max.)	Standby (Max.)
MSM514800D/DSL	60ns	30ns	20ns	20ns	110ns	660mW	5.5mW/
	70ns	35ns	20ns	20ns	130ns	605mW	1.1mW (SL Version)

PIN CONFIGURATION (TOP VIEW)

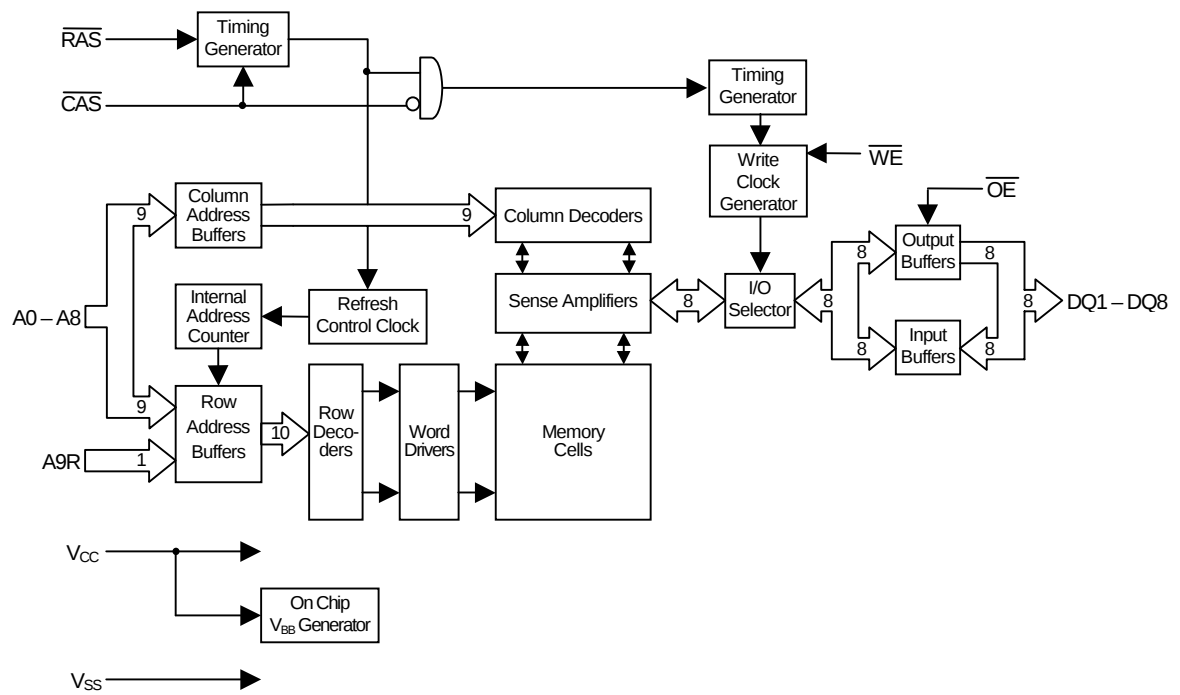


28-Pin Plastic SOJ

Pin Name	Function
A0 - A8, A9R	Address Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
DQ1 – DQ8	Data Input/Data Output
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
V _{CC}	Power Supply (5V)
V _{SS}	Ground (0V)
NC	No Connection

Note : The same power supply voltage must be provided to every V_{CC} pin, and the same GND voltage level must be provided to every V_{SS} pin.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	-1.0 to 7.0	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_{D^*}	1	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	-55 to 150	°C

*: $T_a = 25^{\circ}\text{C}$

Recommended Operating Conditions

 $(T_a = 0^{\circ}\text{C to } 70^{\circ}\text{C})$

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	6.5 *1	V
Input Low Voltage	V_{IL}	-1.0 *2	—	0.8	V

Notes: *1. The input voltage is $V_{CC} + 2.0\text{V}$ when the pulse width is less than 20ns (the pulse width is with respect to the point at which V_{CC} is applied).

*2. The input voltage is $V_{SS} - 2.0\text{V}$ when the pulse width is less than 20ns (the pulse width is with respect to the point at which V_{SS} is applied).

Capacitance

 $(V_{CC} = 5\text{V} \pm 10\%, T_a = 25^{\circ}\text{C}, f=1\text{MHz})$

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 – A8, A9R)	C_{IN1}	—	7	pF
Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ1 – DQ8)	$C_{I/O}$	—	8	pF

DC Characteristics

(V_{CC} = 5V ± 10%, Ta = 0°C to 70°C)

Parameter	Symbol	Condition	MSM514800 D/DSL-60		MSM514800 D/DSL-70		Unit	Note
			Min.	Max.	Min.	Max.		
Output High Voltage	V _{OH}	I _{OH} = -5.0mA	2.4	V _{CC}	2.4	V _{CC}	V	
Output Low Voltage	V _{OL}	I _{OL} = 4.2mA	0	0.4	0	0.4	V	
Input Leakage Current	I _{LI}	0V ≤ V _I ≤ 6.5V ; All other pins not under test = 0V	-10	10	-10	10	μA	
Output Leakage Current	I _{LO}	DQ disable 0V ≤ V _O ≤ 5.5V	-10	10	-10	10	μA	
Average Power Supply Current (Operating)	I _{CC1}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling, t _{RC} = Min.	—	120	—	110	mA	1,2
Power Supply Current (Standby)	I _{CC2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ = V _{IH}	—	2	—	2	mA	1
		$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ ≥ V _{CC} - 0.2V	—	1	—	1	μA	1,5
			—	200	—	200	μA	
Average Power Supply Current ($\overline{\text{RAS}}$ -only Refresh)	I _{CC3}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ = V _{IH} , t _{RC} = Min.	—	120	—	110	mA	1,2
Power Supply Current (Standby)	I _{CC5}	$\overline{\text{RAS}}$ = V _{IH} , $\overline{\text{CAS}}$ = V _{IL} , DQ = enable	—	5	—	5	mA	1
Average Power Supply Current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	I _{CC6}	$\overline{\text{RAS}}$ = cycling, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$	—	120	—	110	mA	1,2
Average Power Supply Current (Fast Page Mode)	I _{CC7}	$\overline{\text{RAS}}$ = V _{IL} , $\overline{\text{CAS}}$ cycling, t _{PC} = Min.	—	110	—	100	mA	1,3
Average Power Supply Current (Battery Backup)	I _{CC10}	t _{RC} = 125μs, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$, t _{RAS} ≤ 1μs	—	300	—	300	μA	1,4,5
Average Power Supply Current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self-Refresh)	I _{CCS}	$\overline{\text{RAS}}$ ≤ 0.2V, $\overline{\text{CAS}}$ ≤ 0.2V	—	300	—	300	μA	1,5

- Notes: 1. I_{CC} Max. is specified as I_{CC} for output open condition.
 2. The address can be changed once or less while $\overline{\text{RAS}}$ = V_{IL}.
 3. The address can be changed once or less while $\overline{\text{CAS}}$ = V_{IH}.
 4. V_{CC} - 0.2V ≤ V_{IH} ≤ 6.5V, - 1.0V ≤ V_{IL} ≤ 0.2V.
 5. SL version.

AC Characteristic (1/2)

(V_{CC} = 5V ± 10%, Ta = 0°C to 70°C) Note1,2,3

Parameter	Symbol	MSM514800 D/DSL-60		MSM514800 D/DSL-70		Unit	Note
		Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t _{RC}	110	—	130	—	ns	
Read Modify Write Cycle Time	t _{RWC}	155	—	185	—	ns	
Fast Page Mode Cycle Time	t _{PC}	40	—	45	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t _{PRWC}	85	—	100	—	ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}	—	60	—	70	ns	4,5,6
Access Time from $\overline{\text{CAS}}$	t _{CAC}	—	20	—	20	ns	4,5
Access Time from Column Address	t _{AA}	—	30	—	35	ns	4,6
Access Time from $\overline{\text{CAS}}$ Precharge	t _{CPA}	—	35	—	40	ns	4
Access Time from $\overline{\text{OE}}$	t _{OEA}	—	20	—	20	ns	4
Output Low Impedance Time from $\overline{\text{CAS}}$	t _{CLZ}	0	—	0	—	ns	4
$\overline{\text{CAS}}$ to Data Output Buffer Turn-off Delay Time	t _{OFF}	0	15	0	20	ns	7
$\overline{\text{OE}}$ to Data Output Buffer Turn-off Delay Time	t _{OEZ}	0	15	0	20	ns	7
Transition Time	t _T	3	50	3	50	ns	3
Refresh Period	t _{REF}	—	16	—	16	ms	
Refresh Period	t _{REF}	—	128	—	128	ms	11
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	40	—	50	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	60	10,000	70	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RASP}	60	100,000	70	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	15	—	20	—	ns	
$\overline{\text{RAS}}$ Hold Time referenced to $\overline{\text{OE}}$	t _{ROH}	15	—	20	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t _{CP}	10	—	10	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	20	10,000	20	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	60	—	70	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	10	—	10	—	ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	35	—	40	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	20	40	20	50	ns	5
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	15	30	15	35	ns	6
Row Address Set-up Time	t _{ASR}	0	—	0	—	ns	
Row Address Hold Time	t _{RAH}	10	—	10	—	ns	

AC Characteristic (2/2)

(V_{CC} = 5V ± 10%, Ta = 0°C to 70°C) Note1,2,3

Parameter	Symbol	MSM514800 D/DSL-60		MSM514800 D/DSL-70		Unit	Note
		Min.	Max.	Min.	Max.		
Column Address Set-up Time	t _{ASC}	0	—	0	—	ns	
Column Address Hold Time	t _{CAH}	10	—	15	—	ns	
Column Address Hold Time from $\overline{\text{RAS}}$	t _{AR}	50	—	55	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t _{RAL}	30	—	35	—	ns	
Read Command Set-up Time	t _{RCS}	0	—	0	—	ns	
Read Command Hold Time	t _{RCH}	0	—	0	—	ns	8
Read Command Hold Time referenced to $\overline{\text{RAS}}$	t _{RRH}	0	—	0	—	ns	8
Write Command Set-up Time	t _{WCS}	0	—	0	—	ns	9
Write Command Hold Time	t _{WCH}	15	—	15	—	ns	
Write Command Hold Time from $\overline{\text{RAS}}$	t _{WCR}	50	—	55	—		
Write Command Pulse Width	t _{WP}	15	—	15	—	ns	
$\overline{\text{OE}}$ Command Hold Time	t _{OEH}	15	—	20	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t _{RWL}	15	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t _{CWL}	15	—	20	—	ns	
Data-in Set-up Time	t _{DS}	0	—	0	—	ns	10
Data-in Hold Time	t _{DH}	15	—	15	—	ns	10
Data-in Hold Time from $\overline{\text{RAS}}$	t _{DHR}	50	—	55	—		
$\overline{\text{OE}}$ to Data-in Delay Time	t _{OED}	15	—	20	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{CWD}	40	—	50	—	ns	9
Column Address to WE Delay Time	t _{AWD}	60	—	65	—	ns	9
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{RWD}	90	—	100	—	ns	9
$\overline{\text{CAS}}$ Precharge $\overline{\text{WE}}$ Delay Time	t _{CPWD}	65	—	70	—	ns	9
$\overline{\text{CAS}}$ Active Delay Time from $\overline{\text{RAS}}$ Precharge	t _{RPC}	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Set-up Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{CSR}	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{CHR}	15	—	15	—	ns	
$\overline{\text{RAS}}$ Pulse Width ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self-Refresh)	t _{RASS}	100	—	100	—	μs	11
$\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self-Refresh)	t _{RPS}	110	—	130	—	ns	11
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self-Refresh)	t _{CHS}	−40	—	−50	—	ns	11

- Notes:
1. A start-up delay of 200 μ s is required after power-up, followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh) before proper device operation is achieved.
 2. The AC characteristics assume $t_T = 5\text{ns}$.
 3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL} .
 4. This parameter is measured with a load circuit equivalent to 2 TTL load and 100pF.
 5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then the access time is controlled by t_{CAC} .
 6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then the access time is controlled by t_{AA} .
 7. t_{OFF} (Max.) and t_{OEZ} (Max.) define the time at which the output achieved the open circuit condition and are not referenced to output voltage levels.
 8. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 9. t_{WCS} , t_{CWD} , t_{RWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.), $t_{RWD} \geq t_{RWD}$ (Min.), $t_{AWD} \geq t_{AWD}$ (Min.) and $t_{CPWD} \geq t_{CPWD}$ (Min.), then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.
 10. These parameters are referenced to the $\overline{\text{CAS}}$, leading edges in an early write cycle, and to the $\overline{\text{WE}}$ leading edge in an $\overline{\text{OE}}$ control write cycle, or a read modify write cycle.
 11. SL version only.

The diagram illustrates the timing relationships for a Read Cycle. The signals and their timing parameters are as follows:

- RAS**: V_{IH} and V_{IL} levels. Timing parameters: t_{RAS} (high pulse width), t_{RP} (return to high after low pulse), t_{CRP} (return to high after low pulse).
- CAS**: V_{IH} and V_{IL} levels. Timing parameters: t_{RAD} (high pulse width), t_{RAL} (low pulse width), t_{CRP} (return to high after low pulse).
- Address**: V_{IH} and V_{IL} levels. Timing parameters: t_{ASR} (Row Address Strobe), t_{RAH} (Row Address Hold), t_{ASC} (Column Address Strobe), t_{CAH} (Column Address Hold).
- WE**: V_{IH} and V_{IL} levels. Timing parameters: t_{RCS} (Row Column Strobe), t_{AA} (Row Address Afterwrite), t_{ROH} (Row Output Hold), t_{RCH} (Row Column Hold).
- OE**: V_{IH} and V_{IL} levels. Timing parameters: t_{OEA} (Output Enable Afterwrite), t_{CAC} (Output Column Address Strobe), t_{RAC} (Row Address Strobe), t_{CLZ} (Output Column Address Strobe), t_{RRH} (Row Address Hold), t_{RCH} (Row Column Hold), t_{OEZ} (Output Enable Z), t_{OFF} (Output Off).
- DQ**: V_{OH} and V_{OL} levels. Timing parameters: t_{CLZ} (Output Column Address Strobe), t_{RAC} (Row Address Strobe), t_{CAC} (Output Column Address Strobe), t_{RRH} (Row Address Hold), t_{RCH} (Row Column Hold), t_{OEZ} (Output Enable Z), t_{OFF} (Output Off).

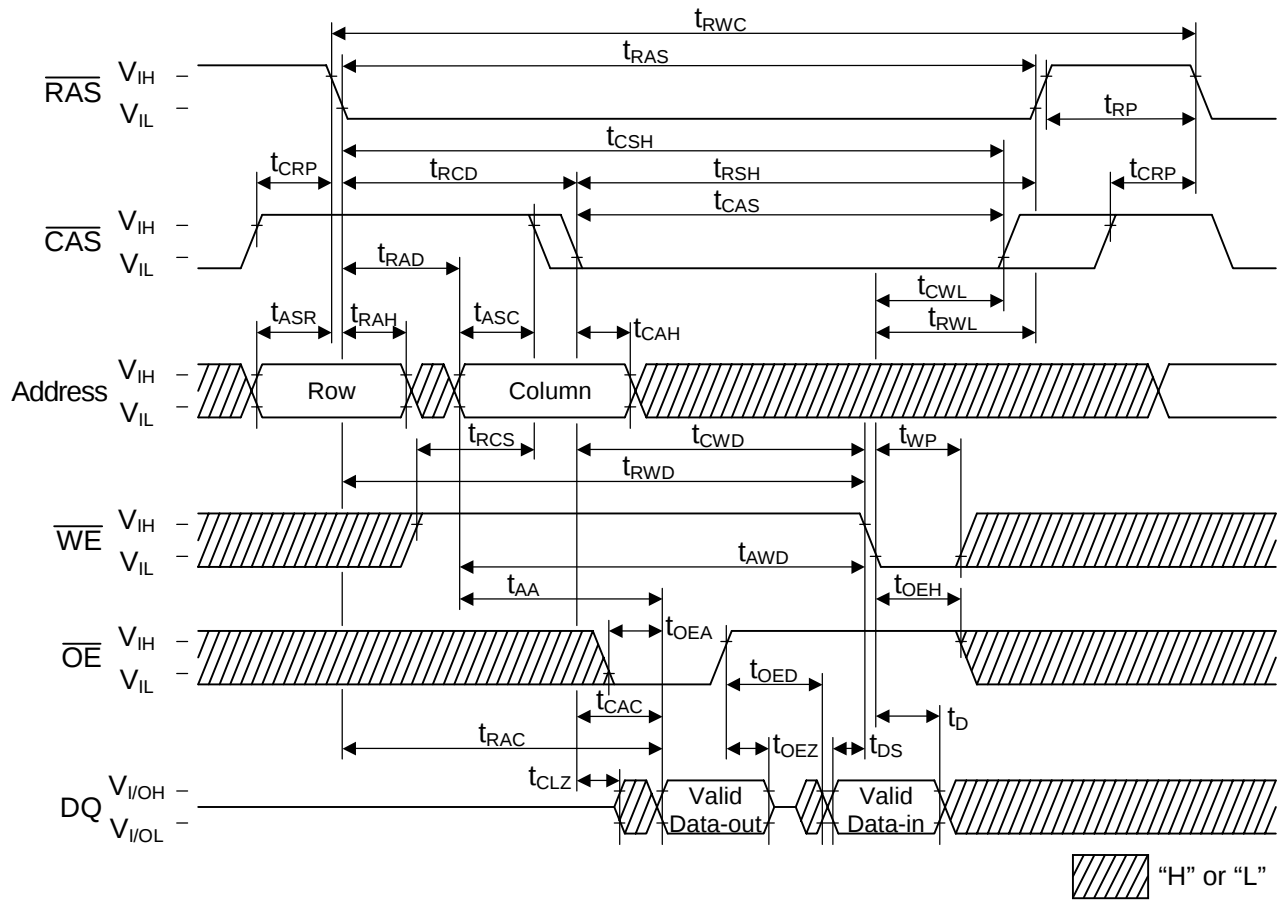
The diagram also shows the "Valid Data-out" period and the "H" or "L" levels for the signals.

Write Cycle (Early write)

The diagram illustrates the timing relationships for a write cycle. The signals and their timing parameters are as follows:

- RAS:** t_{RAS} (RAS to data-in), t_{RC} (RAS to next RAS), t_{RP} (RAS precharge), t_{CRP} (RAS to CAS precharge).
- CAS:** t_{CSD} (CAS to data-in), t_{RSH} (RAS to CAS), t_{CAS} (CAS to data-in), t_{RAD} (RAS to data-in), t_{RAL} (RAS to data-in).
- Address:** t_{ASR} (Address strobe to row), t_{RAH} (Row address hold), t_{ASC} (Address strobe to column), t_{CAH} (Column address hold), t_{CWL} (Column write latency).
- WE:** t_{WCS} (Write enable to column strobe), t_{WCH} (Write enable to column hold), t_{WPL} (Write enable precharge), t_{RWL} (Row write latency).
- OE:** t_{DS} (Data strobe to data-in), t_{DH} (Data hold).
- DQ:** Valid Data-in (during write), Open (after write).

- Read Modify Write Cycle



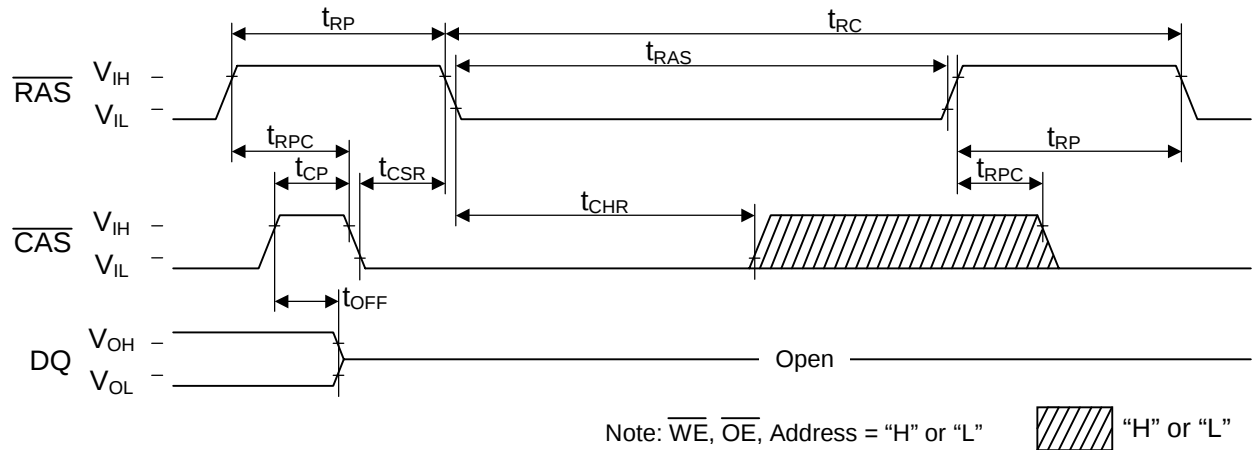


The diagram illustrates the timing relationships for a memory access. The signals shown are $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, Address, and DQ. The voltage levels for $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and DQ are indicated as V_{IH} (high) and V_{IL} (low). The Address signal is shown with a shaded region labeled "Row" and a shaded region labeled "t_{OFF}". The DQ signal is shown with a shaded region labeled "t_{OH}" and a shaded region labeled "Open". The timing parameters are defined as follows:

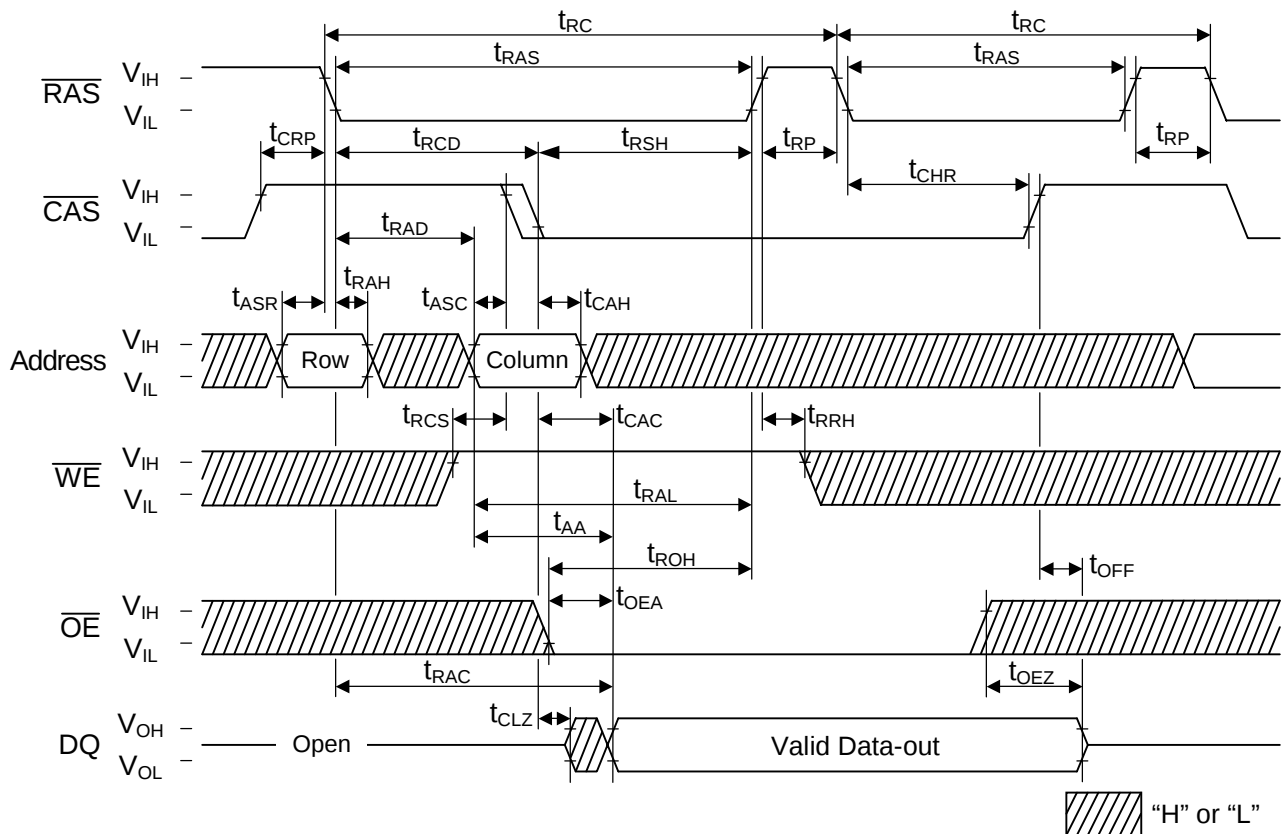
- t_{CRP} : RAS to CAS precharge time.
- t_{RPC} : RAS to CAS precharge time (recovery).
- t_{RAS} : RAS access time.
- t_{RC} : RAS to CAS delay.
- t_{RP} : RAS precharge time.
- t_{ASR} : Address setup time.
- t_{RAH} : Address recovery time.
- t_{OFF} : Address off-time.
- t_{OH} : Output hold time.

12/14

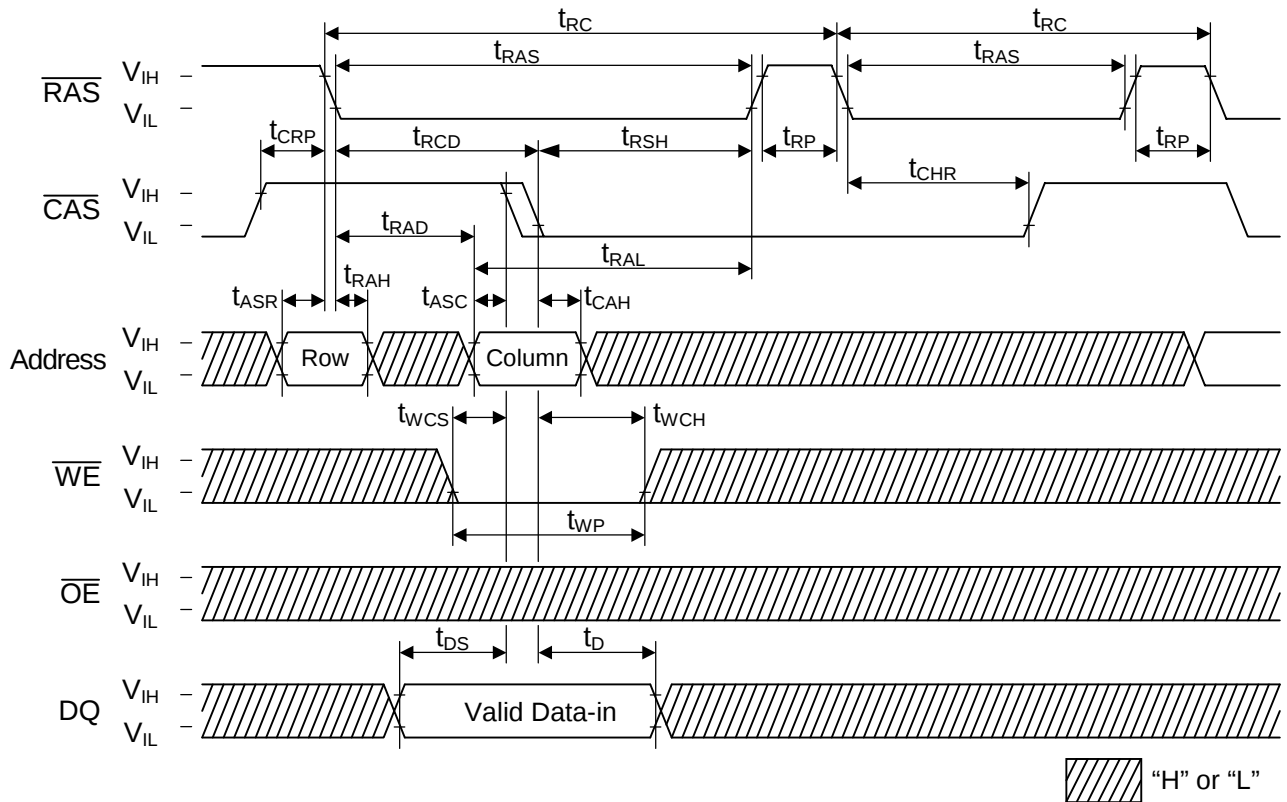
- CAS before RAS Refresh Cycle



- Hidden Refresh Read Cycle



Hidden Refresh Write Cycle



CAS before RAS Self-Refresh Cycle

