300-mA, Low-I_Q, Low-Dropout Regulator

FEATURES

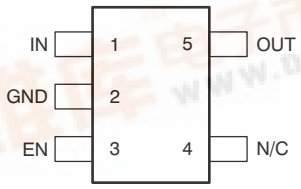
- **Very Low Dropout:**
  - **37 mV at I_{OUT} = 50 mA, V_{OUT} = 2.8 V**
  - **75 mV at I_{OUT} = 100 mA, V_{OUT} = 2.8 V**
  - **220mV at I_{OUT} = 300 mA, V_{OUT} = 2.8 V**
- **2% Accuracy**
- **Low I_Q: 35 μA**
- **Fixed-Output Voltage Combinations Possible from 1.2 V to 4.8 V**
- **High PSRR: 68 dB at 1 kHz**
- **Stable with Effective Capacitance of 0.1 μF(1)**
- **Thermal Shutdown and Overcurrent Protection**
- **Package: SOT23-5**

(1) See the *Input and Output Capacitor Requirements* in the Application Information section.

APPLICATIONS

- **Wireless Handsets**
- **Smart Phones, PDAs**
- **MP3 Players**
- **ZigBee® Networks**
- **Bluetooth® Devices**
- **Li-Ion Operated Handheld Products**
- **WLAN and Other PC Add-on Cards**

TLV702xxDBV
SOT23-5
(TOP VIEW)



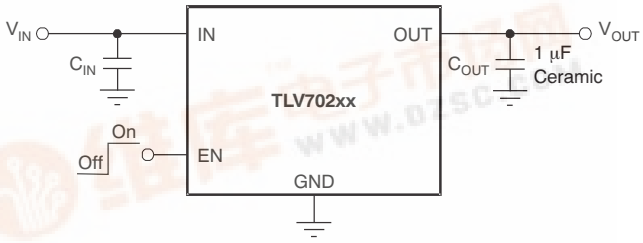
DESCRIPTION

The TLV702xx series of low-dropout (LDO) linear regulators are low quiescent current devices with excellent line and load transient performance. These LDOs are designed for power-sensitive applications. A precision bandgap and error amplifier provides overall 2% accuracy. Low output noise, very high power-supply rejection ratio (PSRR), and low-dropout voltage make this series of devices ideal for a wide selection of battery-operated handheld equipment. All device versions have thermal shutdown and current limit for safety.

Furthermore, these devices are stable with an effective output capacitance of only 0.1 μF. This feature enables the use of cost-effective capacitors that have higher bias voltages and temperature derating. The devices regulate to specified accuracy with no output load.

The TLV702xxP series also provides an active pulldown circuit to quickly discharge the outputs.

The TLV702xx series of LDO linear regulators are available in a SOT23-5 package.



Typical Application Circuit
(Fixed-Voltage Versions)

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT} (2)
TLV702**xx(x)***Pyyyz*	**XX(X)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 475 = 4.75 V). **P** is optional; devices with P have an LDO regulator with an active output discharge. **YYY** is the package designator. **Z** is package quantity. Use "R" for reel (3000 pieces), and "T" for tape (250 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
(2) Output voltages from 1.2 V to 4.8 V in 50-mV increments are available. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE		UNIT
		MIN	MAX	
Voltage(2)	IN	–0.3	+6.0	V
	EN	–0.3	+6.0	V
	OUT	–0.3	+6.0	V
Current (source)	OUT	Internally Limited		
Output short-circuit duration		Indefinite		
Temperature	Operating virtual junction, T_J	–55	+150	°C
	Storage, T_{stg}	–55	+150	°C
Electrostatic Discharge Rating(3)	Human Body Model (HBM) QSS 009-105 (JESD22-A114A)		2	kV
	Charge Device Model (CDM) QSS 009-147 (JESD22-C101B.01)		500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

DISSIPATION RATINGS(1)

PACKAGE	$R_{\theta JA}$	T_A < +25°C	T_A = +70°C	T_A = +85°C
DBV	200°C/W	500mW	275mW	200mW

(1) For board details, see the *Thermal Information* section.

ELECTRICAL CHARACTERISTICS

At V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.0 V (whichever is greater); I_{OUT} = 10 mA, V_{EN} = 0.9 V, C_{OUT} = 1.0 µF, and T_J = –40°C to +125°C, unless otherwise noted. Typical values are at T_J = +25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		2.0		5.5	V
V_{OUT}	DC output accuracy	–40°C ≤ T_J ≤ +125°C	–2	0.5	+2	%
$\Delta V_O/\Delta V_{IN}$	Line regulation	$V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 10 mA		1	5	mV
$\Delta V_O/\Delta I_{OUT}$	Load regulation	0 mA ≤ I_{OUT} ≤ 300 mA		1	15	mV
V_{DO}	Dropout voltage(1)	V_{IN} = 0.98 × $V_{OUT(NOM)}$, I_{OUT} = 50 mA, V_{OUT} = 2.8 V		37		mV
		V_{IN} = 0.98 × $V_{OUT(NOM)}$, I_{OUT} = 100 mA, V_{OUT} = 2.8 V		75		mV
		V_{IN} = 0.98 × $V_{OUT(NOM)}$, I_{OUT} = 300 mA, V_{OUT} = 2.35 V		260	375	mV
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(NOM)}$	320	500	860	mA
I_{GND}	Ground pin current	I_{OUT} = 0 mA		35	55	µA
		I_{OUT} = 300 mA, V_{IN} = V_{OUT} + 0.5 V		370		µA
I_{SHDN}	Ground pin current (shutdown)	V_{EN} ≤ 0.4 V, V_{IN} = 2.0 V		400		nA
		V_{EN} ≤ 0.4 V, 2.0 V ≤ V_{IN} ≤ 4.5 V, T_J = –40°C to +85°C		1	2	µA
PSRR	Power-supply rejection ratio	V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA, f = 1 kHz		68		dB
V_N	Output noise voltage	BW = 100 Hz to 100 kHz, V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA		48		μV_{RMS}
t_{STR}	Startup time(2)	C_{OUT} = 1.0 µF, I_{OUT} = 300 mA		100		µs
$V_{EN(HI)}$	Enable pin high (enabled)		0.9		V_{IN}	V
$V_{EN(LO)}$	Enable pin low (disabled)		0		0.4	V
I_{EN}	Enable pin current	V_{IN} = V_{EN} = 5.5 V		0.04		µA
UVLO	Undervoltage lockout	V_{IN} rising		1.9		V
$R_{DISCHARGE}$	Active pulldown resistance (TLV702xxP only)	V_{EN} = 0 V		120		Ω
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		+165		°C
		Reset, temperature decreasing		+145		°C
T_J	Operating junction temperature		–40		+125	°C

(1) V_{DO} is measured for devices with $V_{OUT(NOM)}$ ≥ 2.35 V.
(2) Startup time = time from EN assertion to 0.98 × $V_{OUT(NOM)}$.

FUNCTIONAL BLOCK DIAGRAMS

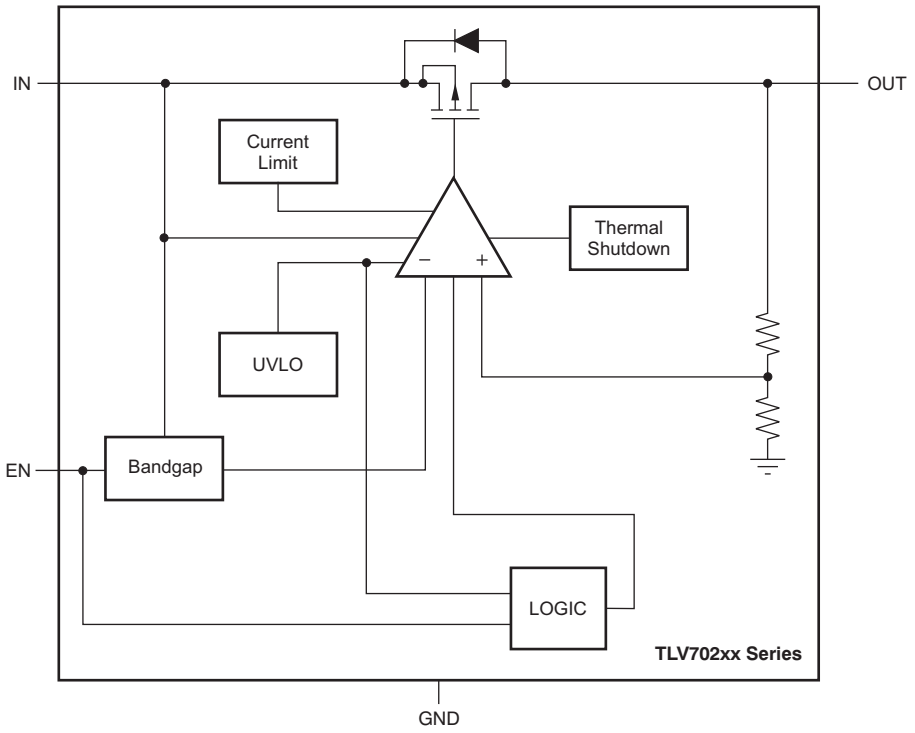


Figure 1. TLV702xx

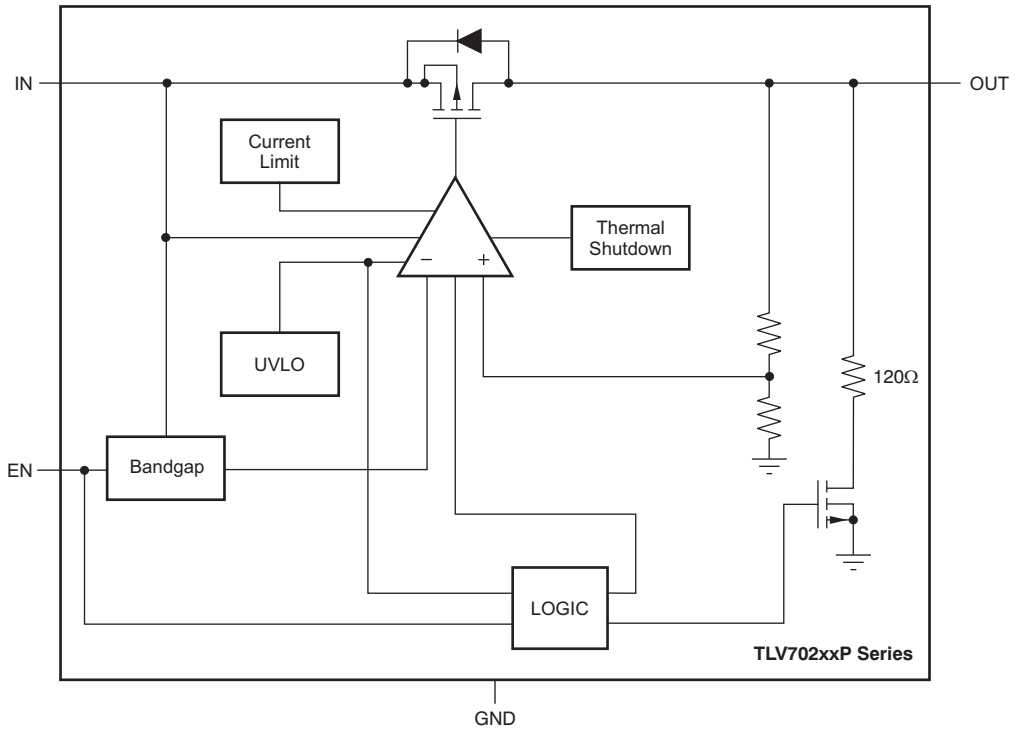
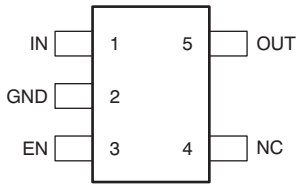


Figure 2. TLV702xxP

PIN CONFIGURATIONS

DBV PACKAGE
SOT23-5
(TOP VIEW)



PIN DESCRIPTIONS

NAME	SOT23-5 DBV	DESCRIPTION
IN	1	Input pin. A small 1-μF ceramic capacitor is recommended from this pin to ground to assure stability and good transient performance. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.
GND	2	Ground pin
EN	3	Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode and reduces operating current to 1 μA, nominal. For TLV702xxP, output voltage is discharged through an internal 120-Ω resistor when device is shut down.
NC	4	No connection. This pin can be tied to ground to improve thermal dissipation.
OUT	5	Regulated output voltage pin. A small 1-μF ceramic capacitor is needed from this pin to ground to assure stability. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.

TYPICAL CHARACTERISTICS

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.0 V, whichever is greater; I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1.0 µF, unless otherwise noted. Typical values are at T_J = +25°C.

LINE REGULATION

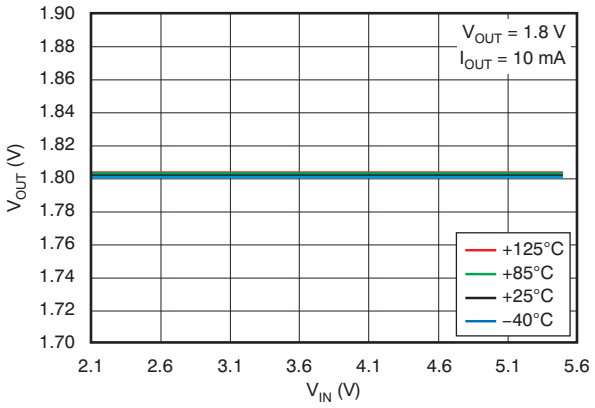


Figure 3.

LINE REGULATION

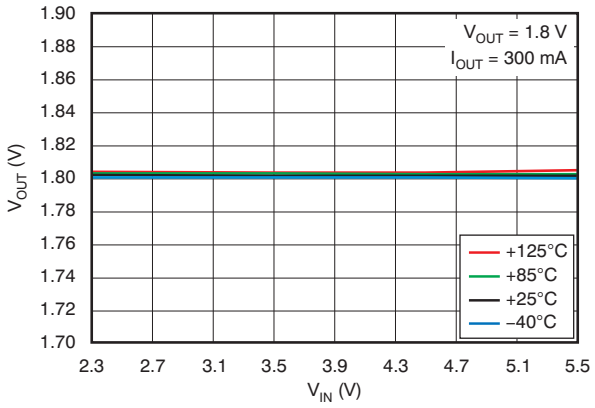


Figure 4.

LOAD REGULATION

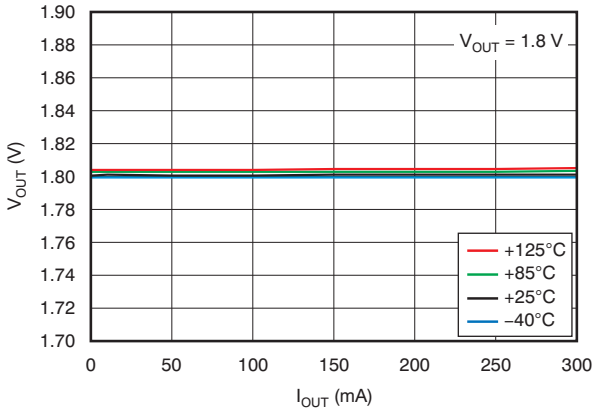


Figure 5.

DROPOUT VOLTAGE vs INPUT VOLTAGE

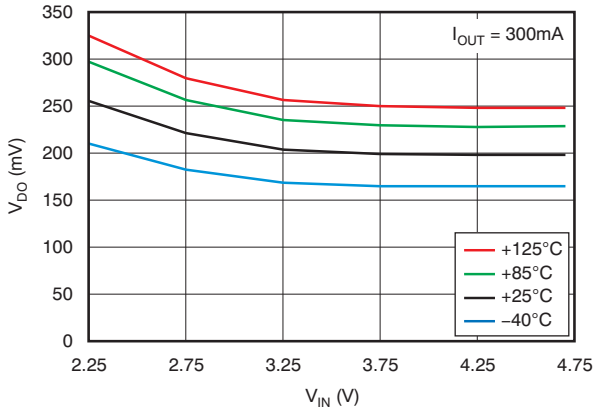


Figure 6.

DROPOUT VOLTAGE vs OUTPUT CURRENT

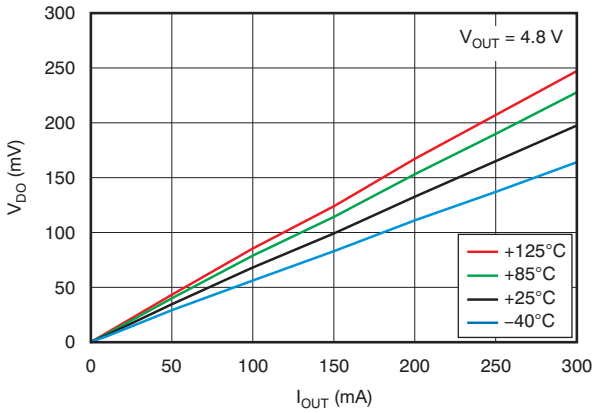


Figure 7.

OUTPUT VOLTAGE vs TEMPERATURE

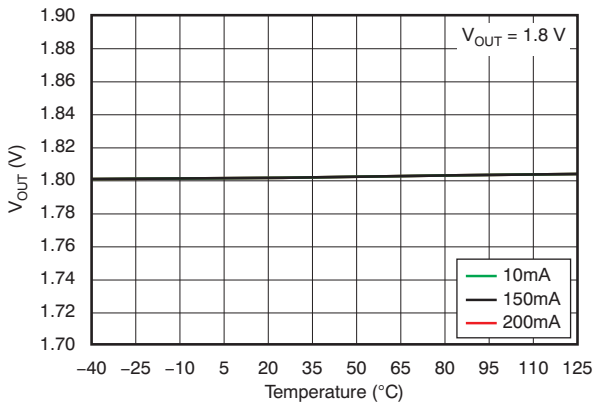


Figure 8.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.0 V, whichever is greater; I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1.0 µF, unless otherwise noted. Typical values are at T_J = +25°C.

GROUND PIN CURRENT vs INPUT VOLTAGE

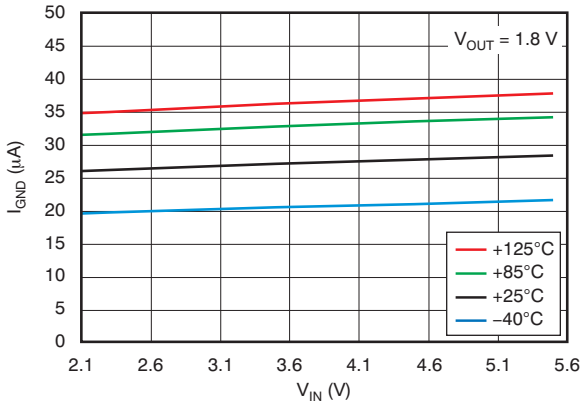


Figure 9.

GROUND PIN CURRENT vs LOAD

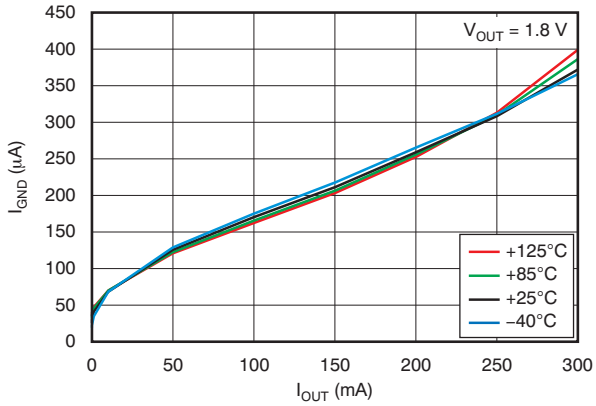


Figure 10.

GROUND PIN CURRENT vs TEMPERATURE

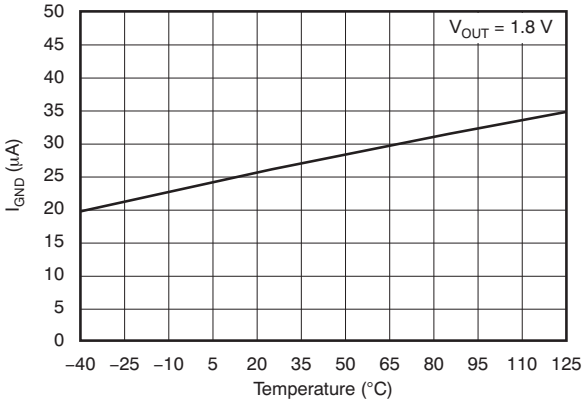


Figure 11.

SHUTDOWN CURRENT vs INPUT VOLTAGE

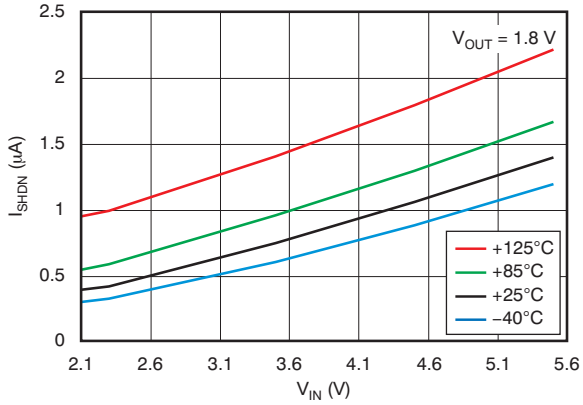


Figure 12.

CURRENT LIMIT vs INPUT VOLTAGE

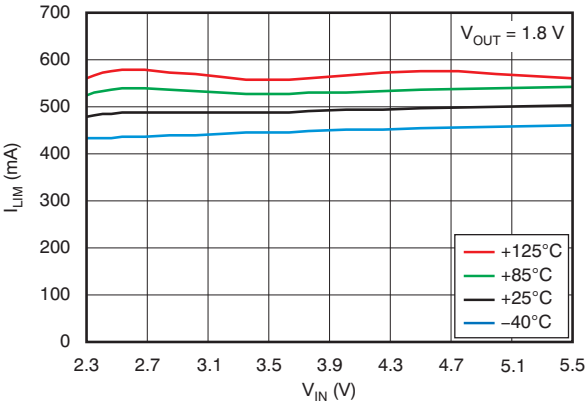


Figure 13.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY

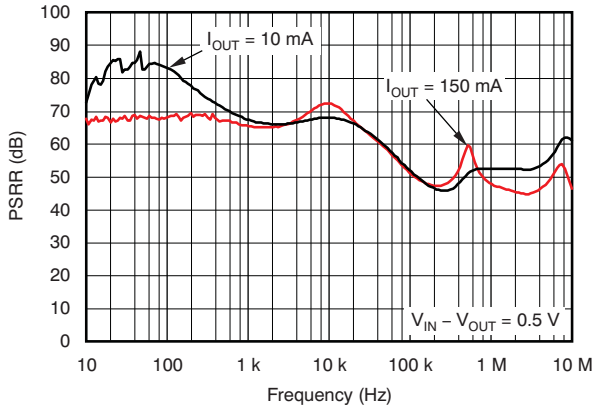


Figure 14.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.0 V, whichever is greater; I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1.0 µF, unless otherwise noted. Typical values are at T_J = +25°C.

POWER-SUPPLY RIPPLE REJECTION vs INPUT VOLTAGE

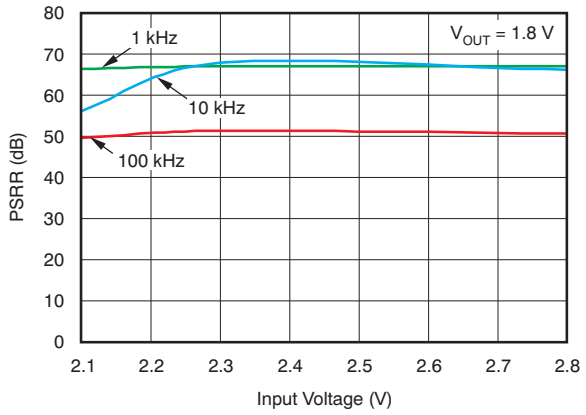


Figure 15.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

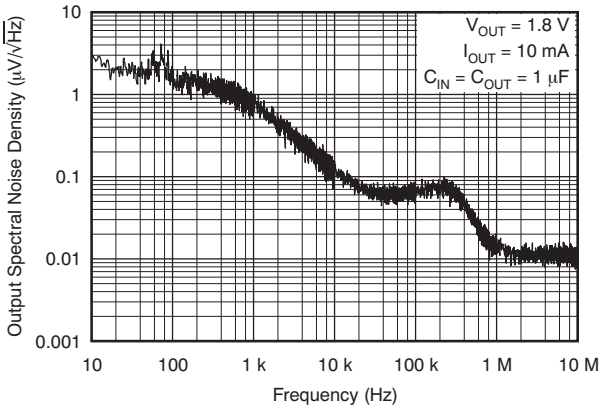


Figure 16.

LOAD TRANSIENT RESPONSE

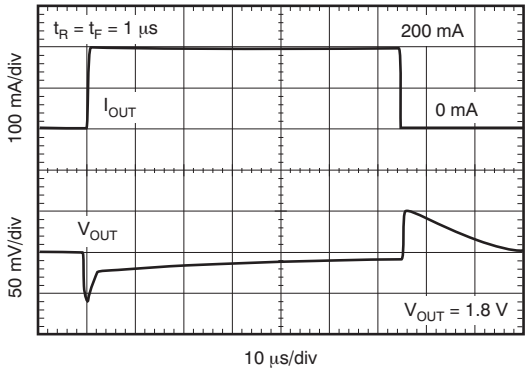


Figure 17.

LOAD TRANSIENT RESPONSE

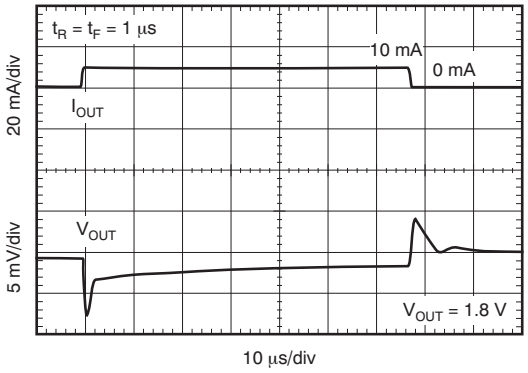


Figure 18.

LOAD TRANSIENT RESPONSE

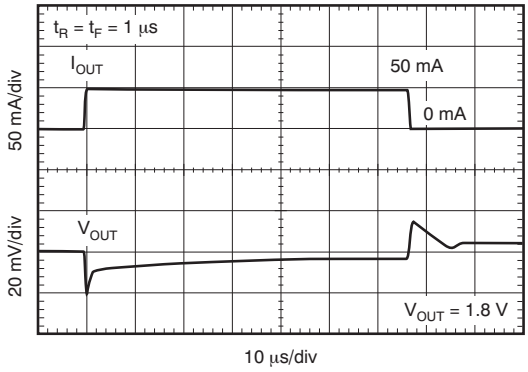


Figure 19.

LOAD TRANSIENT RESPONSE

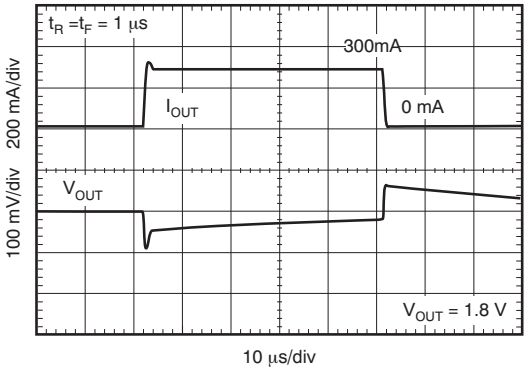


Figure 20.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.0 V, whichever is greater; I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1.0 µF, unless otherwise noted. Typical values are at T_J = +25°C.

LINE TRANSIENT RESPONSE

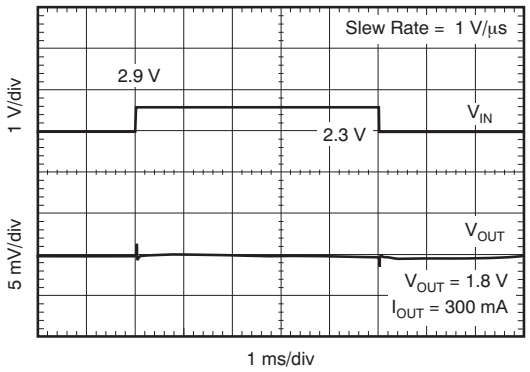


Figure 21.

LINE TRANSIENT RESPONSE

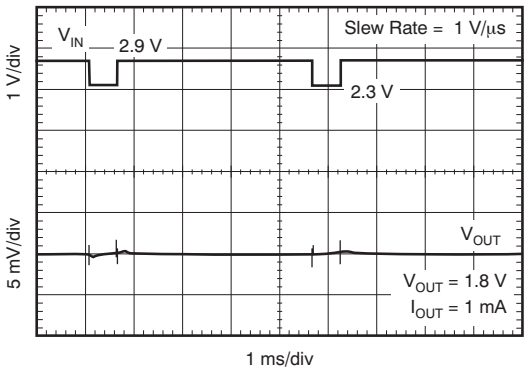


Figure 22.

LINE TRANSIENT RESPONSE

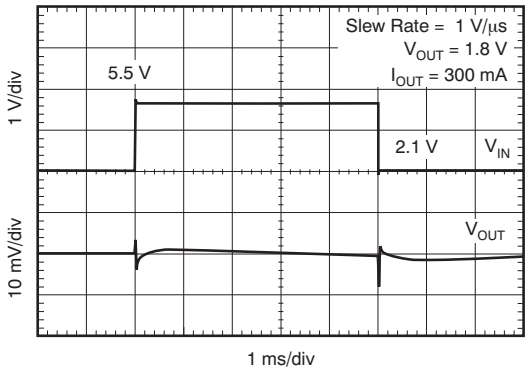


Figure 23.

V_{IN} RAMP UP, RAMP DOWN RESPONSE

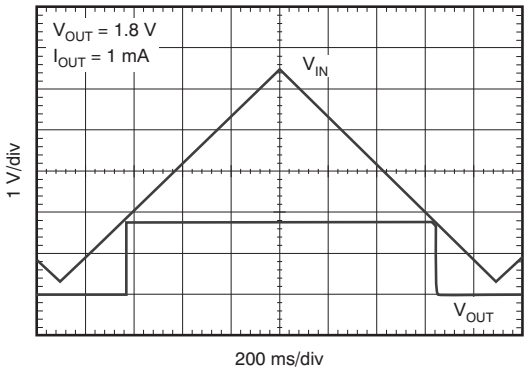


Figure 24.

APPLICATION INFORMATION

The TLV702xx belongs to a new family of next-generation value LDO regulators. These devices consume low quiescent current and deliver excellent line and load transient performance. These characteristics, combined with low noise and very good PSRR with little (V_{IN} – V_{OUT}) headroom, make this family of devices ideal for portable RF applications. This family of regulators offers current limit and thermal protection, and is specified from –40°C to +125°C.

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

1.0-μF X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

However, the TLV702xx is designed to be stable with an *effective capacitance* of 0.1 μF or larger at the output. Thus, the device is stable with capacitors of other dielectric types as well, as long as the effective capacitance under operating bias voltage and temperature is greater than 0.1 μF. This effective capacitance refers to the capacitance that the LDO sees under operating bias voltage and temperature conditions; that is, the capacitance after taking both bias voltage and temperature derating into consideration. In addition to allowing the use of lower-cost dielectrics, this capability of being stable with 0.1-μF effective capacitance also enables the use of smaller footprint capacitors that have higher derating in size- and space-constrained applications.

NOTE: Using a 0.1-μF rated capacitor at the output of the LDO does not ensure stability because the effective capacitance under the specified operating conditions would be less than 0.1 μF. Maximum ESR should be less than 200 mΩ.

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-μF to 1.0-μF, low ESR capacitor across the IN pin and GND pin of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source. If source impedance is more than 2 Ω, a 0.1-μF input capacitor may be necessary to ensure stability.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

Input and output capacitors should be placed as close to the device pins as possible. To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should be connected directly to the GND pin of the device. High ESR capacitors may degrade PSRR performance.

INTERNAL CURRENT LIMIT

The TLV702xx internal current limit helps to protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of the output voltage. In such a case, the output voltage is not regulated, and is $V_{OUT} = I_{LIMIT} \times R_{LOAD}$. The PMOS pass transistor dissipates (V_{IN} – V_{OUT}) × I_{LIMIT} until thermal shutdown is triggered and the device turns off. As the device cools, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown. See the *Thermal Information* section for more details.

The PMOS pass element in the TLV702xx has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

SHUTDOWN

The enable pin (EN) is active high. The device is enabled when voltage at EN pin goes above 0.9V. This relatively lower value of voltage required to turn the LDO on can be exploited to power the LDO with a GPIO of recent processors whose GPIO Logic 1 voltage level is lower than traditional microcontrollers. The device is turned off when the EN pin is held at less than 0.4V. When shutdown capability is not required, EN can be connected to the IN pin.

The TLV702xxP version has internal active pull-down circuitry that discharges the output with a time constant of:

$$\tau = \frac{(120 \bullet R_L)}{(120 + R_L)} \bullet C_{OUT} \quad (1)$$

where:

- R_L = Load resistance
- C_{OUT} = Output capacitor

DROPOUT VOLTAGE

The TLV702xx uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves as a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout. This effect is shown in Figure 15 in the Typical Characteristics section.

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over-/undershoot magnitude but increases the duration of the transient response.

UNDERVOLTAGE LOCKOUT (UVLO)

The TLV702xx uses an undervoltage lockout circuit to keep the output shut off until internal circuitry is operating properly.

THERMAL INFORMATION

Thermal protection disables the output when the junction temperature rises to approximately +165°C, allowing the device to cool. When the junction temperature cools to approximately +145°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum.

To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The internal protection circuitry of the TLV702xx has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TLV702xx into thermal shutdown degrades device reliability.

POWER DISSIPATION

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air.

Thermal performance data for TLV702xx were gathered using the TLV700 evaluation module (EVM), a 2-layer board with two ounces of copper per side. The dimensions and layout for this EVM are shown in Figure 25 and Figure 26. Corresponding thermal performance data are given in Table 1. Note that this board has provision for soldering not only the SOT23-5 package on the bottom layer, but also the SC-70 package on the top layer. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element, as shown in Equation 2.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

PACKAGE MOUNTING

Solder pad footprint recommendations for the TLV702xx are available from the Texas Instruments web site at www.ti.com. The recommended land pattern for the DBV package is shown in Figure 27.

Table 1. EVM Dissipation Ratings

PACKAGE	$R_{\theta JA}$	T_A < +25°C	T_A = +70°C	T_A = +85°C
DBV	200°C/W	500mW	275mW	200mW

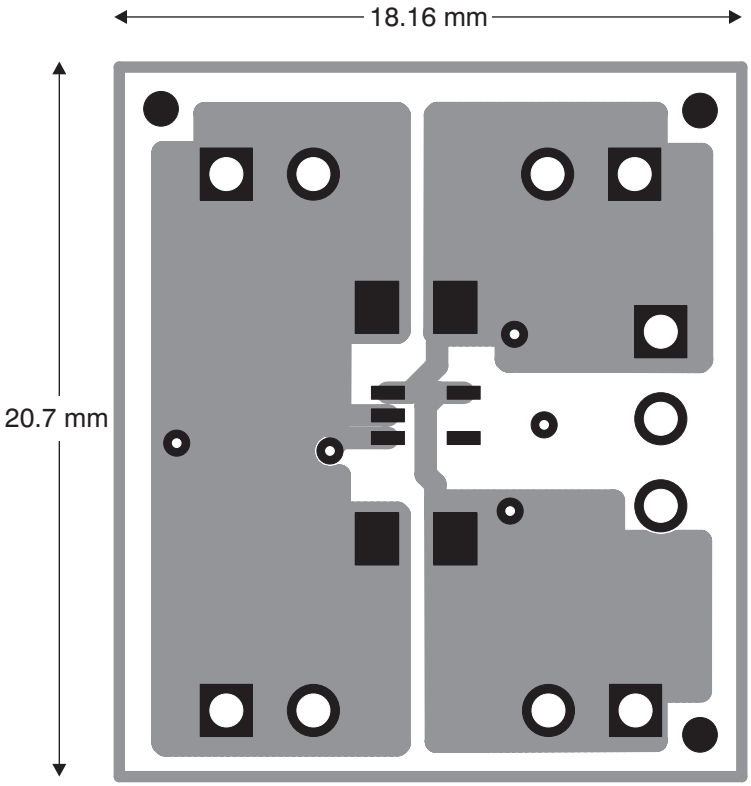


Figure 25. HPA503 EVM Top Layer

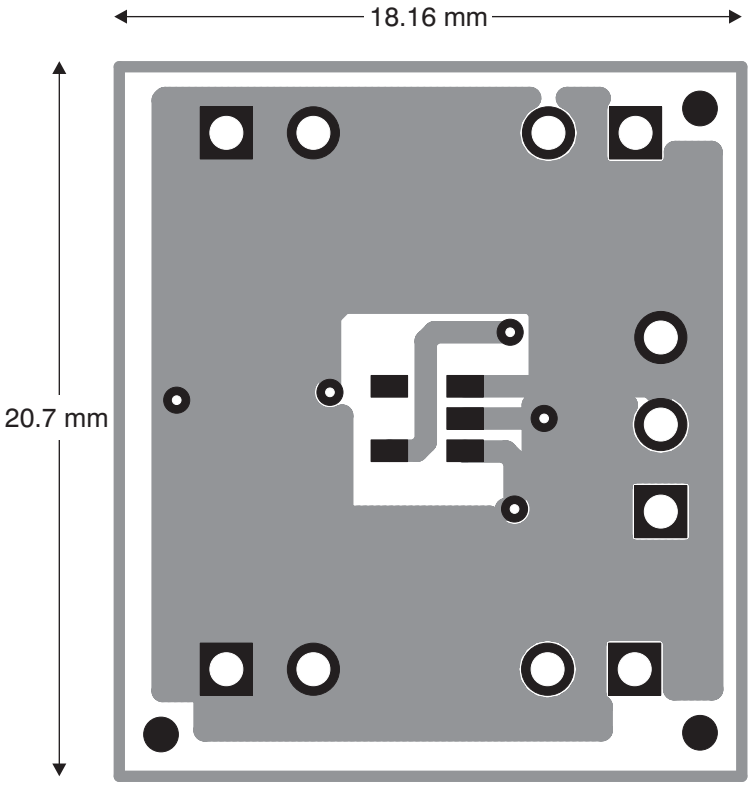
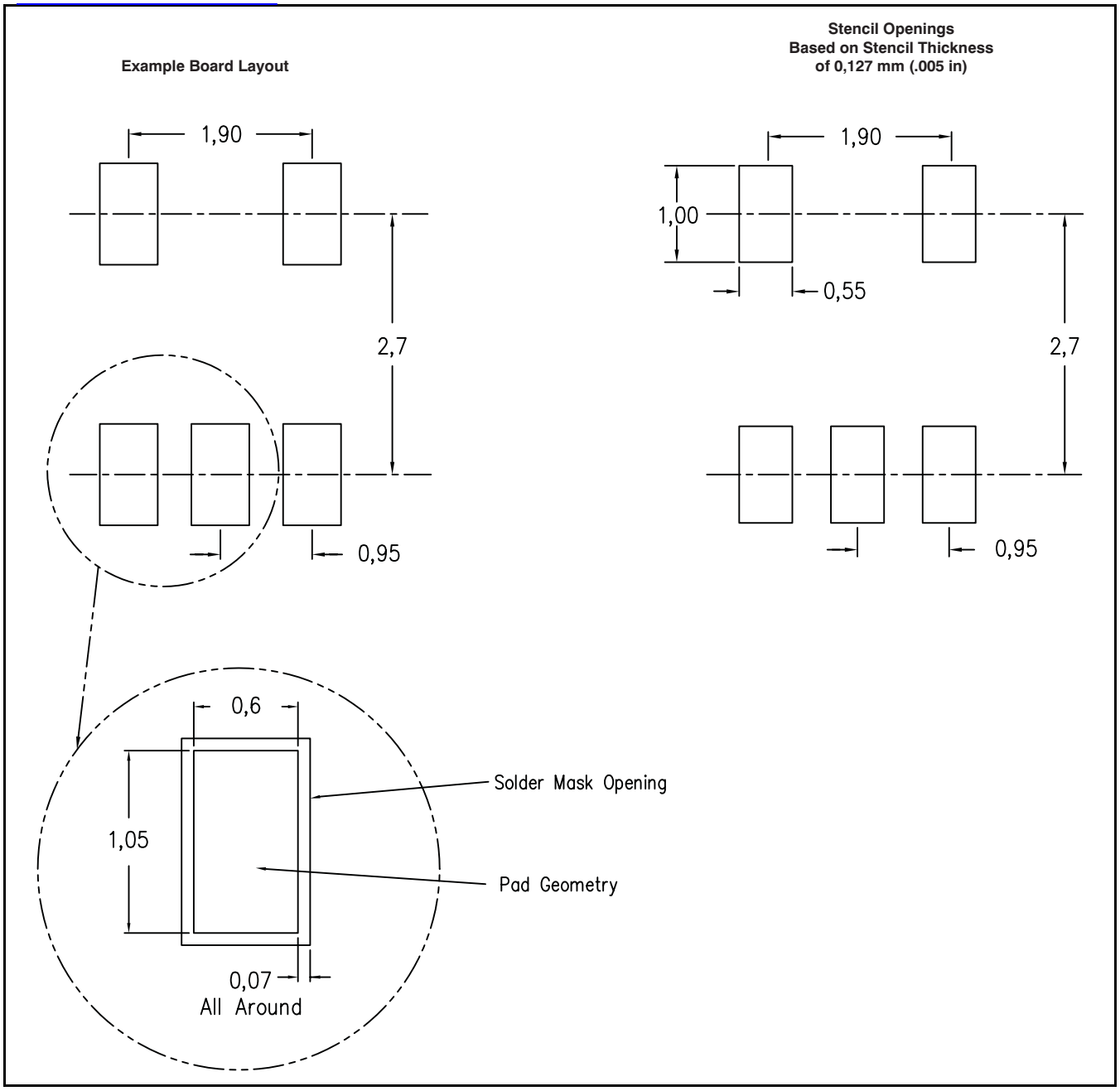


Figure 26. HPA503 EVM Bottom Layer



(1) All linear dimensions are in millimeters.

(2) Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.

(3) Publication IPC-7351 is recommended for alternate designs.

(4) Laser-cutting apertures with trapedzoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric load solder paste. Refer to IPC-7525 for other stencil recommendations.

Figure 27. Recommended Land Pattern for DBV Package

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2010) to Revision A	Page
• Updated ordering number in *Ordering Information* table	2

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Pea
TLV70212DBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI
TLV70212DBVT	PREVIEW	SOT-23	DBV	5	250	TBD	Call TI	Call TI
TLV70218DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV70218DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV70225DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV70225DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV70228DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV70228DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV70228PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV70228PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV70230DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV70230DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV70231DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV70231DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV70233DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
TLV70233DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

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NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.
information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all
lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable fo
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package,
the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retard
in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical an
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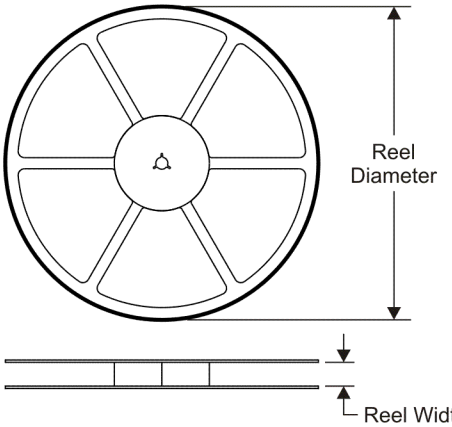
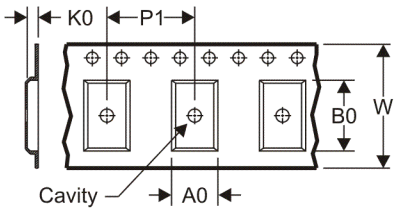
TAPE AND REEL INFORMATION

REEL DIMENSIONS

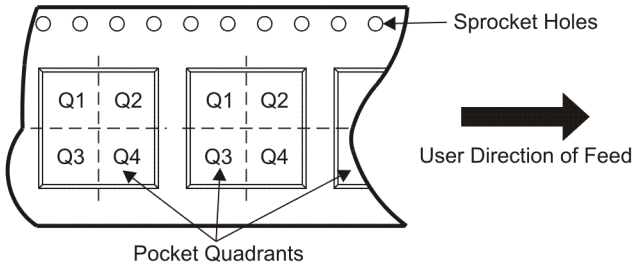


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

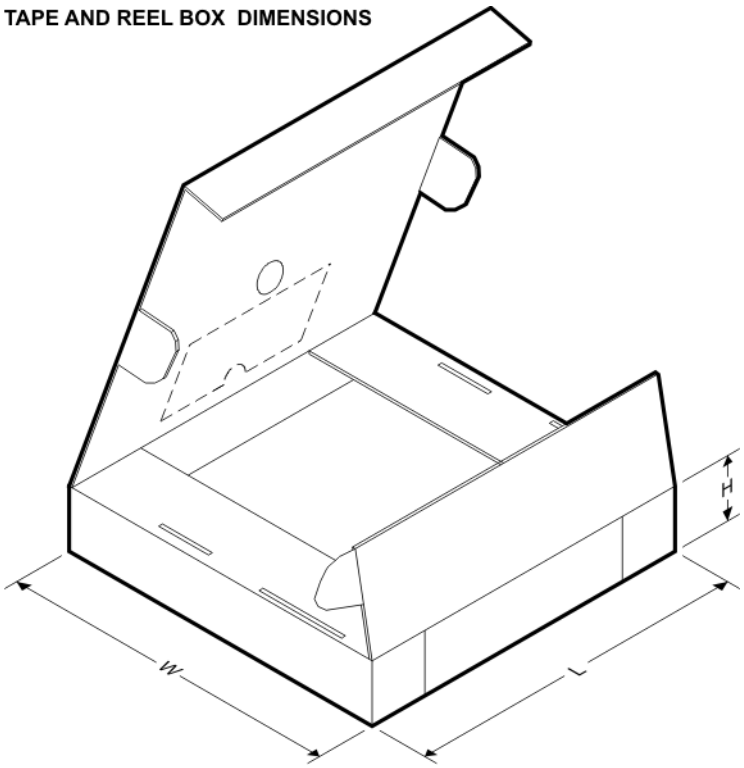
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV70218DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70225DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70225DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70228DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70228DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70228PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70228PDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70230DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70230DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70231DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70231DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70233DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70233DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3

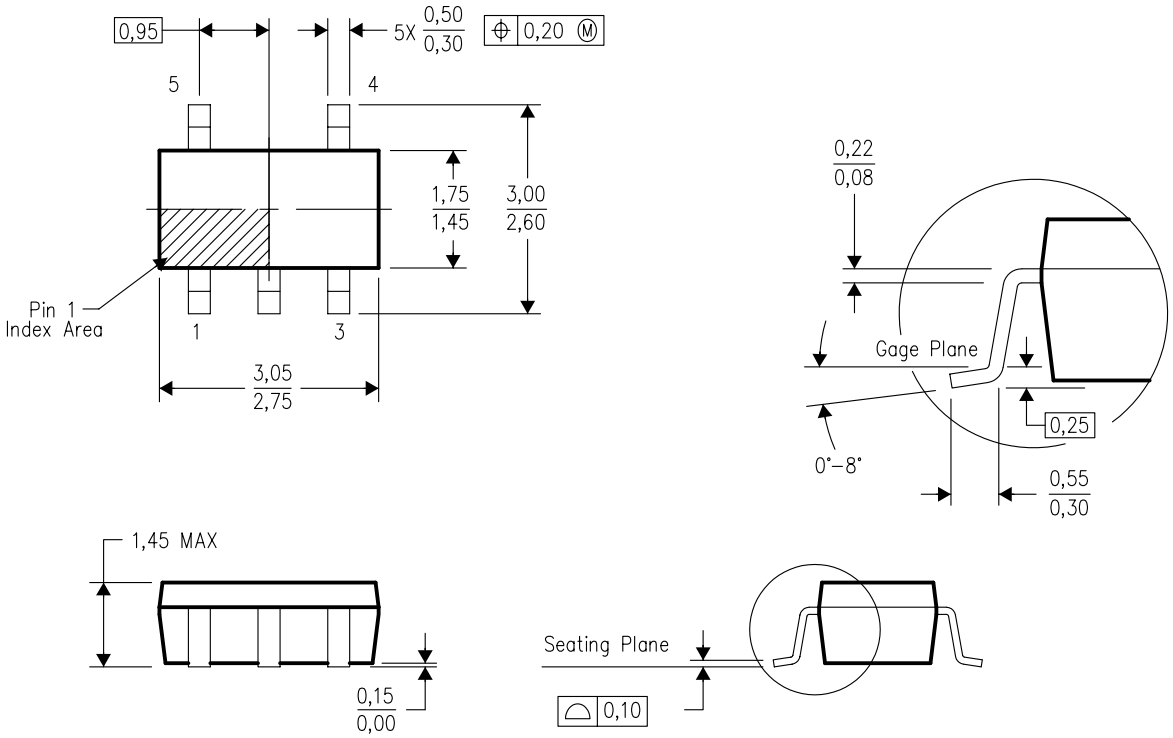
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV70218DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
TLV70225DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
TLV70225DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
TLV70228DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
TLV70228DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
TLV70228PDBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
TLV70228PDBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
TLV70230DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
TLV70230DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
TLV70231DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
TLV70231DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
TLV70233DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
TLV70233DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0

DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

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