128Mb (2Mx4Bankx16) Synchronous DRAM

Feature

- Fully synchronous to positive clock edge
- Single 3.3V +/- 0.3V power supply
- LVTTL compatible with multiplexed address
- Programmable Burst Length (B/ L) - 1,2,4, 8 or full page
- Programmable CAS Latency (C/ L) - 2 or 3
- Data Mask (DQM) for Read / Write masking
- Programmable wrap sequence
  - Sequential (B/ L = 1/2/4/8/full page)
  - Interleave (B/ L = 1/2/4/8)
- Burst read with single-bit write operation
- All inputs are sampled at the rising edge of the system clock.
- Auto refresh and self refresh
- 4,096 refresh cycles / 64ms (15.625us)

Description

The EM488M1644VTD is Synchronous Dynamic Random Access Memory (SDRAM) organized as 2Meg words x 4 banks x 16 bits.All inputs and outputs are synchronized with the positive edge of the clock.

The 128Mb SDRAM uses synchronized pipelined architecture to achieve high speed data transfer rates and is designed to operate at 3.3V low power memory system. It also provides auto refresh with power saving / down mode. All inputs and outputs voltage levels are compatible with LVTTL.

Packages: TSOPII 54P 400mil

Ordering Information

Part No	Organization	Max. Freq	Package	Power	Pb
EM488M1644VTD –75F	8M X16	133MHz @CL3	54pin TSOP (II)	Commercial	Free
EM488M1644VTD –7F	8M X16	143MHz @CL3	54pin TSOP (II)	Commercial	Free

Absolute Maximum Ratings

Symbol	Item	Rating	Units
V_{IN}, V_{OUT}	Input, Output Voltage	-0.3 ~ 4.6	V
V_{DD}, V_{DDQ}	Power Supply Voltage	-0.3 ~ 4.6	V
T_{OP}	Operating Temperature	0 ~ 70	°C
T_{STG}	Storage Temperature	-55 ~ 125	°C
P_D	Power Dissipation	1	W
I_{OS}	Short Circuit Current	50	mA

Note: Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended DC Operation Conditions (Ta = 0 ~ 70 °C)

Symbol	Parameter	Min.	Typical	Typical	Units
V_{DD}	Power Supply Voltage	3.0	3.3	3.6	V
V_{DDQ}	Power Supply Voltage (for I/O Buffer)	3.0	3.3	3.6	V
V_{IH}	Input logic high voltage	2.0		V_{DD}+0.3	V
V_{IL}	Input logic low voltage	-0.3		0.8	V

Note : 1. All voltage referred to VSS.

2. V_{IH} (max) = 5.6V for pulse width ≤3ns

3. V_{IL} (min) = -2.0V for pulse width ≤ 3ns

Capacitance (Vcc =3.3V, f = 1MHz, Ta = 25°C)

Symbol	Parameter	Min.	Max.	Units
C_{CLK}	Clock capacitance	2.5	3.5	pF
C_I	Input capacitance for CLK, CKE, Address, /CS, /RAS, /CAS, /WE, DQML, DQMU	2.5	3.8	pF
C_O	Input/Output capacitance	4.0	6.5	pF

Recommended DC Operating Conditions

(VDD = 3.3V +/- 0.3 V, Ta = 0 ~ 70 °C)

Parameter	Symbol	Test condition	MAX	Units	Notes
				mA	
Operating current	I_{CC1}	Burst length = 1, $t_{RC} \geq t_{RC}$ (min), I_{OL} = 0 mA, One bank active	75	mA	1
Precharge standby current in power down mode	I_{CC2P}	CKE ≤ V_{IL} (max.), t_{CK}= 15 ns	2	mA	
	I_{CC2PS}	CKE ≤ V_{IL} (max.), t_{CK}= ∞	1.5	mA	
Precharge standby current in non-power down mode	I_{CC2N}	CKE ≥ V_{IL} (min.), t_{CK}=15ns, /CS ≥ V_{IH} (min.) Input signals are changed one time during 30ns	20	mA	
	I_{CC2NS}	CKE ≥ V_{IL} (min.), t_{CK} = ∞ Input signals are stable	10	mA	
Active standby current in power down mode	I_{CC3P}	CKE ≤ V_{IL} (max), t_{CK} = 15ns	5	mA	
	I_{CC3PS}	CKE ≤ V_{IL} (max), t_{CK} = ∞	5	mA	
Active standby current in non-power down mode	I_{CC3N}	CKE ≥ V_{IL} (min), t_{CK} = 15ns, /CS ≥ V_{IH} (min) Input signals are changed one time during 30ns	35	mA	
	I_{CC3NS}	CKE ≥ V_{IL} (min), t_{CK} = ∞ Input signals are stable	25	mA	
operating current (Burst mode)	I_{CC4}	t_{CCD} ≥ 2CLKs , I_{OL} = 0 mA	110	mA	2
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min.)	160	mA	3
Self Refresh current	I_{CC6}	CKE ≤ 0.2V	2	mA	4

＊ All voltages referenced to Vss.

Note : 1. I_{CC1} depends on output loading and cycle rates.
Specified values are obtained with the output open.
Input signals are changed only one time during tCK (min)

2. I_{CC4} depends on output loading and cycle rates.
Specified values are obtained with the output open.
Input signals are changed only one time during tCK (min)

3. Input signals are changed only one time during tCK (min)

4. Standard power version.

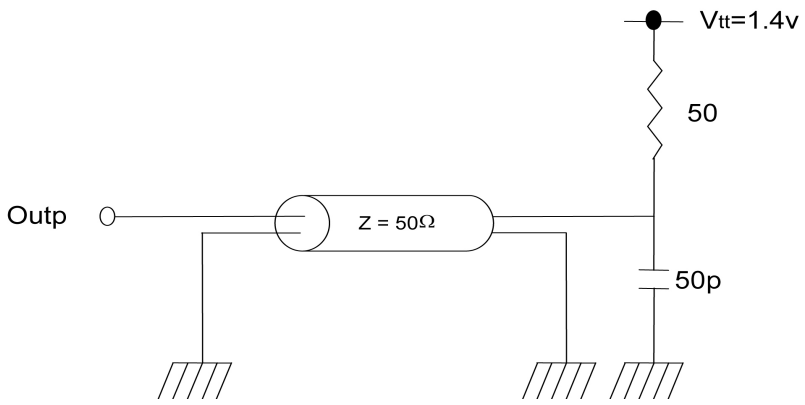
Recommended DC Operating Conditions (Continued)

Parameter	Symbol	Test condition	Min.	Max.	Unit
Input leakage current	I_{IL}	$0 \le V_I \le V_{DDQ}$, $V_{DDQ}=V_{DD}$ All other pins not under test=0 V	-0.5	+0.5	uA
Output leakage current	I_{OL}	$0 \le V_O \le V_{DDQ}$, D_{OUT} is disabled	-0.5	+0.5	uA
High level output voltage	V_{OH}	Io = -2mA	2.4		V
Low level output voltage	V_{OL}	Io = +2mA		0.4	V

AC Operating Test Conditions

(V_{DD} = 3.3V +/- 0.3 V, Ta = 0 ~ 70°C)

Output Reference Level	1.4V / 1.4V
Output Load	See diagram as below
Input Signal Level	2.4V / 0.4V
Transition Time of Input Signals	2ns
Input Reference Level	1.4V



Operating AC Characteristics

(VDD = 3.3V +/- 0.3 V, Ta = 0 ~ 70 °C)

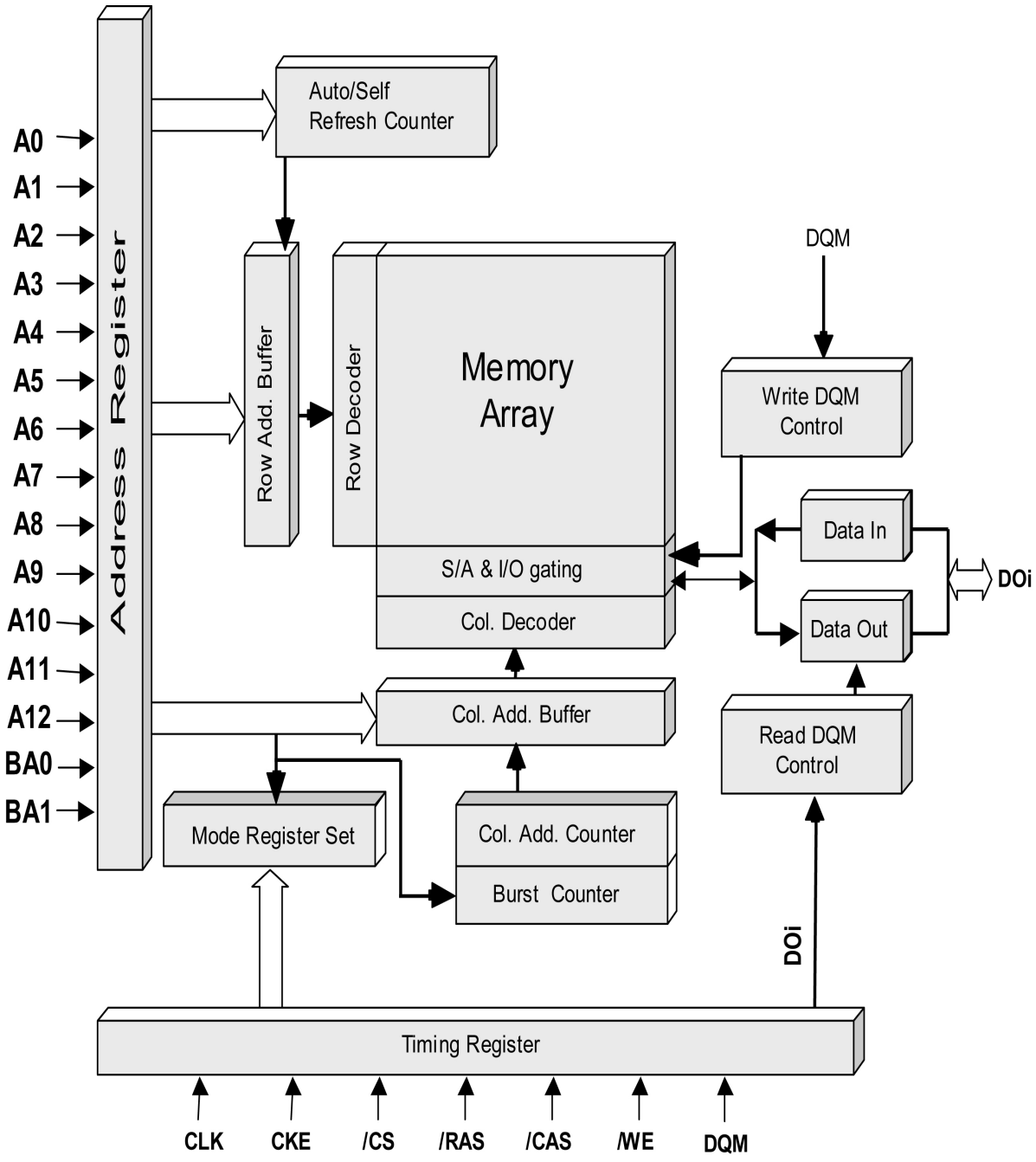
Parameter		Symbol	-7		-7.5		Units	Notes
			Min.	Max.	Min.	Max.		
Clock cycle time	CL = 3	t_{CK}	7		7.5		ns	
	CL = 2		7.5		10		ns	
Access time from CLK	CL = 3	t_{AC}		5.4		5.4	ns	
	CL = 2			5.4		6	ns	
CLK high level width		t_{CH}	2.5		2.5		ns	
CLK low level width		t_{CL}	2.5		2.5		ns	
Data-out hold time	CL = 3	t_{OH}	3		3		ns	
	CL = 2						ns	
Data-out high impedance time	CL = 3	t_{HZ}	3	7	3	7	ns	
	CL = 2						ns	
Data-out low impedance time		t_{LZ}	0		0		ns	
Input hold time		t_{IH}	1		1		ns	
Input setup time		t_{IS}	1.5		1.5		ns	
ACTIVE to ACTIVE command period		t_{RC}	62		67		ns	2
ACTIVE to PRECHARGE command period		t_{RAS}	42	100k	45	100k	ns	2
PRECHARGE to ACTIVE command period		t_{RP}	3		3		CLK	2
ACTIVE to READ/WRITE delay time		t_{RCD}	3		3		CLK	2
ACTIVE(one) to ACTIVE(another) command		t_{RRD}	2		2		CLK	2
READ/WRITE command to READ/WRITE command		t_{CCD}	1		1		CLK	
Data-in to PRECHARGE command		t_{DPL}	2		2		CLK	
Data-in to BURST stop command		t_{BDL}	1		1		CLK	
Data-out to high impedance from PRECHARGE command	CL = 3	t_{ROH}	3		3		CLK	
	CL = 2		2		2		CLK	
Refresh time(4,096 cycle)		t_{EF}		64		64	ms	

∗ All voltages referenced to Vss.

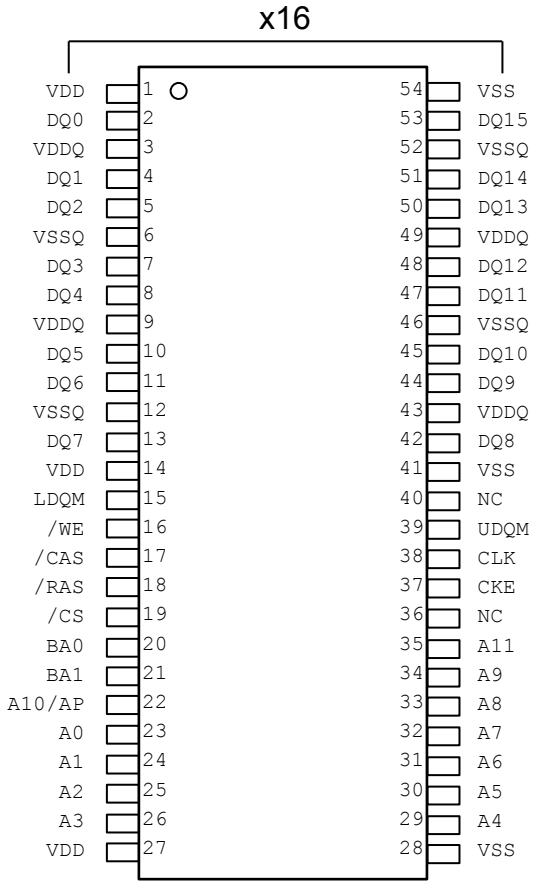
Note : 1. tHZ defines the time at which the output achieve the open circuit condition and is not referenced to output voltage levels.

2. These parameters account for the number of clock cycles and depend on the operating frequency of the clock, as follows :
The number of clock cycles = Specified value of timing/clock period
(Count fractions as a whole number)

Block Diagram



Pin Assignment : TSOP 54P



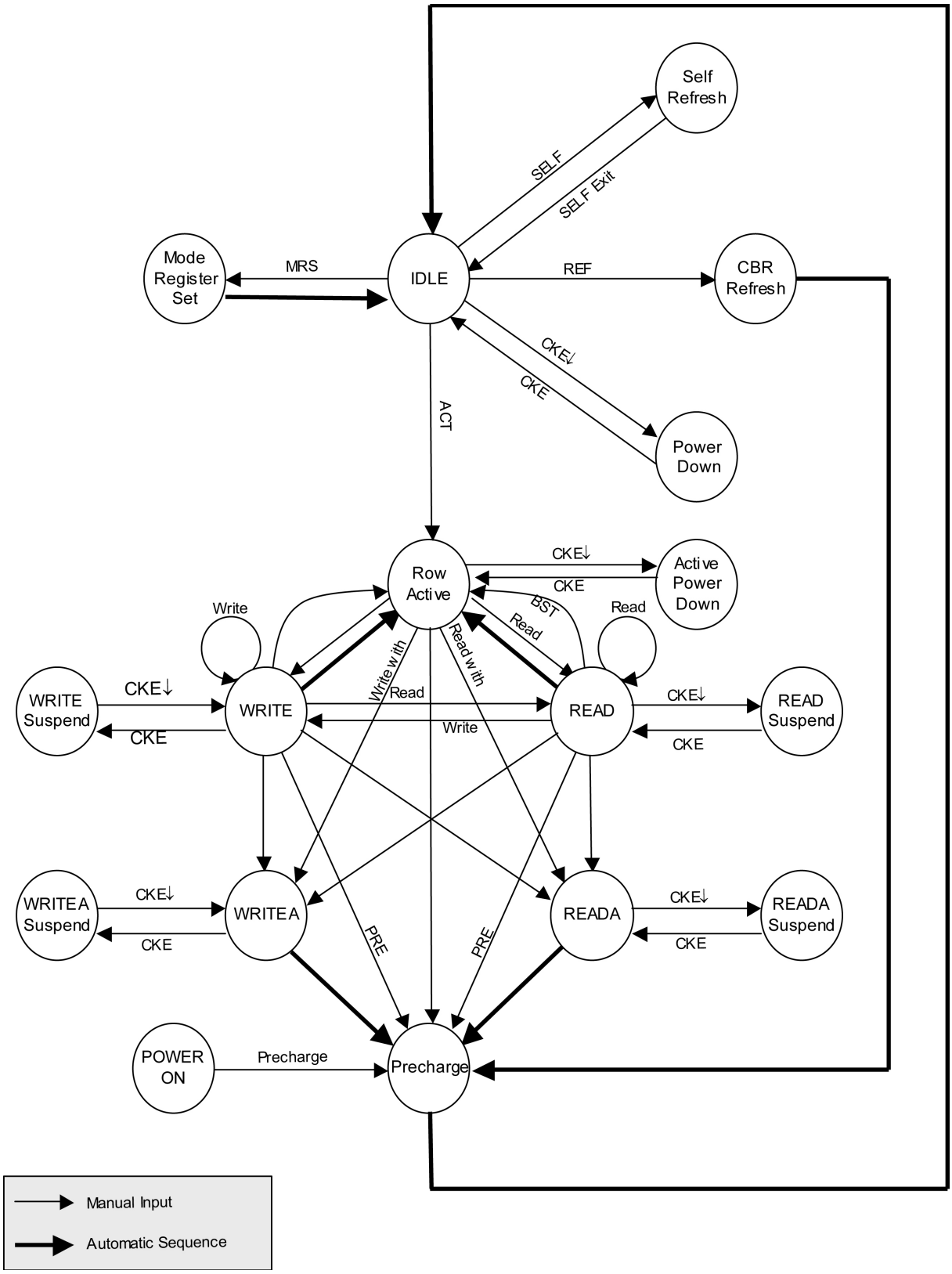
54pin TSOP-II

(400mil x 875mil)

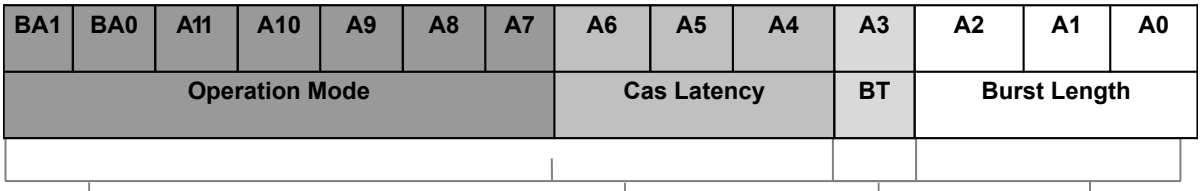
Pin Descriptions (Simplified)

Pin	Name	Pin Function
CLK	System Clock	Master Clock Input(Active on the Positive rising edge)
/CS	Chip select	Selects chip when active
CKE	Clock Enable	Activates the CLK when “H” and deactivates when “L”. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A0 ~ A11	Address	Row address (A0 to A11) is determined by A0 to A11 level at the bank active command cycle CLK rising edge. CA (CA0 to CA8) is determined by A0 to A8 level at the read or write command cycle CLK rising edge. And this column address becomes burst access start address. A10 defines the pre-charge mode. When A10= High at the pre-charge command cycle, all banks are pre-charged. But when A10= Low at the pre-charge command cycle, only the bank that is selected by BA0/BA1 is pre-charged.
BA0, BA1	Bank Address	Selects which bank is to be active.
/RAS	Row address strobe	Latches Row Addresses on the positive rising edge of the CLK with /RAS “L”. Enables row access & pre-charge.
/CAS	Column address strobe	Latches Column Addresses on the positive rising edge of the CLK with /CAS low. Enables column access.
/WE	Write Enable	Latches Column Addresses on the positive rising edge of the CLK with /CAS low. Enables column access.
UDQM / LDQM	Data input/output Mask	DQM controls I/O buffers.
DQ0 ~ 15	Data input/output	DQ pins have the same function as I/O pins on a conventional DRAM.
V_{DD} / V_{SS}	Power supply / Ground	V_{DD} and V_{SS} are power supply pins for internal circuits.
V_{DDQ} / V_{SSQ}	Power supply / Ground	V_{DDQ} and V_{SSQ} are power supply pins for the output buffers.
NC	No connection	This pin is recommended to be left No Connection on the device.

Simplified State Diagram



Address Input for Mode Register Set



Burst Length				
Sequential	Interleave	A2	A1	A0
1	1	0	0	0
2	2	0	0	1
4	4	0	1	0
8	8	0	1	1
Reserved	Reserved	1	0	0
Reserved	Reserved	1	0	1
Reserved	Reserved	1	1	0
Full Page	Reserved	1	1	1

Burst Type	A3
Interleave	1
Sequential	0

CAS Latency	A6	A5	A4
Reserved	0	0	0
Reserved	0	0	1
2	0	1	0
3	0	1	1
Reserved	1	0	0
Reserved	1	0	1
Reserved	1	1	0
Reserved	1	1	1

BA1	BA0	A11	A10	A9	A8	A7	Operation Mode
0	0	0	0	0	0	0	Normal
0	0	0	0	1	0	0	Burst read with Single-bit Write

Burst Type (A3)

Burst Length	A2	A1	A0	Sequential Addressing	Interleave Addressing
2	X	X	0	0 1	0 1
	X	X	0	1 0	1 0
4	X	0	0	0 1 2 3	0 1 2 3
	X	0	1	1 2 3 0	1 0 3 2
	X	1	0	2 3 0 1	2 3 0 1
	X	1	1	3 0 1 2	3 2 1 0
8	0	0	0	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7
	0	0	1	1 2 3 4 5 6 7 0	1 0 3 2 5 4 7 6
	0	1	0	2 3 4 5 6 7 0 1	2 3 0 1 6 7 4 5
	0	1	1	3 4 5 6 7 0 1 2	3 2 1 0 7 6 5 4
	1	0	0	4 5 6 7 0 1 2 3	4 5 6 7 0 1 2 3
	1	0	1	5 6 7 0 1 2 3 4	5 4 7 6 1 0 3 2
	1	1	0	6 7 0 1 2 3 4 5	6 7 4 5 2 3 0 1
	1	1	1	7 0 1 2 3 4 5 6	7 6 5 4 3 2 1 0
Full Page *	n	n	n	Cn Cn+1 Cn+2	-

* Page length is a function of I/O organization and column addressing

X16 (CA0 ~ CA8) : Full page = 512bits

Truth Table

1.Command Truth Table

Command	Symbol	CKE		/CS	/RAS	/CAS	/WE	BA0, BA1	A10	A11, A9~A0
		n-1	n							
Ignore Command	DESL	H	X	H	X	X	X	X	X	X
No operation	NOP	H	X	L	H	H	H	X	X	X
Burst stop	BSTH	H	X	L	H	H	L	X	X	X
Read	READ	H	X	L	H	L	H	V	L	V
Read with auto pre-charge	READA	H	X	L	H	L	H	V	H	V
Write	WRIT	H	X	L	H	L	L	V	L	V
Write with auto pre-charge	WRITA	H	X	L	L	H	H	V	H	V
Bank activate	ACT	H	X	L	L	H	H	V	V	V
Pre-charge select bank	PRE	H	X	L	L	H	L	V	L	X
Pre-charge all banks	PALL	H	X	L	L	H	L	X	H	X
Mode register set	MRS	H	X	L	L	L	L	L	L	V

2. DQM Truth Table

Command	Symbol	CKE		/CS
		n-1	n	
Data write / output enable	ENB	H	x	H
Data mask / output disable	MASK	H	x	L
Upper byte write enable / output enable	BSTH	H	x	L
Read	READ	H	x	L
Read with auto pre-charge	READA	H	x	L
Write	WRIT	H	x	L
Write with auto pre-charge	WRITA	H	x	L
Bank activate	ACT	H	x	L
Pre-charge select bank	PRE	H	x	L
Pre-charge all banks	PALL	H	x	L
Mode register set	MRS	H	x	L

3. CKE Truth Table

Command	Command	Symbol	CKE		/CS	/RAS	/CAS	/WE	Addr.
			n-1	n					
Activating	Clock suspend mode entry		H	L	X	X	X	X	X
Any	Clock suspend mode		L	L	X	X	X	X	X
Clock suspend	Clock suspend mode exit		L	H	X	X	X	X	X
Idle	CBR refresh command	REF	H	H	L	L	L	H	X
Idle	Self refresh entry	SELF	H	L	L	L	L	H	X
Self refresh	Self refresh exit		L	H	L	H	H	H	X
			L	H	H	X	X	X	X
Idle	Power down entry		H	L	X	X	X	X	X
Power down	Power down exit		L	H	X	X	X	X	X

Note : H = High level, L = Low level, X = High or Low level (Don't care), V = Valid data input

4. Operative Command Table

Current state	/CS	/R	/C	/W	Addr.	Command	Action	Notes
Idle	H	X	X	X	X	DESL	Nop or power down	2
	L	H	H	X	X	NOP or BST	Nop or power down	2
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA/RA	ACT	Row activating	
	L	L	H	L	BA, A10	PRE/PALL	Nop	
	L	L	L	H	X	REF/SELF	Refresh or self refresh	4
	L	L	L	L	Op-Code	MRS	Mode register accessing	
Row active	H	X	X	X	X	DESL	Nop	
	L	H	H	X	X	NOP or BST	Nop	
	L	H	L	H	BA/CA/A10	READ/READA	Begin read : Determine AP	5
	L	H	L	L	BA/CA/A10	WRIT/WRITA	Begin write : Determine AP	5
	L	L	H	H	BA/RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	Pre-charge	6
	L	L	L	H	X	REF/SELF	ILLEGAL	4
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Read	H	X	X	X	X	DESL	Continue burst to end→ Row active	
	L	H	H	H	X	NOP	Continue burst to end→ Row active	
	L	H	H	L	X	BST	Burst stop→ Row active	
	L	H	L	H	BA/CA/A10	READ/READA	Terminate burst, new read : Determine AP	7
	L	L	L	L	BA/CA/A10	WRIT/WRITA	Terminate burst, start write : Determine AP	7.8
	L	L	H	H	BA/RA	ACT	ILLEGAL	3
	L	L	H	L	BA/A10	PRE/PALL	Terminate burst, pre-charging	4
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write	H	X	X	X	X	DESL	Continue burst to end→ Write recovering	
	L	H	H	H	X	NOP	Continue burst to end→ Write recovering	
	L	H	H	L	X	BST	Burst stop→ Row active	
	L	H	L	H	BA/CA/A10	READ/READA	Terminate burst, start read: Determine AP 7, 8	7.8
	L	L	L	L	BA/CA/A10	WRIT/WRITA	Terminate burst, new write: Determine AP 7	7
	L	L	H	H	BA/RA	ACT	ILLEGAL	3
	L	L	H	L	BA/A10	PRE/PALL	Terminate burst, pre-charging	9
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	

Remark H = High level, L = Low level, X = High or Low level (Don't care)

Current state	/CS	/R	/C	/W	Addr.	Command	Action	Notes
Read with AP	H	X	X	X	X	DESL	Continue burst to end→ Pre-charging	
	L	H	H	H	X	NOP	Continue burst to end→ Pre-charging	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA/RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write with AP	H	X	X	X	X	DESL	burst to end→ Write recovering with auto pre-charge	
	L	H	H	H	X	NOP	Continue burst to end→ Write recovering with auto pre-charge	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA/RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Pre-charging	H	X	X	X	X	DESL	Nop→ Enter idle after t_{RP}	
	L	H	H	H	X	NOP	Nop→ Enter idle after t_{RP}	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA/RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	Nop→ Enter idle after t_{RP}	
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Row activating	H	X	X	X	X	DESL	Nop→ Enter idle after t_{RCD}	
	L	H	H	H	X	NOP	Nop→ Enter idle after t_{RCD}	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA/RA	ACT	ILLEGAL	3.1
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	

Remark H = High level, L = Low level, X = High or Low level (Don't care), AP = Auto Pre-charge

Current state	/CS	/R	/C	/W	Addr.	Command	Action	Notes
Write recovering	H	X	X	X	X	DESL	Nop→ Enter row active after t_{DPL}	
	L	H	H	H	X	NOP	Nop→ Enter row active after t_{DPL}	
	L	H	H	L	X	BST	Nop→ Enter row active after t_{DPL}	
	L	H	L	H	BA/CA/A10	READ/READA	Start read, Determine AP	
	L	H	L	L	BA/CA/A10	WRIT/WRITA	New write, Determine AP	8
	L	L	H	H	BA/RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write recovering with AP	H	X	X	X	X	DESL	Nop→ Enter pre-charge after t_{DPL}	
	L	H	H	H	X	NOP	Nop→ Enter pre-charge after t_{DPL}	
	L	H	H	L	X	BST	Nop→ Enter pre-charge after t_{DPL}	
	L	H	L	H	BA/CA/A10	READ/READA	ILLEGAL	3.8
	L	H	L	L	BA/CA/A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA/RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Refreshing	H	X	X	X	X	DESL	Nop→ Enter idle after t_{RC}	
	L	H	H	X	X	NOP/ BST	Nop→ Enter idle after t_{RC}	
	L	H	L	X	X	READ/WRIT	ILLEGAL	
	L	L	H	X	X	ACT/PRE/PALL	ILLEGAL	
	L	L	L	X	X	REF/SELF/MRS	ILLEGAL	
Mode Register Accessing	H	X	X	X	X	DESL	Nop	
	L	H	H	H	X	NOP	Nop	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	X	X	READ/WRIT	ILLEGAL	
	L	L	X	X	X	ACT/PRE/PALL/ REF/SELF/MRS	ILLEGAL	

Remark H = High level, L = Low level, X = High or Low level (Don't care), AP = Auto Pre-charge

Notes 1. All entries assume that CKE was active (High level) during the preceding clock cycle.

2. If all banks are idle, and CKE is inactive (Low level), SDRAM will enter Power down mode. All input buffers except CKE will be disabled.

3. Illegal to bank in specified states;Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.

4. If all banks are idle, and CKE is inactive (Low level), SDRAM will enter Self refresh mode. All input buffers except CKE will be disabled.

5. Illegal if t_{RCD} is not satisfied.

6. Illegal if t_{RAS} is not satisfied.

7. Must satisfy burst interrupt condition.

8. Must satisfy bus contention, bus turn around, and/or write recovery requirements.

9. Must mask preceding data which don't satisfy t_{DPL}.

10. Illegal if t_{RRD} is not satisfied.

5. Command Truth Table for CKE

Current state	CKE n-1	CKE n	/CS	/R	/C	/W	Addr.	Action	Notes
Self refresh	H	X	X	X	X	X	X	INVALID, CLK (n – 1) would exit self refresh	
	L	H	H	X	X	X	X	Self refresh recovery	
	L	H	L	H	H	X	X	Self refresh recovery	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	Maintain self refresh	
Self refresh	H	H	H	X	X	X	X	Idle after t_{RC}	
	H	H	L	H	H	X	X	Idle after t_{RC}	
recovery	H	H	L	H	L	X	X	ILLEGAL	
	H	H	L	L	X	X	X	ILLEGAL	
	H	L	H	X	X	X	X	ILLEGAL	
	H	L	L	H	H	X	X	ILLEGAL	
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	X	X	X	ILLEGAL	
Power down	H	X	X	X	X	X	X	INVALID, CLK(n-1) would exit power down	
	L	H	X	X	X	X	X	Exit power down→ Idle	
	L	L	X	X	X	X	X	Maintain power down mode	
Both banks	H	H	H	X	X	X		Refer to operations in Operative Command Table	
	H	H	L	H	X	X		Refer to operations in Operative Command Table	
idle	H	H	L	L	H	X		Refer to operations in Operative Command Table	
	H	H	L	L	L	H	X	Refresh	
	H	H	L	L	L	L	Op-Code	Refer to operations in Operative Command Table	
	H	L	H	X	X	X		Refer to operations in Operative Command Table	
	H	L	L	H	X	X		Refer to operations in Operative Command Table	
	H	L	L	L	H	X		Refer to operations in Operative Command Table	
	H	L	L	L	L	H	X	Self refresh	1
	H	L	L	L	L	L	Op-Code	Refer to operations in Operative Command Table	
	L	X	X	X	X	X	X	Power down	1
Row active	H	X	X	X	X	X	X	Refer to operations in Operative Command Table	
	L	X	X	X	X	X	X	Power down	1
Any state	H	H	X	X	X	X		Refer to operations in Operative Command Table	
	H	L	X	X	X	X	X	Begin clock suspend next cycle	2
other than	L	H	X	X	X	X	X	Exit clock suspend next cycle	
listed above	L	L	X	X	X	X	X	Maintain clock suspend	

Remark : H = High level, L = Low level, X = High or Low level (Don't care)

Notes: 1. Self refresh can be entered only from the both banks idle state.

Power down can be entered only from both banks idle or row active state.

2. Must be legal command as defined in Operative Command Tabl

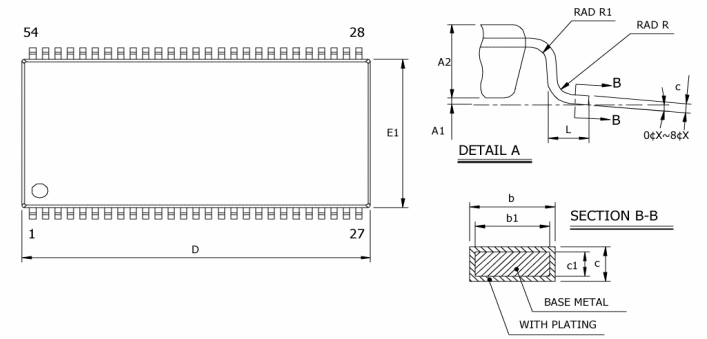
Recommended Power On and Initialization :

The following power on and initialization sequence guarantees the device is preconditioned to each users specific needs.(Like a conventional DRAM)
During power on, all VDD and VDDQ pins must be built up simultaneously to the specified voltage when the input signals are held in the “NOP” state.
The power on voltage must not exceed VDD+0.3V on any of the input pins or VDD supplies. (CLK signal started at same time)
After power on, an initial pause of 200 μs is required followed by a precharge of all banks using the precharge command.
To prevent data contention on the DQ bus during power on, it is required that the DQM and CKE pins be held high during the initial pause period.
Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register.
A minimum of eight Auto Refresh cycles (CBR) are also required, and these may be done before or after programming the Mode Register.

Package Drawing :

TSOPII 54P

DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	1.20	---	---	0.047
A1	0.05	---	0.15	0.002	---	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	---	0.45	0.012	---	0.018
b1	0.30	---	0.40	0.012	---	0.016
c	0.12	---	0.21	0.005	---	0.008
c1	0.12	---	0.16	0.005	---	0.006
D	22.09	22.22	22.35	0.870	0.875	0.880
ZD	0.71 REF.			0.028 REF.		
e	0.80 BASIC			0.0315 BASIC		
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
L	0.40	0.50	0.60	0.016	0.020	0.024
R	0.12	---	0.25	0.005	---	0.010
R1	0.12	---	---	0.005	---	---



NOTE:
1. CONTROLLING DIMENSION : MILLIMETERS
2. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSION.
   MOLD PROTRUSION SHALL NOT EXCEED 0.15mm(0.006") PER SIDE.
   DIMENSION E1 DOES NOT INCLUDE INTERLEAD PROTRUSION.
   INTERLEAD PROTRUSION SHALL NOT EXCEED 0.25mm(0.01") PER SIDE.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSIONS/INTRUSION.
   ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD TO BE WIDER THAN THE MAX b DIMENSION BY MORE THAN 0.13mm.
   DAMBAR INTRUSION SHALL NOT CAUSE THE LEAD TO BE NARROWER THAN THE MIN b DIMENSION BY MORE THAN 0.07mm.