March 2006

LM27222
High-Speed 4.5A Synchronous MOSFET Driver

General Description

The LM27222 is a dual N-channel MOSFET driver designed to drive MOSFETs in push-pull configurations as typically used in synchronous buck regulators. The LM27222 takes the PWM output from a controller and provides the proper timing and drive levels to the power stage MOSFETs. Adaptive shoot-through protection prevents damaging and efficiency reducing shoot-through currents, thus ensuring a robust design capable of being used with nearly any MOSFET. The adaptive shoot-through protection circuitry also reduces the dead time down to as low as 10ns, ensuring the highest operating efficiency. The peak sourcing and sinking current for each driver of the LM27222 is about 3A and 4.5Amps respectively with a Vgs of 5V. System performance is also enhanced by keeping propagation delays down to 8ns. Efficiency is once again improved at all load currents by supporting synchronous, non-synchronous, and diode emulation modes through the LEN pin. The minimum output pulse width realized at the output of the MOSFETs is as low as 30ns. This enables high operating frequencies at very high conversion ratios in buck regulator designs. To support low power states in notebook systems, the LM27222 draws only 5µA from the 5V rail when the IN and LEN inputs are low or floating.

Features

- Adaptive shoot-through protection
- 10ns dead time
- 8ns propagation delay
- 30ns minimum on-time
- 0.4Ω pull-down and 0.9Ω pull-up drivers
- 4.5A peak driving current
- MOSFET tolerant design
- 5µA quiescent current
- 30V maximum input voltage in buck configuration
- 4V to 6.85V operating voltage
- SO-8 and LLP packages

Applications

- High Current Buck And Boost Voltage Converters
- Fast Transient DC/DC Power Supplies
- Single Ended Forward Output Rectification
- CPU And GPU Core Voltage Regulators

Typical Application

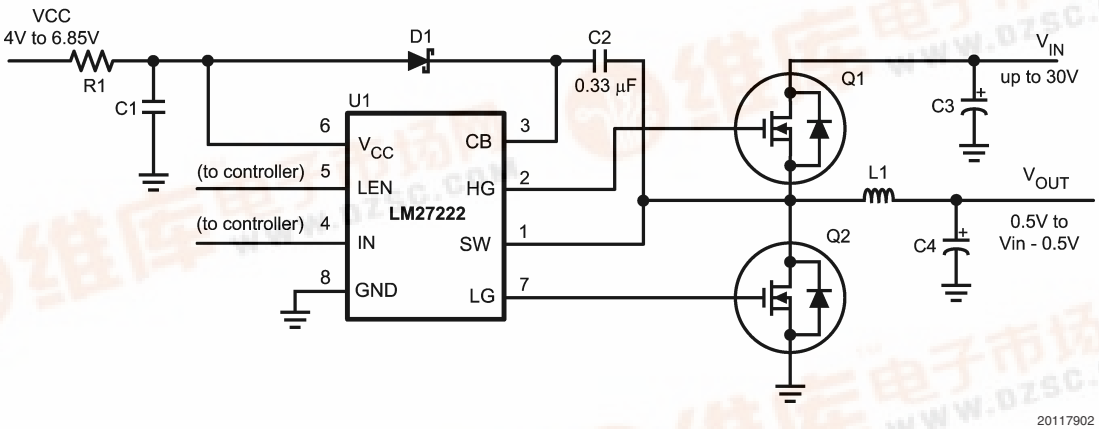
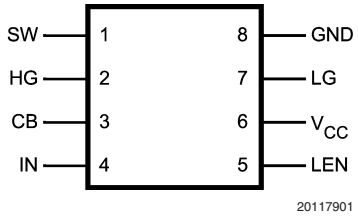


FIGURE 1.

Connection Diagram



Top View
SO-8 (NS Package # M08A) θ_{JA} = 172˚C/W
or
LLP-8 (NS Package # SDC08A) θ_{JA} = 39˚C/W

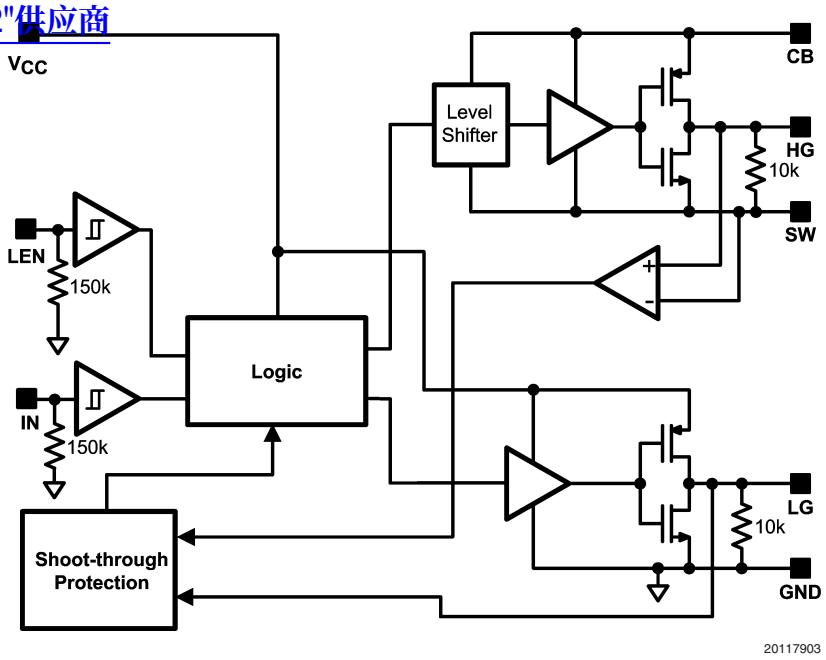
Ordering Information

Order Number	Size	NSC Drawing #	Package Type	Supplied As
LM27222M	SO-8	M08A	Rail	95 Units/Rail
LM27222MX			Tape and Reel	2500 Units/Reel
LM27222SD	LLP-8	SDC08A	Tape and Reel	1000 Units/Reel
LM27222SDX			Tape and Reel	4500 Units/Reel

Pin Descriptions

Pin #	Pin Name	Pin Function
1	SW	High-side driver return. Should be connected to the common node of high and low-side MOSFETs.
2	HG	High-side gate drive output. Should be connected to the high-side MOSFET gate. Pulled down internally to SW with a 10K resistor to prevent spurious turn on of the high-side MOSFET when the driver is off.
3	CB	Bootstrap. Accepts a bootstrap voltage for powering the high-side driver.
4	IN	Accepts a PWM signal from a controller. Active High. Pulled down internally to GND with a 150K resistor to prevent spurious turn on of the high-side MOSFET when the controller is inactive.
5	LEN	Low-side gate enable. Active High. Pulled down internally to GND with a 150K resistor to prevent spurious turn-on of the low-side MOSFET when the controller is inactive.
6	V_{CC}	Connect to +5V supply.
7	LG	Low-side gate drive output. Should be connected to low-side MOSFET gate. Pulled down internally to GND with a 10K resistor to prevent spurious turn on of the low-side MOSFET when the driver is off.
8	GND	Ground.

Block Diagram



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{CC} to GND	-0.3V to 7V
CB to GND	-0.3V to 36V
CB to SW	-0.3V to 7V
SW to GND (Note 2)	-2V to 36V
LEN, IN, LG to GND	-0.3V to V_{CC} + 0.3V ≤ 7V
HG to GND	-0.3V to 36V
Junction Temperature	+150˚C
Power Dissipation (Note 3)	720mW
Storage Temperature	−65˚ to 150˚C
ESD Susceptibility	
Human Body Model	2kV

Operating Ratings (Note 1)

VCC	4V to 6.85V
Junction Temperature Range	−40˚ to 125˚C
CB (max)	33V

Electrical Characteristics (Note 4)

VCC = CB = 5V, SW = GND = 0V, unless otherwise specified. Typicals and limits appearing in plain type apply for $T_A = T_J$ = +25˚C. Limits appearing in **boldface** type apply over the entire operating temperature range (-40˚C ≤ T_J ≤ 125˚C).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER SUPPLY						
I_{q_op}	Operating Quiescent Current	IN = 0V, LEN = 0V		5	15	µA
					30	
		IN = 0V, LEN = 5V	500	540	650	µA
					825	
HIGH-SIDE DRIVER						
	Peak Pull-up Current			3		A
R_{H-pu}	Pull-up Rds_on	$I_{CB} = I_{HG}$ = 0.3A		0.9	**2.5**	Ω
	Peak Pull-down Current			4.5		A
R_{H-pd}	Pull-down Rds_on	$I_{SW} = I_{HG}$ = 0.3A		0.4	**1.5**	Ω
t_4	Rise Time	Timing Diagram, C_{LOAD} = 3.3nF		17		ns
t_6	Fall Time	Timing Diagram, C_{LOAD} = 3.3nF		12		ns
t_3	Pull-up Dead Time	Timing Diagram		9.5		ns
t_5	Pull-down Delay	Timing Diagram		16.5		ns
t_{on_min}	Minimum Positive Output Pulse Width			30		ns
LOW-SIDE DRIVER						
	Peak Pull-up Current			3.2		A
R_{L-pu}	Pull-up Rds_on	$I_{VCC} = I_{LG}$ = 0.3A		0.9	**2.5**	Ω
	Peak Pull-down Current			4.5		A
R_{L-pd}	Pull-down Rds_on	$I_{GND} = I_{LG}$ = 0.3A		0.4	**1.5**	Ω
t_8	Rise Time	Timing Diagram, C_{LOAD} = 3.3nF		17		ns
t_2	Fall Time	Timing Diagram, C_{LOAD} = 3.3nF		14		ns
t_7	Pull-up Dead Time	Timing Diagram		11.5		ns
t_1	Pull-down Delay	Timing Diagram		7.7		ns
PULL-DOWN RESISTANCES						
	HG-SW Pull-down Resistance			10k		Ω
	LG-GND Pull-down Resistance			10k		Ω
	LEN-GND Pull-down Resistance			150K		Ω
	IN-GND Pull-down Resistance			150K		Ω
LEAKAGE CURRENTS						
I_{leak_IN}	IN pin Leakage Current	IN = 0V, Source Current		50		nA
		IN = 5V, Sink Current		33		µA

Electrical Characteristics (Note 4) (Continued)

VCC = VBST = VEN = 5V, unless otherwise specified. Typicals and limits appearing in plain type apply for $T_A = T_J =$ +25˚C. Limits appearing in **boldface** type apply over the entire operating temperature range (-40˚C ≤ T_J ≤ 125˚C).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{leak_LEN}	LEN pin Leakage Current	LEN = 0V, Source Current		200		nA
		LEN = 5V, Sink Current		33		µA
LOGIC						
V_{IH_LEN}	LEN Low to High Threshold	Low to High Transition			**65**	% of V_{CC}
V_{IL_LEN}	LEN High to Low Threshold	High to Low Transition	**30**			% of V_{CC}
V_{IH_IN}	IN Low to High Threshold	Low to High Transition			**65**	% of V_{CC}
V_{IL_IN}	IN High to Low Threshold	High to Low Transition	**30**			% of V_{CC}
	Threshold Hysteresis			0.7		V

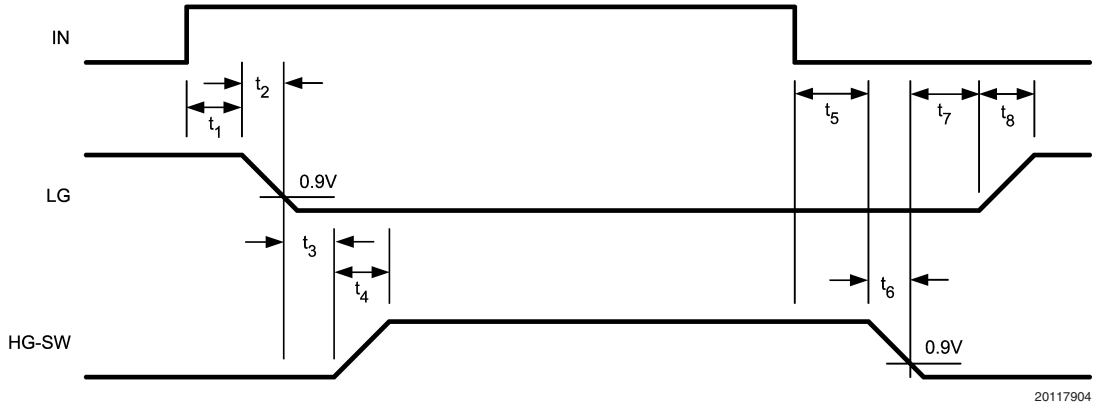
Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. **Operating ratings** are conditions under which the device operates correctly. Operating Ratings do not imply guaranteed performance limits.

Note 2: The SW pin can have -2V to -0.5 volts applied for a maximum duty cycle of 10% with a maximum period of 1 second. There is no duty cycle or maximum period limitation for a SW pin voltage range of -0.5V to 30 Volts.

Note 3: Maximum allowable power dissipation is a function of the maximum junction temperature, T_{JMAX}, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{MAX} = (T_{JMAX}-T_A) / \theta_{JA}$. The junction-to-ambient thermal resistance, θ_{JA}, for the LM27222M, it is 165˚C/W. For a T_{JMAX} of 150˚C and T_A of 25˚C, the maximum allowable power dissipation is 0.76W. The θ_{JA} for the LM27222SD is 42˚C/W. For a T_{JMAX} of 150˚C and TA of 25˚C, the maximum allowable power dissipation is 3W.

Note 4: Min and Max limits are 100% production tested at 25˚C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate National's Average Outgoing Quality Level (AOQL).

Timing Diagram



Typical Waveforms

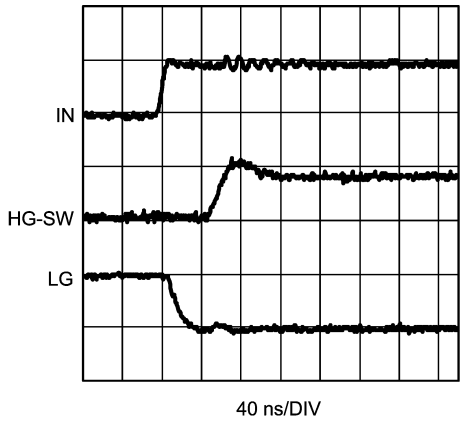


FIGURE 2. PWM Low-to-High Transition at IN Input

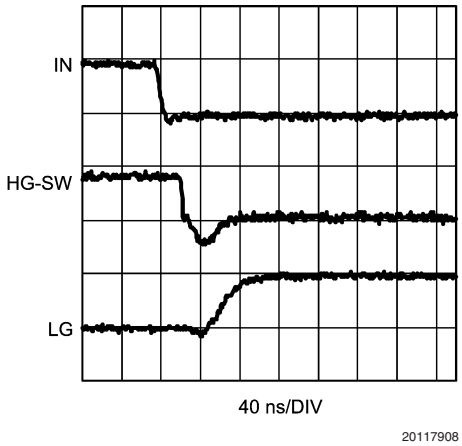


FIGURE 3. PWM High-to-Low Transition at IN Input

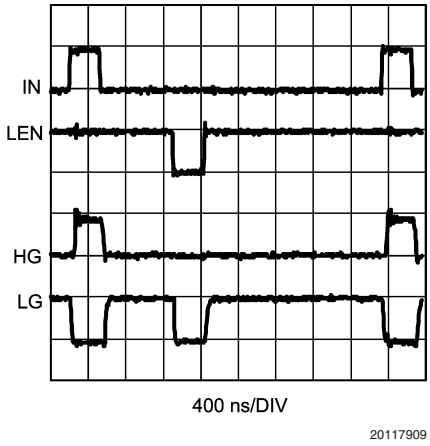


FIGURE 4. LEN Operation

The typical waveforms are from a circuit similar to *Figure 1* with:

Q1: 2 x Si7390DP

Q2: 2 x Si7356DP

L1: 0.4 µH

V_{IN}: 12V

Application Information

GENERAL

The LM27222 is designed for high speed and high operating reliability. The driver can handle very narrow, down to zero, PWM pulses in a guaranteed, deterministic way. Therefore, the HG and LG outputs are always in predictable states. No latches are used in the HG and LG control logic so the drivers cannot get "stuck" in the wrong state. The driver design allows for powering up with a pre-biasing voltage being present at the regulator output. To reduce conduction losses in DC-DC converters with low duty factors the LM27222 driver can be powered from a 6.5V ±5% power rail.

It is recommended to use the same power rail for both the controller and driver. If two different power rails are used, never allow the PWM pulse magnitude at the IN input or the control voltage at the LEN input to be above the driver V_{CC} voltage or unpredictable HG and LG outputs pulse widths may result.

MINIMUM PULSE WIDTH

As the input pulse width to the IN pin is decreased, the pulse width of the high-side gate drive (HG-SW) also decreases. However, for input pulse widths 60ns and smaller, the HG-SW remains constant at 30ns. Thus the minimum pulse width of the driver output is 30ns. *Figure 5* shows an input pulse at the IN pin 20ns wide, and the output of the driver, as measured between the nodes HG and SW is a 30ns wide pulse. *Figure 6* shows the variation of the SW node pulse width vs IN pulse width. At the IN pin, if a falling edge is followed by a rising edge within 5ns, the HG may ignore the rising edge and remain low until the IN pin toggles again. If a rising edge is followed by a falling edge within 5ns, the pulse may be completely ignored.

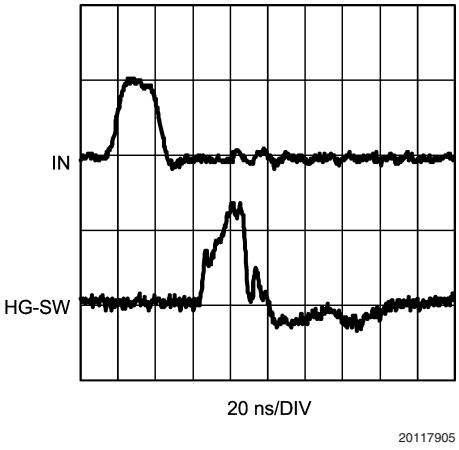


FIGURE 5. Min On Time

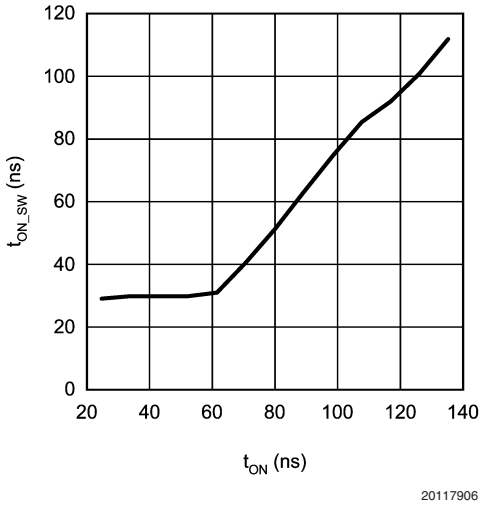


FIGURE 6.

ADAPTIVE SHOOT-THROUGH PROTECTION

The LM27222 prevents shoot-through power loss by ensuring that both the high- and low-side MOSFETs are not conducting at the same time. When the IN signal rises, LG is first pulled down. The adaptive shoot-through protection circuit waits for LG to reach 0.9V before turning on HG. Similarly, when IN goes low, HG is pulled down first, and the circuit turns LG on only after the voltage difference between the high-side gate and the switch node, i.e. HG-SW, has fallen to 0.9V.

It is possible in some applications that at power-up the driver's SW pin is above 3V in either buck or boost converter applications. For instance, in a buck configuration a pre-biasing voltage can be either a voltage from anothert power rail connected to the load, or a leakage voltage through the load, or it can be an output capacitor pre-charged above 3V while no significant load is present. In a boost application it can be an input voltage rail above 3V.

In the case of insufficient initial CB-SW voltage (less than 2V) such as when the output rail is pre-biased, the shoot-through protection circuit holds LG low for about 170ns, beginning from the instant when IN goes high. After the 170ns delay, the status of LG is dictated by LEN and IN. Once LG goes high and SW goes low, the bootstrap capacitor will be charged up (assuming SW is grounded for long enough time). As a result, CB-SW will be close to 5V and the LM27222 will now fully support synchronous operation.

The dead-time between the high- and low-side pulses is kept as small as possible to minimize conduction through the body diode of the low-side MOSFET(s).

Application Information (Continued)

POWER DISSIPATION

The power dissipated in the driver IC when switching synchronously can be calculated as follows:

$$P = \frac{f_{SW} \times V_{CC}}{2} \left\{ Q_{G\text{-}H} \left[\left(\frac{R_{H\text{-}pu}}{R_{H\text{-}pu} + R_{G\text{-}H}} \right) + \left(\frac{R_{H\text{-}pd}}{R_{H\text{-}pd} + R_{G\text{-}H}} \right) \right] + Q_{G\text{-}L} \left[\left(\frac{R_{L\text{-}pu}}{R_{L\text{-}pu} + R_{G\text{-}L}} \right) + \left(\frac{R_{L\text{-}pd}}{R_{L\text{-}pd} + R_{G\text{-}L}} \right) \right] \right\}$$

where f_{SW} = switching frequency

V_{CC} = voltage at the V_{CC} pin,

Q_{G_H} = total gate charge of the (parallel combination of the) high-side MOSFET(s)

Q_{G_L} = total gate charge of the (parallel combination of the) low-side MOSFET(s)

R_{G_H} = gate resistance of the (parallel combination of the) high-side MOSFET(s)

R_{G_L} = gate resistance of the (parallel combination of the) low-side MOSFET(S)

R_{H_pu} = pull-up R_{DS_ON} of the high-side driver

R_{H_pd} = pull-down R_{DS_ON} of the high-side driver

R_{L_pu} = pull-up R_{DS_ON} of the low-side driver

R_{L_pd} = pull-down R_{DS_ON} of the low-side driver

PC BOARD LAYOUT GUIDELINES

1. Place the driver as close to the MOSFETs as possible.
2. HG, SW, LG, GND: Run short, thick traces between the driver and the MOSFETs. To minimize parasitics, the traces for HG and SW should run parallel and close to each other. The same is true for LG and GND.
3. Driver V_{CC}: Place the decoupling capacitor close to the V_{CC} and GND pins.
4. The high-current loop between the high-side and low-side MOSFETs and the input capacitors should be as small as possible.
5. There should be enough copper area near the MOSFETs and the inductor for heat dissipation. Vias may also be added to carry the heat to other layers.

TYPICAL APPLICATION CIRCUIT DESCRIPITON

The Application Example on the following page shows the LM27222 being used with National's LM27212, a 2-phase hysteretic current mode controller. Although this circuit is capable of operating from 5V to 28V, the components are optimized for an input voltage range of 9V to 28V. The high-side FET is selected for low gate charge to reduce switching losses. For low duty cycles, the average current through the high-side FET is relatively small and thus we trade off higher conduction losses for lower switching losses. The low-side FET is selected solely on R_{DS_ON} to minimize conduction losses. If the input voltage range were 4V to 6V, the MOSFET selection should be changed. First, much lower voltage FETs can be used, and secondly, high-side FET R_{DS_ON} becomes a larger loss factor than the switching losses. Of course with a lower input voltage, the input capacitor voltage rating can be reduced and the inductor value can be reduced as well. For a 4V to 6V application, the inductor can be reduced to 200nH to 300nH. The switching frequency of the LM27212 is determined by the allowed ripple current in the inductor. This circuit is set for approximately 300kHz. At lower input voltages, higher frequencies are possible without suffering a significant efficiency loss. Although the LM27222 can support operating frequencies up to 2MHz in many applications, the LM27212 should be limited to about 1MHz. The control architecture of the LM27212 and the low propagation times of the LM27222 potentially gives this solution the fastest transient response in the industry.

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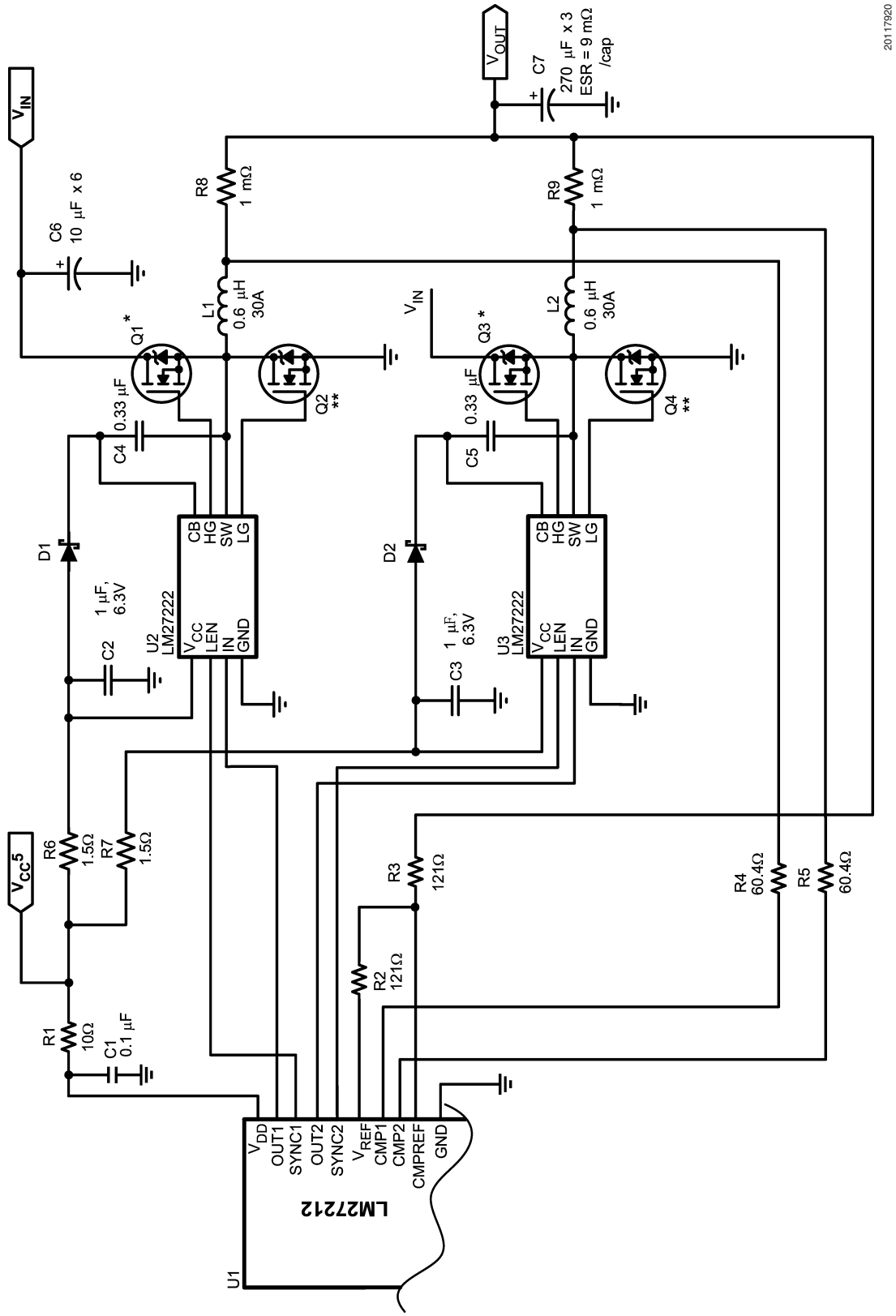
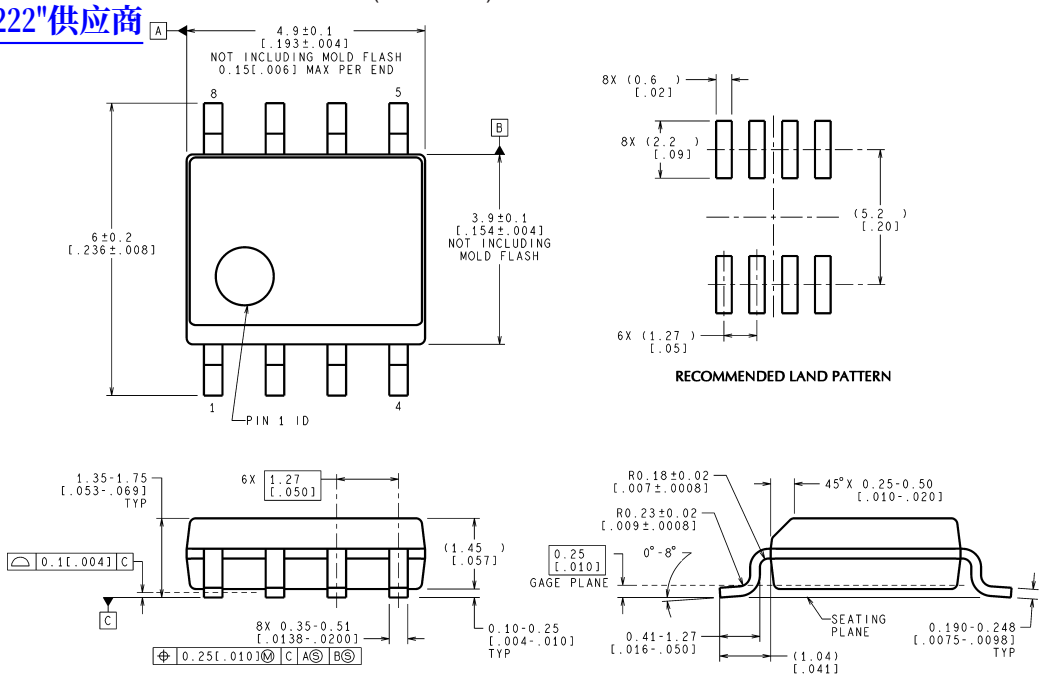
Application Example



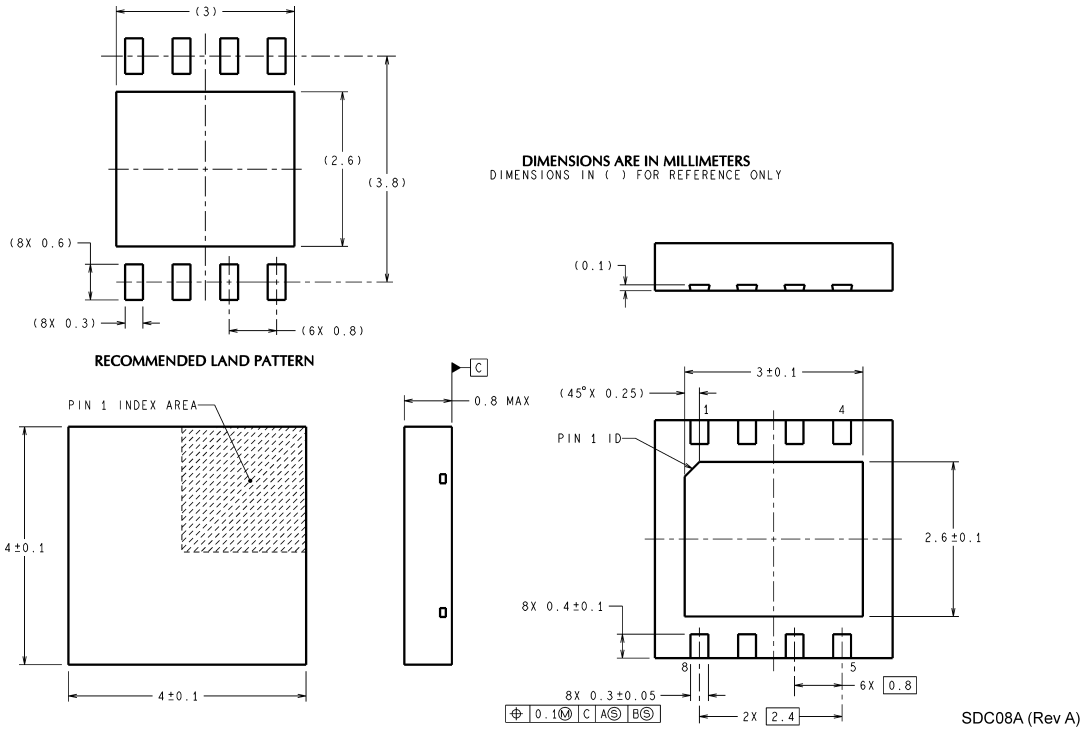
Physical Dimensions inches (millimeters) unless otherwise noted



CONTROLLING DIMENSION IS MILLIMETER
VALUES IN [ ] ARE INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

M08A (Rev K)

8-Lead Small Outline Package
Order Number: LM27222M, LM27222MX
NS Package Number M08A



SDC08A (Rev A)

8-Lead LLP Package
Order Number: LM27222SD, LM27222SDX
NS Package Number SDC08A

Notes