P-channel silicon field-effect transistors

J174; J175; J176; J177

DESCRIPTION

Silicon symmetrical p-channel junction FETs in a plastic TO-92 envelope and intended for application with analog switches, choppers, commutators etc.

A special feature is the interchangeability of the drain and source connections.

PINNING

1 = source
2 = gate
3 = drain

Note: Drain and source are interchangeable.

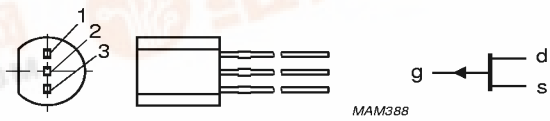

Fig.1 Simplified outline and symbol, TO-92.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30				V
Gate-source voltage	V_{GSO}	max.	30				V
Gate current	$-I_G$	max.	50				mA
Total power dissipation up to T_{amb} = 50 °C	P_{tot}	max.	400				mW
			J174	**J175**	**J176**	**J177**	
Drain current $-V_{DS}$ = 15 V; V_{GS} = 0	$-I_{DSS}$	min.	20	7	2	1.5	mA
		max.	135	70	35	20	mA
Drain-source ON-resistance $-V_{DS}$ = 0.1 V; V_{GS} = 0	$R_{DS\ on}$	max.	85	125	250	300	Ω

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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage	V_{GSO}	max.	30	V
Gate-drain voltage	V_{GDO}	max.	30	V
Gate current (DC)	$-I_G$	max.	50	mA
Total power dissipation				
up to T_{amb} = 50 °C	P_{tot}	max.	400	mW
Storage temperature range	T_{stg}		−65 to +150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			J174	J175	J176	J177	
Gate cut-off current							
V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	1	1	1	1	nA
Drain cut-off current							
$-V_{DS}$ = 15 V; V_{GS} = 10 V	$-I_{DSX}$	max.	1	1	1	1	nA
Drain current							
$-V_{DS}$ = 15 V; V_{GS} = 10 V	$-I_{DSS}$	min.	20	7	2	1.5	mA
		max.	135	70	35	20	mA
Gate-source breakdown voltage							
I_G = 1 µA; V_{DS} = 0	$V_{(BR)GSS}$	min.	30	30	30	30	V
Gate-source cut-off voltage							
$-I_D$ = 10 nA; V_{DS} = −15 V	$V_{GS\ off}$	min.	5	3	1	0.8	V
		max.	10	6	4	2.25	V
Drain-source ON-resistance							
$-V_{DS}$ = 0.1 V; V_{GS} = 0	R_{DSon}	max.	85	125	250	300	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Input capacitance, f = 1 MHz							
V_{GS} = 10 V; V_{DS} = 0 V	C_{is}	typ.		8			pF
V_{GS} = V_{DS} = 0	C_{is}	typ.		30			pF
Feedback capacitance, f = 1 MHz							
V_{GS} = 10 V; V_{DS} = 0 V	C_{rs}	typ.		4			pF
Switching times (see Fig.2 + 3)			**J174**	**J175**	**J176**	**J177**	
Delay time	t_d	typ.	2	5	15	20	ns
Rise time	t_r	typ.	5	10	20	25	ns
Turn-on time	t_{on}	typ.	7	15	35	45	ns
Storage time	t_s	typ.	5	10	15	20	ns
Fall time	t_f	typ.	10	20	20	25	ns
Turn-off time	t_{off}	typ.	15	30	35	45	ns
Test conditions:	$-V_{DD}$		10	6	6	6	V
	$V_{GS\ off}$		12	8	6	3	V
	R_L		560	1200	2000	2900	Ω
	$V_{GS\ on}$		0	0	0	0	V

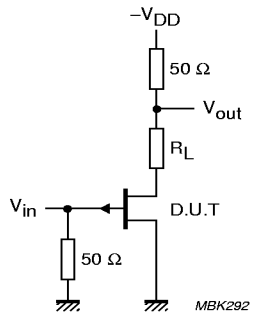


Fig.2 Switching times test circuit.

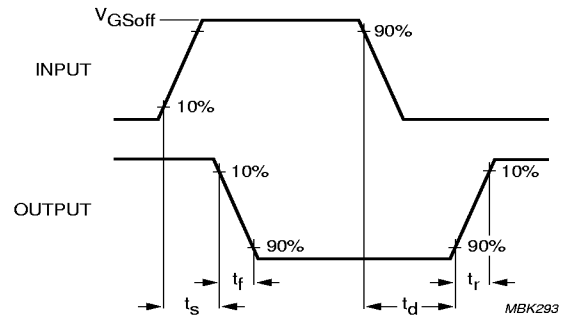
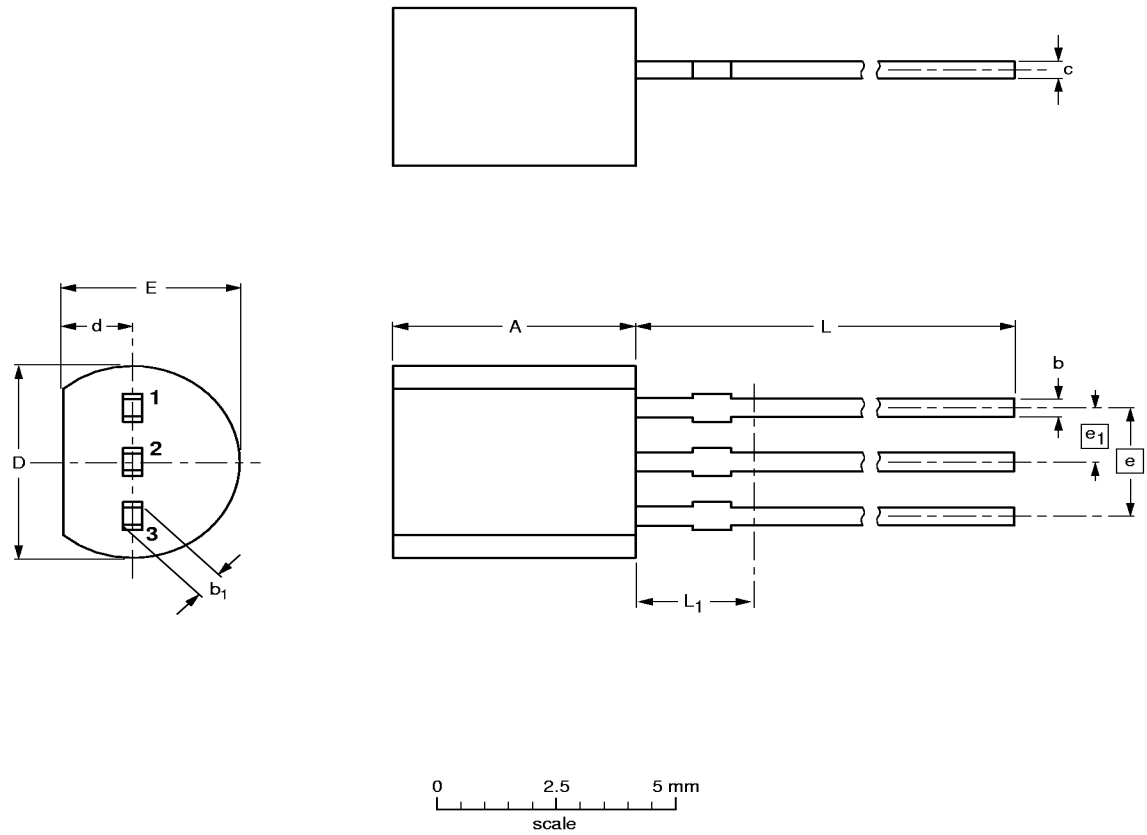


Fig.3 Input and output waveforms; $t_d + t_r = t_{on}$; $t_s + t_f = t_{off}$.

PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads **SOT54**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b_1	c	D	d	E	e	e_1	L	L_1 (1)
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT54		TO-92	SC-43			97-02-28